2024 Q1 Cadence Taiwan Training Schedule

cadence

Click the 'Course Name' to see the course description

CourseCode	Course Name	Duration (Day)	Jan	Feb	Mar	Location	Fees /Per person (Tax Incl.)
Custom Design with Virtuoso Technology							
84460	Virtuoso Layout Suite L - IC6.1.8 //Virtuoso Layout Design Basics	1	4			Hsinchu	TWD 6,000
85081	Virtuoso Layout Suite XL -IC6.1.8 //Virtuoso Connectivity-Driven Layout Transition	1		21		Hsinchu	TWD 12,000
83018	Skill Language Programming -v6.1.8	2			14-15	Hsinchu	TWD 10,400
84453	Skill Programming for IC Layout Design - v6.1.6	1			28	Hsinchu	TWD 5,200
86253-6	ADE Explorer and Assembler v6.1.8 (S1~S4)	2	31-2/1			Hsinchu	TWD 12,000
84474	Virtuoso Spectre RF - v6.1	2	16-17			Hsinchu	TWD 12,000
82086	Analog Modeling with Verilog -A - Spectre17.1	1	23			Hsinchu	TWD 6,000
86241	Mixed Signal Simulations Using Spectre AMS Designer v20.09	1			5	Hsinchu	TWD 6,000
(Q2&Q4 only) 2024Q2	Physical Verification System (PVS) Training v22.1 - *Usage Introduction* (New)	2				Hsinchu	TWD 12,000
86418	Quantus Transistor-Level v 19.1 - T1: Overview and Technology Setup; & T2: Parasitic Extraction	1	30			Hsinchu	TWD 6,000
Digital Design and Signoff							
86141	Innovus Implementation System (Block) v21.1	3			6-7-8	Hsinchu	TWD 18,000
86142	Innovus Implementation System (Hierarchical) v21.1	1			29	Hsinchu	TWD 6,000
82130	Abstract Generator - v5.1.41	1	3			Hsinchu	TWD 6,000
86143	Low-Power Flow with Innovus Implementation System v21.1	1	24			Hsinchu	TWD 6,000
86220	Genus Synthesis Solution with Stylus Common UI v21.1	2	18-19			Hsinchu	TWD 12,000
82169	Voltus Power-Grid Analysis and Signoff v21.1	2			14-15	Hsinchu	TWD 12,000
82147	Tempus Signoff Timing Analysis and Closure v21.1	1			27	Hsinchu	TWD 6,000
Equivalence Checking							
82123	Conformal Equivalence Checking v23.1	1	5			Hsinchu	TWD 6,000
82142	Encounter Conformal Constraint Designer (SDC/CDC Checks)	1		27		Hsinchu	TWD 6,000
82156	Conformal Low-Power Verification Using IEEE 1801 v22.1	1			26	Hsinchu	TWD 6,000
82194	Conformal ECO v21.1	1	11			Hsinchu	TWD 6,000
System Design and Verification							
86218	Xcelium Simulator v22.09	2	25-26			Hsinchu	TWD 12,000
86225	Xcelium Integrated Coverage V20.09	1			1	Hsinchu	TWD 6,000
82143	SystemVerilog Language for Verification v21.1	2			12-13	Hsinchu	TWD 10,400
PCB and Sigrity							
86263	Allegro Package Designer Plus v17.4	3			20-21-22	Hsinchu	TWD 18,000
(Q1&Q3 only) 2024Q1	Allegro High-Speed Constraint Management v17.4	2	9-10			Hsinchu	TWD 12,000
	Sigrity PowerDC and OptimizePI	2		22-23		Hsinchu	TWD 12,000
	PowerSI + Clarity : Wideband Model Extraction Technology	2			26-27	Hsinchu	TWD 12,000
(Q2&Q4 only) 2024Q2	XtractIM : Allegro Sigrity Package Assessment and Model Extraction	2				Hsinchu	TWD 12,000
	SystemSI – Basic	2				Hsinchu	TWD 12,000
	SystemSI – Advanced	2				Hsinchu	TWD 12,000

2023.12.1 updated

Remark ● **Cadence General Tool training= NTD 6,000** (per day/per person) ; **Cadence Language training: NTD 5,200** (per day/per person)