| Q4'18 Cadence China Training Schedule | | | | | |
|---|---|---|---|---|---|
| **BU** | **Course Start Date** | **Course End Date** | **Location** | **Duration** | **Course Title** |
| CIC | 9/25/2018 | 9/25/2018 | Shanghai | 1 | Spectre Simulations Using Virtuoso ADE-vMMSIM14.1IC616 |
| | 9/25/2018 | 9/25/2018 | Beijing | 1 | Spectre Simulations Using Virtuoso ADE-vMMSIM14.1IC616 |
| | 9/25/2018 | 9/25/2018 | Shenzhen | 1 | Spectre Simulations Using Virtuoso ADE-vMMSIM14.1IC616 |
| | 9/26/2018 | 9/26/2018 | Shanghai | 1 | Virtuoso Layout for Advanced Nodes-vICADV12.2 |
| | 9/26/2018 | 9/26/2018 | Beijing | 1 | Virtuoso Layout for Advanced Nodes-vICADV12.2 |
| | 9/26/2018 | 9/26/2018 | Shenzhen | 1 | Virtuoso Layout for Advanced Nodes-vICADV12.2 |
| DV | 9/17/2018 | 9/18/2018 | Shanghai | 2 | SystemVerilog Accelerated Verification with UVM-v1.2 |
| | 10/18/2018 | 10/18/2018 | Shanghai | 1 | Low-Power Simulation with IEEE Std 1801™ UPF-v15.2 |
| | 10/30/2018 | 10/30/2018 | Beijing | 1 | Xcelium Simulator-17.04 |
| | 10/30/2018 | 10/30/2018 | Shanghai (Remotely Join In) | 1 | Xcelium Simulator-17.04 |
| | 11/22/2018 | 11/22/2018 | Beijing | 1 | Acceleration with Palladium XP |
| | 11/22/2018 | 11/22/2018 | Shanghai (Remotely Join In) | 1 | Acceleration with Palladium XP |
| | 11/23/2018 | 11/23/2018 | Beijing | 1 | In Circuit Emulation with Palladium XP |
| | 11/23/2018 | 11/23/2018 | Shanghai (Remotely Join In) | 1 | In Circuit Emulation with Palladium XP |
| | 11/15/2018 | 11/15/2018 | Shanghai | 1 | JasperGold Basic training |
| | 11/15/2018 | 11/15/2018 | Beijing (Remotely Join In) | 1 | JasperGold Basic training |
| | 12/13/2018 | 12/13/2018 | Shanghai | 1 | JasperGold Apps training |
| | 12/13/2018 | 12/13/2018 | Beijing (Remotely Join In) | 1 | JasperGold Apps training |
| ICD | 10/11/2018 | 10/12/2018 | Shanghai | 2 | Tempus Signoff Timing Analysis and Closure-v18.1 |
| SPB | 9/4/2018 | 9/5/2018 | Beijing | 2 | Allegro Design Entry HDL Front-to-Back Flow-17.2-2016QIR6 |
| | 9/13/2018 | 9/14/2018 | Shanghai | 2 | Allegro Design Entry HDL Front-to-Back Flow-17.2-2016QIR6 |
| | 9/20/2018 | 9/21/2018 | Shanghai | 2 | Allegro PCB Editor Basic Techniques -17.2-2016QIR6 |