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In-Design Thermal Analysis for MMIC and RF PCB Power Applications

Next-generation wireless communication and radar systems often demand increased RF power within a smaller footprint to meet the performance and size requirements of their respective commercial and aerospace applications. As a result, RF front-end electronics are exposed to the risk of higher operating temperatures, which degrade RF performance and threaten device reliability. For many device manufacturers, thermal concerns are addressed by imposing excessive thermal margins that reduce optimum performance or excessive heatsinking that adds weight and cost to the final product.

When design teams understand the actual operating temperatures within their electronic systems, designers can make better-informed decisions about heatsinking strategies and guidelines for operating at an optimal thermal margin. Historically, this information is derived through simulations performed by the mechanical team using specialized thermal analysis tools or through build and test methods that can delay development by months. Access to thermal analysis within the framework of the RF design platform provides RF engineers with insight into device operating temperatures as a function of their design decisions without the long wait for this critical data.

The Cadence® AWR Design Environment® platform integrates electromagnetic (EM) and multiphysics analysis tools to support greater simulation accuracy and reduced development cycles for RF and microwave components and systems. Thermal analysis is now possible through the integration of the Cadence Celsius™ Thermal Solver within the AWR® platform. This paper discusses the impact of operating temperature on RF device performance and reliability. It presents a thermal analysis solution based on finite element analysis (FEA) that is integrated within a dedicated RF component design platform for direct access by the RF engineering team. Its associated application note demonstrates the Cadence thermal analysis workflow for a monolithic microwave IC (MMIC) power amplifier (PA) on a PCB.

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Design Overview

Virtually every modern hardware application uses wireless communications and sensing to connect devices, and consequently, requires RF technology to be an integral part of the system that must co-exist with high-speed digital and analog signals across chip, package, and board physical designs. Traditionally, the path to superior performance was custom IC designs based on the latest advanced node technology; however, today's complex designs are more likely to be adopting the heterogeneous integration of different semiconductor technologies to gain a performance edge. RF and mixed-signal engineering efforts have embraced not only diverse semiconductor processes but also advanced cross-fabric packaging and system- and package-in-package (SiP/PiP) technologies, as well as 3D-ICs and integrated antenna-in-package (AiP) solutions. While these devices offer greater performance and functionality within a smaller footprint, they do so at the cost of design complexity and the increased impact of electromagnetic (EM) and electrothermal concerns. To meet the challenges posed by heterogeneous integration, RF designers need to expand their awareness of operating temperatures and thermal management beyond the principle heat sources (power transistors) to include the package, PCB, and surrounding electronics.

Given the impact of EM and thermal effects on RF performance, the need to integrate multi-physics analysis within a design and implementation (IC, package, and PCB) workflow is critical to mitigating design flaws earlier in the product development cycle. For this reason, Cadence is investing significantly in developing its RF design and multiphysics analysis offerings through acquisitions and internal development of core solver technologies and workflow interoperability so that customers can achieve greater first pass success with their most difficult RF system integration challenges.

The Cost of Operating Hot

RF front-end engineers, particularly power amplifier (PA) designers are concerned about device heating and operating temperatures because of the effect on device reliability and performance. While PA designers for mobile and IoT devices are concerned with achieving maximum power-added efficiency (PAE) to preserve battery life. PAE values when operating at the output power back-off levels needed for linearity are often below 50%. This means that less than 50% of the DC bias power is converted into RF power. The DC power that PAs don't convert into RF energy is converted into heat. Device generated heat impacts RF performance with the dominant drain lag effect dependent on both the voltage bias and the channel temperature. In addition, device channel temperature is a primary source for thermal degradation mechanisms leading to shortened device lifetimes (Figure 1, right).

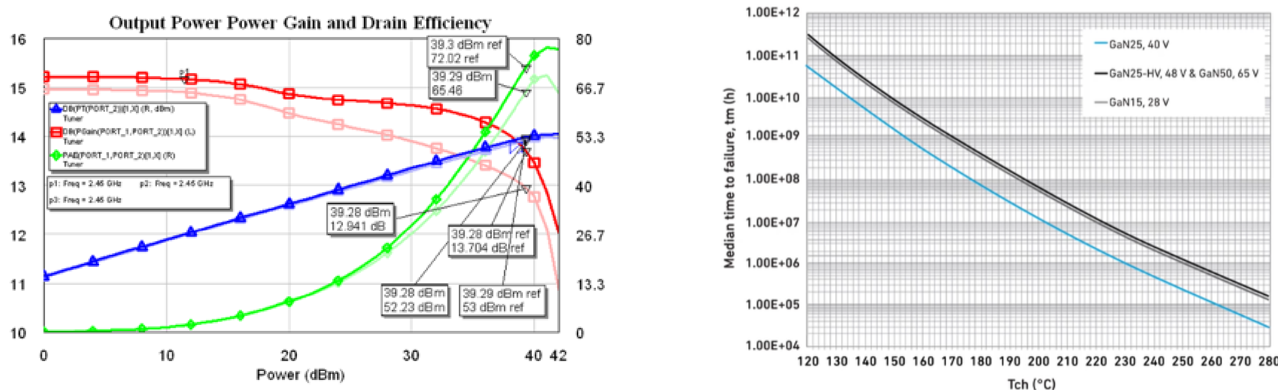


Figure 1: Gallium nitride (GaN) high-electron mobility transistor (HEMT) performance with and without self-heating on the right (image courtesy of Cree) and GaN device mean time to failure (MTTF) vs. thermal conduction heating (TCH) on the left (image courtesy of Qorvo)

GaN transistors provide higher output power densities, wider bandwidths, and improved DC-to-RF efficiencies than their gallium arsenide (GaAs) counterparts, but can run hotter than GaAs devices due to the higher power densities. For this reason, designers using GaN technology need to be aware of operating temperatures and be prepared to mitigate these elevated thermal conditions with effective heatsinking techniques. RF performance degradation for GaN devices is caused by trapping effects related to channel temperature that result in transconductance frequency dispersion, current collapse, gate-and-drain-lag transients, and restricted microwave power output. The impact of operating temperature on RF PA gain and PAE can be observed in the swept input power plots shown in Figure 1 (left).

As mentioned above, the reliability of high-power devices such as silicon-on-carbide (SiC) metal semiconductor field-effect transistors (MESFET) and GaN HEMT devices are directly dependent on maximum operating channel temperature. Therefore, it is important to determine the channel temperature under specific operating modes with a high degree of confidence, particularly for products exposed to elevated temperatures, such as PAs operating under continuous wave (CW) conditions and dissipating large amounts of thermal energy. To ensure safety and offer products with an application appropriate time-to-failure, transistors must operate below the manufacturer's rated operating junction or channel temperatures. Therefore, good thermal management techniques and appropriate characterization of the device operating temperature are critical to avoid costly replacements and/or premature mission failure.

As an example of how much heat can be generated by a typical high-power GaN PA in a basestation, consider a GaN HEMT device with a gate periphery of 28.8mm operating at 28V of drain voltage delivers 120W of continuous wave (CW) power. At a 60% DC-to-RF conversion efficiency, there will be 80W of dissipated heat, which translates into a heat density of over 20kw per square inch (Figure 2). How this heat dissipates from the transistor channel to its environment is critical to understanding if the device is operating above its temperature threshold. This information can be obtained through FEA simulations or actual device testing, performed with infrared (IR) measurements of the bare die, which will only capture the temperature on the surface of the device and not in the actual channel. IR cameras also lack the resolution necessary to accurately measure typical RF to millimeter-wave (mmWave) gate lengths (.25 to .15 μm).

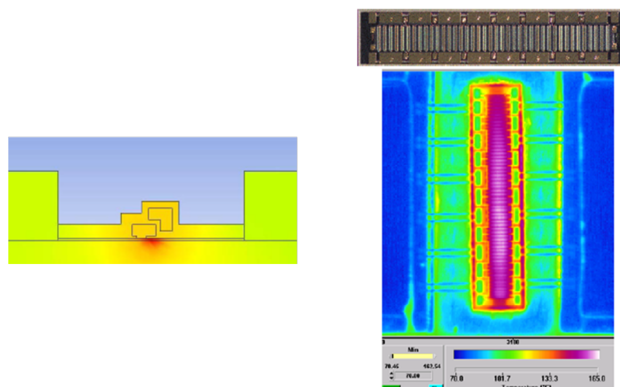


Figure 2: Thermal profile near FET channel (left) using simulation and infrared thermal measurement at the surface of a 28.8mm GaN HEMT (right) (image courtesy of Cree)

This heat will be dissipated from the device channel to the package and PCB through structures such as wire bonds, grounding vias, the semiconductor, and the package materials themselves. Designers need to ensure that the device is operating below the rated operating junction temperature, so they want to know that value and lower it, if possible, using structures such as wire bonds, grounding vias, and other heatsinking paths, which can be optimized through in-design thermal analysis.

Thermal Analysis with the Celsius Thermal Solver

To overcome the thermal challenges impacting RF design performance, Cadence offers the Celsius Thermal Solver, delivering FEA with a massively parallel architecture that enables electrical-thermal co-simulation at the system level. The Celsius Thermal Solver provides Cadence gold-standard accuracy with FEA and computational fluid dynamics (CFD) to analyze the entire thermal response across an entire system. It is capable of detailed thermal model analysis of chips, packages, and boards, offering fine-grain power input for accurate thermal response and detailed power profile for accurate chip thermal models, based on advanced 3D finite element method (FEM) meshing technology (Figure 3). The Celsius Thermal Solver uses parallel processing to shorten simulation run times significantly. It supports multi-threading and distributed processing, making it 10X faster than other thermal analysis tools in completing simulations. The massively parallelized matrix solver can analyze 3D-ICs and complex 3D structures.

To address the needs of the RF component design and system integrator, the Celsius Thermal Solver provides end-to-end capabilities for both in-design and signoff through integration within the AWR Design Environment platform. This allows RF designers to leverage existing RF design details such as layout geometry, material stackup, and simulated power dissipation as input data for Celsius thermal analysis. The integration takes advantage of co-simulation data from the Microwave Office®

harmonic balance (HB) circuit simulator, as well as all the design functionality within the AWR Design Environment platform including support for heterogeneous technology hierarchy for chip, package, and board analysis, parametric optimization, post-processing and back-annotation of color-coded heat maps and 3D meshing.

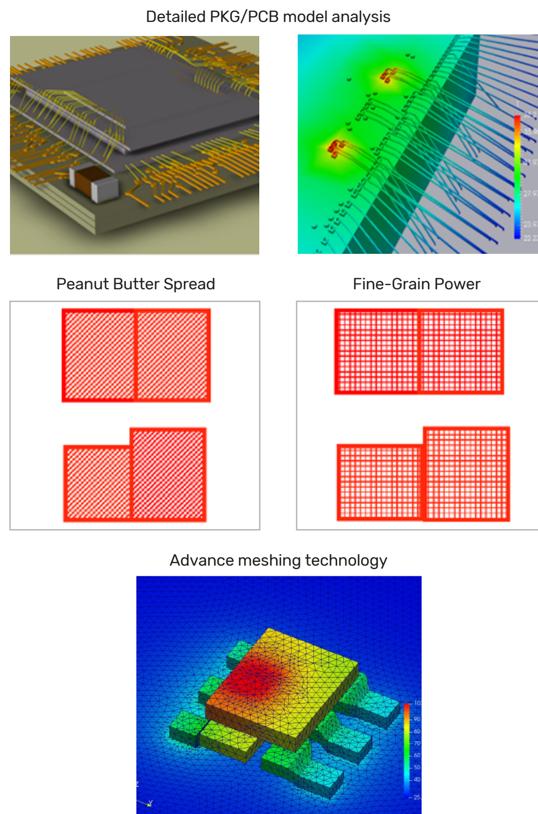


Figure 3: The Celsius Thermal Solver provides accuracy through FEA and CFD analysis, thermal model analysis, detailed power profile, and advanced meshing technology

A Faster Path to Thermal Data

Most high-power designs require thermal analysis. Suppliers developing RF MMICs and PAs often supply their customers with compact thermal device models and information such as thermal resistance from the junction to the bottom case of the package so that the end user can perform junction temperature calculation.

Designers developing their own MMIC or PA designs may want to simulate the transistor channel temperature within the MMIC design, including packaging/assembly (heatsink), as part of the device modeling effort to ensure the operation is below temperature operating limits for reliability and to optimize performance over temperature. It is also important to simulate the thermal dissipation of RF surface mount component(s) on a PCB to ensure it is below the temperature operating limit, as Figure 4 shows.

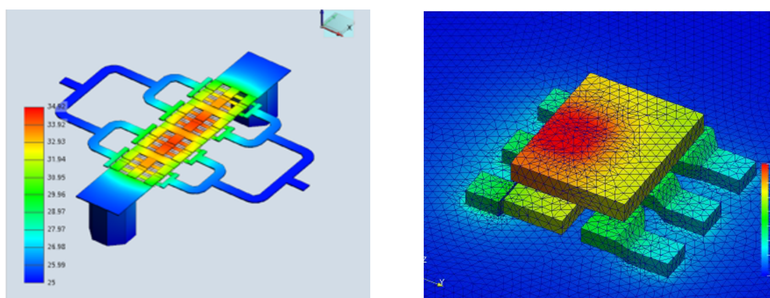


Figure 4: Thermal analysis of a multi-finger RF FET with gate and drain feed manifold and vias (left) and packaged device on PCB

For an RF PCB populated with many thermal sources, such as a balanced or Doherty PA (Figure 5) or a phased array antenna with multiple front-end modules driving individual antenna elements, thermal analysis may be needed to determine the PCB temperature gradient, which can impact the performance of temperature-sensitive components designed directly into the PCB. In RF circuit simulations and EM analysis, PCB materials are defined by parameters, including dielectric constant (Dk) and dissipation factor (Df), both of which also have temperature-based variants. These parameters, as defined in the stackup material, can be linked to a user-specified thermal coefficient for the dielectric constant (TCDk) and dissipation factor (TCDf) to provide insight into the expected behavior of a circuit material with changes in temperature. These parameters detail the amount of change in a material's Dk and Df, respectively, as a function of temperature and will, in turn, impact the simulation results for elements referencing a substrate using temperature sensitive electrical properties. For instance, distributed passive components, such as a hair-pin filter, can suffer from unwanted frequency changes with changes in Dk, including shifts in passbands and stopbands.

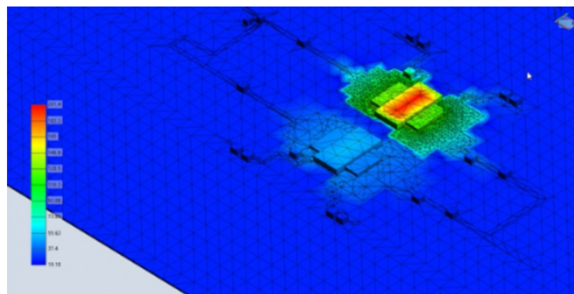


Figure 5: Celsius thermal analysis of a PCB-based Doherty PA clearly indicating the elevated operating temperature of the Peak amplifier

Without direct access to thermal analysis, an RF designer has essentially two approaches to investigating operating temperature. The first is to use a mechanical thermal engineer with access to thermal analysis tools to simulate the operating temperatures using information supplied by the RF design team. This approach often flows from the RF design team to the mechanical engineers by way of a simplified model, which extracts information from the GDS layout of the design with labels that indicate the geometry of the heat source, such as the FET gate fingers, package heatsink, etc. The mechanical engineer then creates a thermal model of the structure either from scratch or by importing an MCAD model, which contains only the simple 3D geometry and doesn't include information about the material properties. The engineer then performs a thermal analysis to create a thermal model (Figure 6). This process is resource-intensive and results in long turnaround times, sometimes up to four weeks. In addition, feedback to the RF engineer on thermo-electrical performance is delayed until the end of the design cycle, rather than being available to uncover and correct issues earlier in the design cycle, before last moment redesigns become necessary.

The second approach is to use build and test methods, which require time-consuming fabrication, assembly, and test. These methods rely on measured data using infrared (IR) techniques to build and test a device. The shortcomings with this approach include the delays associated with device fabrication and test, as well as measurement inaccuracies as described previously in this paper.

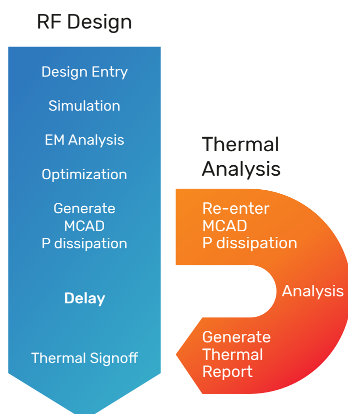


Figure 6: RF design and thermal analysis as performed by different engineering teams using a disjointed workflow

A more efficient approach is to use an integrated workflow that combines the RF design tool with a thermal analysis solver (Figure 7). Cadence provides RF designers direct access to the Celsius Thermal Solver through the Cadence AWR Design Environment software platform. All the information required for thermal analysis is available through the design and simulation data in the AWR platform. Designers use the Microwave Office software to perform their nonlinear RF network analysis using the Microwave Office HB circuit simulator, which produces the power dissipation data that is provided to the Celsius Thermal Solver along with the layout and material stackup information that defines the structure in both the AWR platform and Celsius Thermal Solver. This eliminates the time-consuming task of manual data re-entry because the physical design and simulated RF power dissipation data are automatically provided to the Celsius Thermal Solver through the integration of the solver technology within the AWR framework.

The Celsius analysis can take place directly within the AWR Design Environment, without leaving the platform. The operating temperatures and thermal mapping are back-annotated to operating temperature tables, which link to the associated heat source for easy identification. Temperature color mapping is also back-annotated to the 3D viewer. Alternatively, the structure can be opened within the Celsius Thermal 3D workbench for inspection and analysis in the Celsius native editor. When the simulation is run from within the AWR Design Environment, the Celsius Thermal Solver generates a results summary that is automatically sent back to the AWR environment as a data table listing the temperatures of all the defined heat sources. Users may select any entry from this summary listing, which highlights the contributing heat source (individual component) as its geometry appears in the 2D layout editor, as Figure 8 shows.

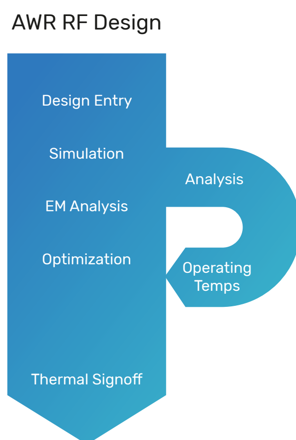


Figure 7: Cadence In-Design Thermal Analysis leverages seamless data transfer from the RF Design platform to shorten development cycles

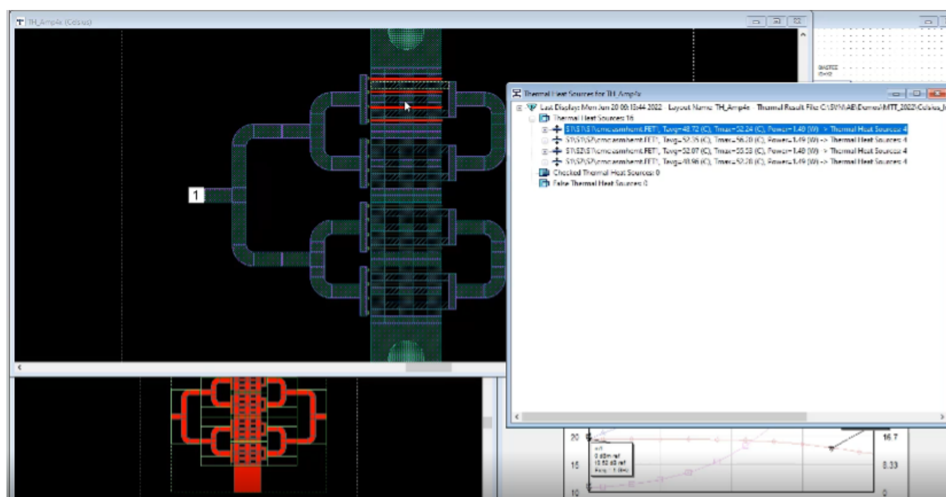


Figure 8: The operating temperature of each heat source is back-annotated into a table in Microwave Office, which highlights the element in the layout viewer when selected from the table entry

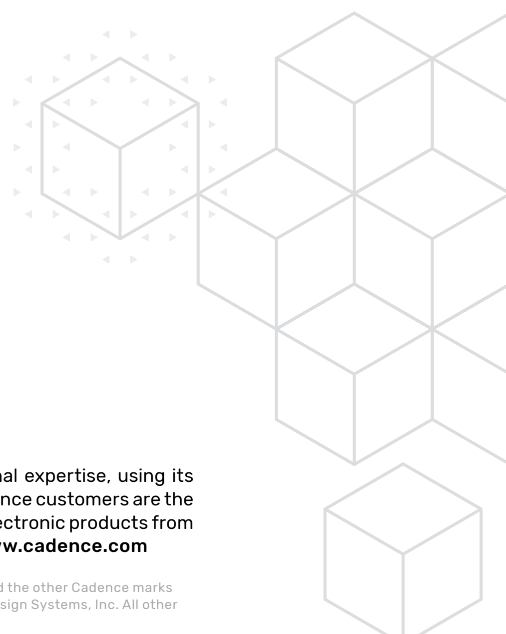
Enabling thermal analysis is a simple and straightforward process that can be implemented by a modeling team or the individual designer. For projects that are enabled for thermal analysis, a user-defined thermal layer with the prefix "Heat_" is added to the drawing layers in the project's layout process file (LPF), providing a layer definition for all rendered heat sources prior to design entry and analysis. The footprint of the heat source can then be drawn on this layer during the model development/entry stage. For designs that include a transistor such as a MMIC, multiple heat sources can be defined within the transistor parameterized cell (PCell) itself, one for each channel of the transistor. In this case, the heat source is represented by a parameterized footprint that is coded into the PCell script by the foundry modeling team. Designers may also hand draw a heat source footprint on the design or within a component footprint, as might be the case for a packaged device. Table 1 shows the results of a simulation vs. measured operating temperatures study that was conducted by a GaN foundry implementing a PDK enabled by Celsius Thermal Solver as part of their validation process. The results show excellent agreement between the Celsius results and those obtained through fabrication and testing.

Power density (W/mm)	Delta Sim-Measured Tj (C)	Delta Simulated – Measured Tj (C)
2.7	1.0	2.8%
4.0	2.8	5.1%
4.7	2.2	3.3%

Table 1. Celsius thermal analysis results for sample FET finger of GaN HEMT compared to measured results.

Conclusion

This paper illustrates the importance of thermal analysis for RF power applications. As RF systems become more densely populated with heat dissipated electonics, the operating temperatures of those devices impact reliability (device lifetime) and performance. Thermal analysis with the Celsius Thermal Solver integrated within the AWR Microwave Office circuit simulator gives designers an understanding of device operating temperatures related to power dissipation and that temperature information can be introduced into an electrothermal model to predict the impact on RF performance. This in-design thermal analysis workflow gives RF engineers the critical operating temperature to improve performance, determine optimum thermal margins and heatsinking strategies while shortening product development cycles, and reducing the number of design iterations.



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