# Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence<sup>®</sup> technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

#### Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff

- System Design and Analysis
- IC Package Design and Analysis

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• Tensilica<sup>®</sup> Processor IP

## PCB Design and Analysis Learning Map

Beginner

Advanced

	Logic [	Design	PCB Design	SI/PI Analysis	Library Development
	Allegro <sup>®</sup> Design Entry HDL Front-to-Back Flow	Allegro Design Entry Using OrCAD <sup>®</sup> Capture	Allegro PCB Editor Basic Techniques	Essential High-Speed PCB Design for Signal Integrity	Allegro PCB Librarian
l	Allegro Design Entry HDL Basics	OrCAD CIS	Allegro PCB Editor Intermediate Techniques	PCB Design at RF – Multi- Gigabit Transmission, EMI Control, and PCB Materials	Allegro EDM PCB Librarian
	Allegro System (NEW) Design Authoring	Allegro EDM Design Entry HDL Front-to- Back Flow	Allegro PCB Router Basics	Allegro Sigrity <sup>™</sup> SI Foundations	Allegro EDM for Administrators
	Allegro System Architect	Allegro Team Design Authoring	Allegro PCB Editor Advanced Methodologies (NEW)	Allegro Sigrity PI	Allegro EDM Administration for OrCAD
l	Allegro Design Reuse	Allegro EDM for Engineers and Designers	Allegro High-Speed Constraint Management	Sigrity PowerDC <sup>™</sup> and OptimizePI <sup>™</sup>	Allegro Design Entry HDL SKILL <sup>®</sup> Programming Language
k	Allegro AMS	Analog Simulation	Allegro Update Training	Sigrity SystemSI <sup>™</sup> for Parallel Bus and Serial Link Analysis	Allegro PCB Editor SKILL Programming Language
H	Simulator	with PSpice <sup>®</sup>	1	Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM	ý v v v v v v v v v v v v v v v v v v v
	Allegro AMS Simulator Advanced Analysis	Analog Simulation with PSpice Advanced Analysis	Advanced Design Verification with the RAVEL Programming Language ••••	Clarity 3D Solver	
New Course 🗰 Number of days for instructor-led course 🔲 🗵 GXL Tiers of Cadence products used in course 🔛 Online Course Available 😥 Digital Badge Available 💿 2020 Cadence Design Systems, Inc.					

Advanced

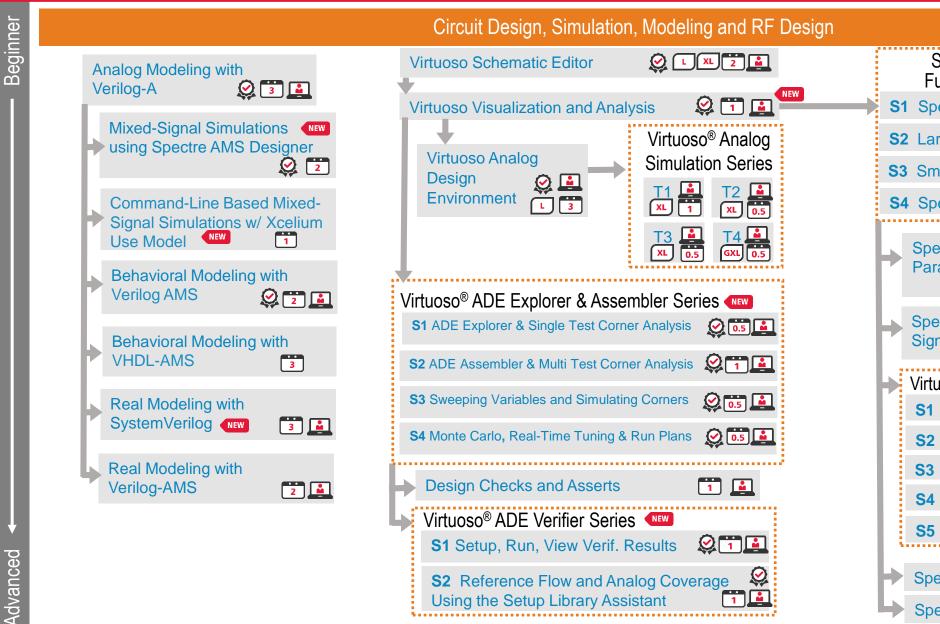
#### IC Package Design and Analysis Learning Map

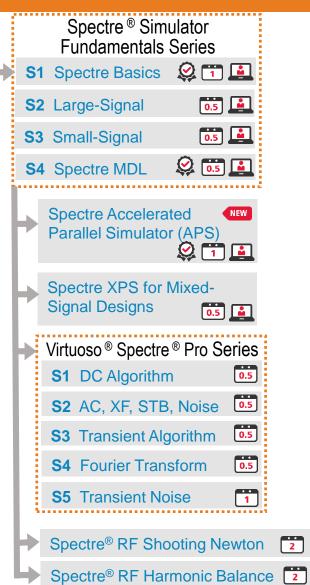
IC Package Design	SI/PI Analysis	
SiP Layout	Allegro Sigrity <sup>™</sup> SI Foundations	
4	2	
Allegro® Package Designer	Allegro Sigrity PI	
4	1	
Allegro FPGA System Planner	Sigrity PowerDC <sup>™</sup> and OptimizePI <sup>™</sup>	
2	🥺 🗂 🛄	
Allegro Sigrity Package Assessment and Model Extraction	Sigrity SystemSI <sup>™</sup> for Parallel Bus and Serial Link Analysis <	
1	3	
OrbitIO <sup>™</sup> System Planner	Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM	
1	2	
Advanced Design Verification with the RAVEL Programming Language	Clarity 3D Solver	
2	1	

Beginner

## Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page





Advanced

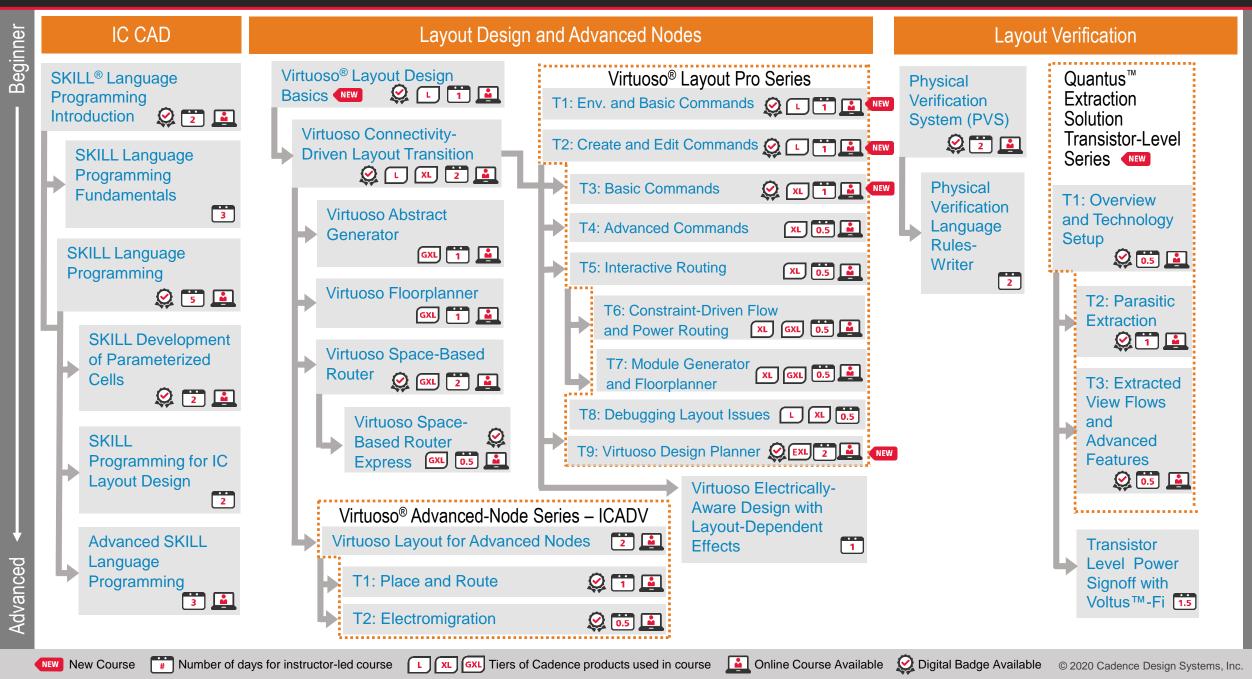
2

**#** Number of days for instructor-led course New Course

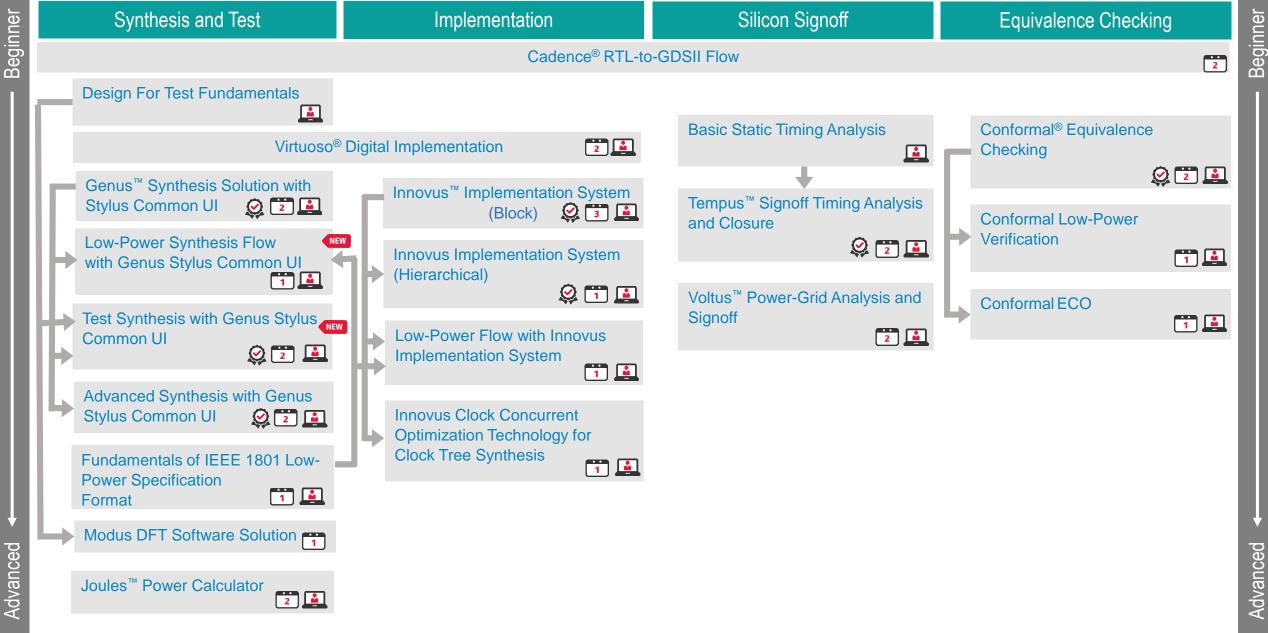
💶 😰 😥 🔝 🔝 🔝 🔝 🖬 🔝 🔝 🔝 Iters of Cadence products used in course 📓 Online Course Available 😥 Digital Badge Available 🛛 🖾 2020 Cadence Design Systems, Inc.

#### Custom IC, Analog and RF Design Learning Map

#### 2 of 2 – see prior page



### Digital Design and Signoff Learning Map



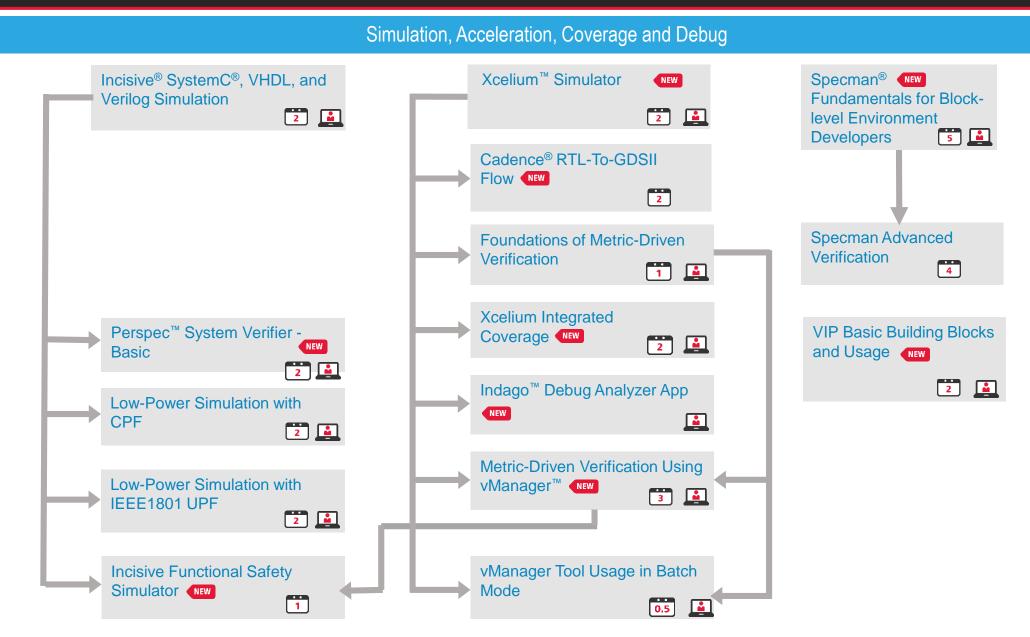
Digital Badge Available

Online Course Available

New Course

Wumber of days for instructor-led course

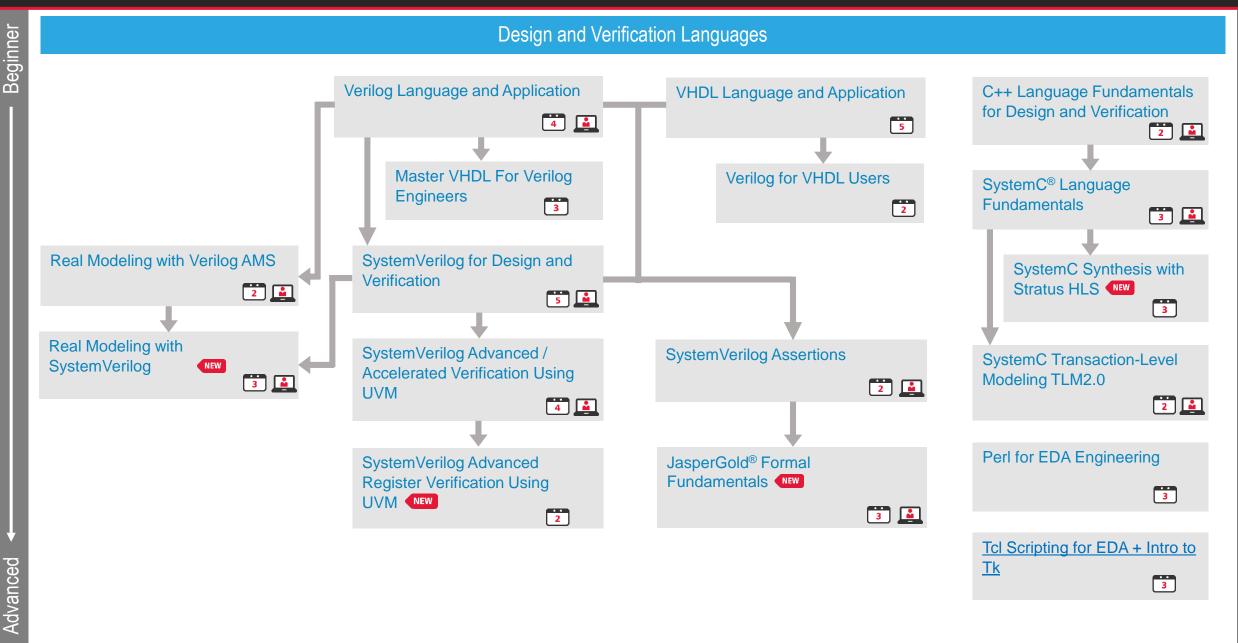
#### System Design and Verification Learning Map



Advanced

New Course

#### System Design and Verification Learning Map



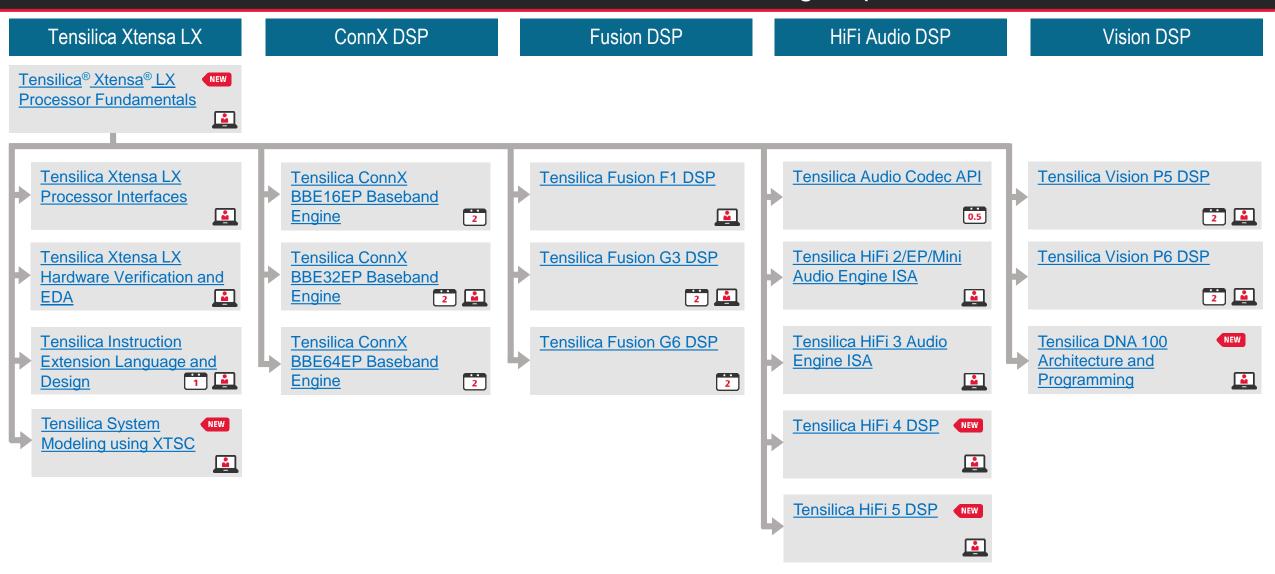
New Course

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Advanced

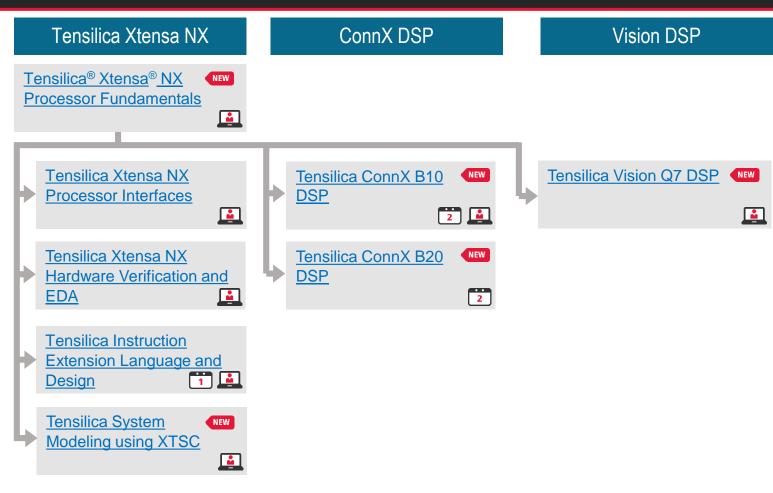
Wumber of days for instructor-led course L GXL Tiers of Cadence products used in course Online Course Available

#### **Tensilica Processor IP Learning Map**



#### Tensilica Processor IP Learning Map

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