Cadence Training Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at https://www.cadence.com/training.

Contents

cadence®

PCB Design and Analysis Learning Map

Beginner

Advanced

Logic Design

- Allegro® Design Entry HDL Front-to-Back Flow — 3 days
- Allegro Design Entry HDL Basics — 1 day
- Allegro System Design Authoring NEW — 1 day
- Allegro System Architect — 2 days
- Allegro Design Reuse — 1 day
- Allegro AMS Simulator — 3 days
  - Allegro AMS Simulator Advanced Analysis — 1 day
- Allegro Design Entry Using OrCAD® Capture — 2 days
- OrCAD CIS — 1 day
- Allegro EDM Design Entry HDL Front-to-Back Flow NEW — 3 days
- Allegro Team Design Authoring — 1 day
- Allegro EDM for Engineers and Designers — 1 day
- Analog Simulation with PSpice® — 3 days
  - Analog Simulation with PSpice Advanced Analysis — 1 day

PCB Design

- Allegro PCB Editor Basic Techniques — 3 days
  - Allegro PCB Editor Intermediate Techniques — 2 days
  - Allegro PCB Router Basics — 2 days
  - Allegro PCB Editor Advanced Methodologies NEW — 1 day
- Allegro High-Speed Constraint Management — 2 days
- Allegro Update Training NEW — 1 day
- Advanced Design Verification with the RAVEL Programming Language NEW — 2 days

SI/PI Analysis

- Essential High-Speed PCB Design for Signal Integrity — 3 days
- PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials — 2 days
- Allegro Sigrity™ SI Foundations — 2 days
- Allegro Sigrity PI — 1 day
- Sigrity PowerDC™ and OptimizePI™ — 1 day
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis — 3 days
- Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM NEW — 3 days
- Clarity 3D Solver NEW — 1 day

Library Development

- Allegro PCB Librarian — 2 days
- Allegro EDM PCB Librarian NEW — 2 days
- Allegro EDM for Administrators — 2 days
- Allegro EDM Administration for OrCAD — 2 days
- Allegro Design Entry HDL SKILL® Programming Language — 3 days
- Allegro PCB Editor SKILL Programming Language — 3 days

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

IC Package Design and Analysis Learning Map

Beginner

Advanced

IC Package Design

- SiP Layout — 4 days, online
- Allegro® Package Designer — 4 days, online
- Allegro FPGA System Planner — 2 days, online
- Allegro Sigrity Package Assessment and Model Extraction — 1 day, online
- OrbitIO™ System Planner — 1 day, online
- Advanced Design Verification with the RAVEL Programming Language NEW — 2 days, online

SI/PI Analysis

- Allegro Sigrity™ SI Foundations — 2 days, online
- Allegro Sigrity PI — 1 day, online
- Sigrity PowerDC™ and OptimizePI™ — 1 day, online
- Sigrity SystemSI™ for Parallel Bus and Serial Link Analysis NEW — 3 days, online
- Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM — 2 days, online
- Clarity 3D Solver NEW — 1 day, online

Beginner

Advanced

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Custom IC, Analog and RF Design Learning Map

1 of 2 – see next page

Beginner

Advanced

Circuit Design, Simulation, Modeling and RF Design

- Analog Modeling with Verilog-A
- Mixed-Signal Simulations using Spectre AMS Designer (NEW)
- Command-Line Based Mixed-Signal Simulations w/ Xcelium Use Model (NEW)
- Behavioral Modeling with Verilog AMS
- Behavioral Modeling with VHDL-AMS
- Real Modeling with SystemVerilog (NEW)
- Real Modeling with Verilog-AMS

- Virtuoso Schematic Editor
- Virtuoso Visualization and Analysis (NEW)
- Virtuoso Analog Design Environment

Virtuoso® Analog Simulation Series

- T1
- T2
- T3
- T4

Virtuoso® ADE Explorer & Assembler Series (NEW)

- S1 ADE Explorer & Single Test Corner Analysis
- S2 ADE Assembler & Multi Test Corner Analysis
- S3 Sweeping Variables and Simulating Corners
- S4 Monte Carlo, Real-Time Tuning & Run Plans

- Design Checks and Asserts

Virtuoso® ADE Verifier Series (NEW)

- S1 Setup, Run, View Verif. Results
- S2 Reference Flow and Analog Coverage Using the Setup Library Assistant

Spectre® Simulator Fundamentals Series

- S1 Spectre Basics
- S2 Large-Signal
- S3 Small-Signal
- S4 Spectre MDL

- Spectre Accelerated Parallel Simulator (APS) (NEW)
- Spectre XPS for Mixed-Signal Designs

Virtuoso® Spectre® Pro Series

- S1 DC Algorithm
- S2 AC, XF, STB, Noise
- S3 Transient Algorithm
- S4 Fourier Transform
- S5 Transient Noise

- Spectre® RF Shooting Newton
- Spectre® RF Harmonic Balance

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Custom IC, Analog and RF Design Learning Map

2 of 2 – see prior page

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction — 2
- SKILL Language Programming Fundamentals — 3
- SKILL Language Programming — 5
- SKILL Development of Parameterized Cells — 2
- SKILL Programming for IC Layout Design — 2
- Advanced SKILL Language Programming — 3

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics — NEW — L — 1
- Virtuoso Connectivity-Driven Layout Transition — L — XL — 2
  - Virtuoso Abstract Generator — GXL — 1
  - Virtuoso Floorplanner — GXL — 1
  - Virtuoso Space-Based Router — GXL — 2
    - Virtuoso Space-Based Router Express — GXL — 0.5

Virtuoso® Layout Pro Series

- T1: Env. and Basic Commands — L — 1 — NEW
- T2: Create and Edit Commands — L — 1 — NEW
- T3: Basic Commands — XL — 1 — NEW
- T4: Advanced Commands — XL — 0.5
- T5: Interactive Routing — XL — 0.5
- T6: Constraint-Driven Flow and Power Routing — XL — GXL — 0.5
- T7: Module Generator and Floorplanner — XL — GXL — 0.5
- T8: Debugging Layout Issues — L — XL — 0.5
- T9: Virtuoso Design Planner — EXL — 2 — NEW

- Virtuoso Electrically-Aware Design with Layout-Dependent Effects — 1

Virtuoso® Advanced-Node Series – ICADV

- Virtuoso Layout for Advanced Nodes — 2
  - T1: Place and Route — 1
  - T2: Electromigration — 0.5

Layout Verification

- Physical Verification System (PVS) — 2
  - Physical Verification Language Rules-Writer — 2

Quantus™ Extraction Solution Transistor-Level Series — NEW

- T1: Overview and Technology Setup — 0.5
- T2: Parasitic Extraction — 1
- T3: Extracted View Flows and Advanced Features — 0.5
- Transistor Level Power Signoff with Voltus™-Fi — 1.5

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available | Digital Badge Available

Digital Design and Signoff Learning Map

Beginner

Advanced

Synthesis and Test

- Design For Test Fundamentals
- Genus™ Synthesis Solution with Stylus Common UI
- Low-Power Synthesis Flow with Genus Stylus Common UI (NEW)
- Test Synthesis with Genus Stylus Common UI (NEW)
- Advanced Synthesis with Genus Stylus Common UI
- Fundamentals of IEEE 1801 Low-Power Specification Format
- Modus DFT Software Solution
- Joules™ Power Calculator

Implementation

- Innovus™ Implementation System (Block)
- Innovus Implementation System (Hierarchical)
- Low-Power Flow with Innovus Implementation System
- Innovus Clock Concurrent Optimization Technology for Clock Tree Synthesis

Silicon Signoff

- Basic Static Timing Analysis
- Tempus™ Signoff Timing Analysis and Closure
- Voltus™ Power-Grid Analysis and Signoff

Equivalence Checking

- Conformal® Equivalence Checking
- Conformal Low-Power Verification
- Conformal ECO

Cadence® RTL-to-GDSII Flow

NEW New Course | # Number of days for instructor-led course | Online Course Available | Digital Badge Available

System Design and Verification Learning Map

Beginner

Advanced

Simulation, Acceleration, Coverage and Debug

- Incisive® SystemC®, VHDL, and Verilog Simulation — 2
- Xcelium™ Simulator NEW — 2
- Specman® NEW Fundamentals for Block-level Environment Developers — 5
- Cadence® RTL-To-GDSII Flow NEW — 2
- Specman Advanced Verification — 4
- Foundations of Metric-Driven Verification — 1
- Perspec™ System Verifier - Basic NEW — 2
- Xcelium Integrated Coverage NEW — 2
- VIP Basic Building Blocks and Usage NEW — 2
- Indago™ Debug Analyzer App NEW
- Low-Power Simulation with CPF — 2
- Metric-Driven Verification Using vManager™ NEW — 3
- Low-Power Simulation with IEEE1801 UPF — 2
- Incisive Functional Safety Simulator NEW — 1
- vManager Tool Usage in Batch Mode — 0.5

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

System Design and Verification Learning Map

Beginner

Advanced

Design and Verification Languages

- Verilog Language and Application — 4
  - Master VHDL For Verilog Engineers — 3
  - Real Modeling with Verilog AMS — 2
    - Real Modeling with SystemVerilog NEW — 3
  - SystemVerilog for Design and Verification — 5
    - SystemVerilog Advanced / Accelerated Verification Using UVM — 4
      - SystemVerilog Advanced Register Verification Using UVM NEW — 2
- VHDL Language and Application — 5
  - Verilog for VHDL Users — 2
  - SystemVerilog for Design and Verification — 5
    - SystemVerilog Assertions — 2
      - JasperGold® Formal Fundamentals NEW — 3
- C++ Language Fundamentals for Design and Verification — 2
  - SystemC® Language Fundamentals — 3
    - SystemC Synthesis with Stratus HLS NEW — 3
    - SystemC Transaction-Level Modeling TLM2.0 — 2
- Perl for EDA Engineering — 3
- Tcl Scripting for EDA + Intro to Tk — 3

NEW New Course | # Number of days for instructor-led course | L XL GXL Tiers of Cadence products used in course | Online Course Available

Tensilica Processor IP Learning Map

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Tensilica Xtensa LX

- Tensilica® Xtensa® LX Processor Fundamentals — NEW
- Tensilica Xtensa LX Processor Interfaces
- Tensilica Xtensa LX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design — 1
- Tensilica System Modeling using XTSC — NEW

ConnX DSP

- Tensilica ConnX BBE16EP Baseband Engine — 2
- Tensilica ConnX BBE32EP Baseband Engine — 2
- Tensilica ConnX BBE64EP Baseband Engine — 2

Fusion DSP

- Tensilica Fusion F1 DSP
- Tensilica Fusion G3 DSP — 2
- Tensilica Fusion G6 DSP — 2

HiFi Audio DSP

- Tensilica Audio Codec API — 0.5
- Tensilica HiFi 2/EP/Mini Audio Engine ISA
- Tensilica HiFi 3 Audio Engine ISA
- Tensilica HiFi 4 DSP — NEW
- Tensilica HiFi 5 DSP — NEW

Vision DSP

- Tensilica Vision P5 DSP — 2
- Tensilica Vision P6 DSP — 2
- Tensilica DNA 100 Architecture and Programming — NEW

NEW New Course | # Number of days for instructor-led course | Online Course Available

Tensilica Processor IP Learning Map

Tensilica Xtensa NX

- Tensilica® Xtensa® NX Processor Fundamentals — NEW
- Tensilica Xtensa NX Processor Interfaces
- Tensilica Xtensa NX Hardware Verification and EDA
- Tensilica Instruction Extension Language and Design — 1
- Tensilica System Modeling using XTSC — NEW

ConnX DSP

- Tensilica ConnX B10 DSP — NEW — 2
- Tensilica ConnX B20 DSP — NEW — 2

Vision DSP

- Tensilica Vision Q7 DSP — NEW

NEW New Course | # Number of days for instructor-led course | Online Course Available