



Learning Maps

Cadence Training Services learning maps provide a comprehensive visual overview of the learning opportunities for Cadence customers. They provide recommended course flows as well as tool experience and knowledge levels to guide students through a complete learning plan. Learning Maps cover all Cadence® technologies and reference courses available worldwide. For course names, descriptions, and schedules, please select the Browse Catalog button at <https://www.cadence.com/training>.

Contents

- PCB Design and Analysis
- Custom IC, Analog, and RF Design
- Digital Design and Signoff
- System Design and Analysis
- IC Package Design and Analysis
- Tensilica® Processor IP
- Computational Fluid Dynamics

PCB Design and Analysis Learning Map

























Beginner

Advanced



















Beginner

Advanced



























Logic Design

Allegro® Design Entry HDL Front-to-Back Flow   3 	Allegro Design Entry Using OrCAD® Capture   2 
Allegro Design Entry HDL Basics   1 	OrCAD CIS  1
Allegro System Capture   2.5 	OrCAD Capture Constraint Manager PCB Flow   1
Allegro System Architect  2 	Allegro EDM Design Entry HDL Front-to-Back Flow   3 
Allegro Design Reuse  1 	Allegro Team Design Authoring  1 
Allegro AMS Simulator  3 	Analog Simulation with PSpice®   3 
Allegro AMS Simulator Advanced Analysis  1 	Analog Simulation with PSpice® using System Capture   3 
	Analog Simulation with PSpice Advanced Analysis   1 












PCB Design

Allegro PCB Editor Basic Techniques   3 
Allegro PCB Editor Intermediate Techniques   2 
Allegro PCB Router Basics  2 
Allegro PCB Editor Advanced Methodologies   1 
Allegro High-Speed Constraint Management   2 
Allegro Update Training  1 
Advanced Design Verification with the RAVEL Programming Language  2 

SI/PI Analysis

Essential High-Speed PCB Design for Signal Integrity  3
PCB Design at RF – Multi-Gigabit Transmission, EMI Control, and PCB Materials  2
Allegro Sigrity™ SI Foundations  2 
Allegro Sigrity PI  1 
Sigrity PowerDC™ and OptimizePI™   1 
Sigrity Aurora    3 
TopXplorer SystemSI for Parallel Bus and Serial Link Analysis   3 
Model Generation and Analysis using PowerSI, Broadband SPICE and 3D-EM   3 
Clarity 3D Solver    2 
Celsius Thermal Solver   1 

Library Development

Allegro PCB Librarian   2 
Allegro EDM PCB Librarian   2 
Allegro Design Entry HDL SKILL® Programming Language  3 
Allegro PCB Editor SKILL Programming Language   3 

IC Package Design and Analysis Learning Map

Beginner



Advanced

Beginner



Advanced

IC Package Design

SiP Layout



Allegro® Package Designer



Allegro FPGA System Planner



Allegro Sigrity Package Assessment and Model Extraction



OrbitIO™ System Planner



Advanced Design Verification with the RAVEL Programming Language



Allegro Package Designer Plus NEW



SI/PI Analysis

Allegro Sigrity™ SI Foundations



Allegro Sigrity PI



Sigrity PowerDC™ and OptimizePI™



TopXplorer SystemSI for Parallel Bus and Serial Link Analysis



Model Generation and Analysis using PowerSI, Broadband SPICE, and 3D-EM



Clarity 3D Solver NEW



Celsius Thermal Solver



NEW

New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available



Digital Badge Available

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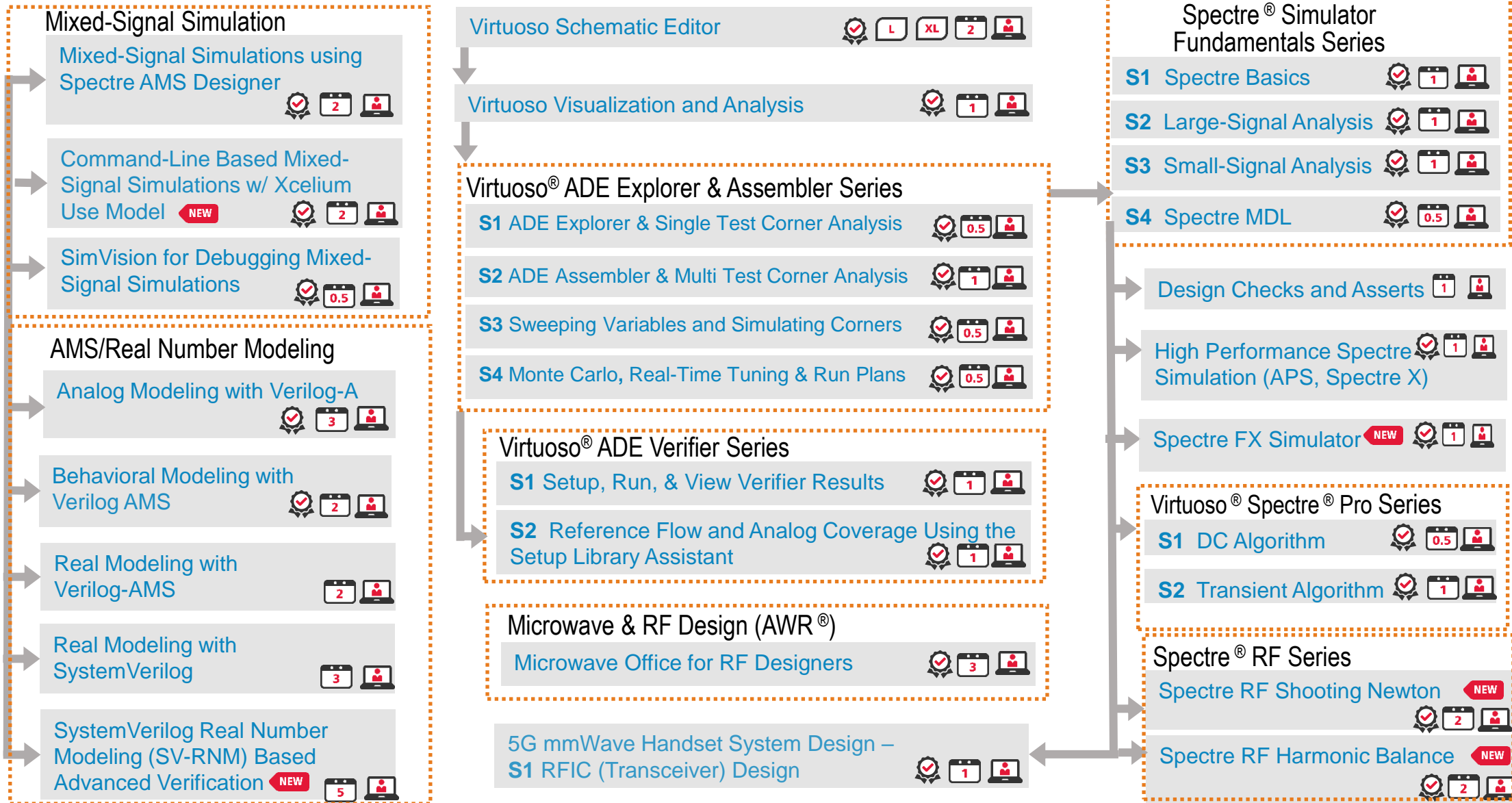
Circuit Modeling, Analog/Mixed-Signal/RF Circuit Design and Simulation

Beginner

Advanced

Beginner

Advanced



Beginner

Advanced

Beginner

Advanced

IC CAD

- SKILL® Language Programming Introduction
- SKILL Language Programming
- SKILL Development of Parameterized Cells **NEW**
- Advanced SKILL Language Programming **NEW**

Layout Design and Advanced Nodes

- Virtuoso® Layout Design Basics
- Virtuoso Connectivity-Driven Layout Transition
- Virtuoso Abstract Generator
- Virtuoso Floorplanner
- Virtuoso® Advanced-Node – ICADV^M
 - Virtuoso Layout for Advanced Nodes
 - T1: Place and Route **NEW**
 - T2: Electromigration
 - Virtuoso Layout for Advanced Nodes and Methodology Platform
- Virtuoso® Layout Pro Series
 - T1: Env. and Basic Commands
 - T2: Create and Edit Commands
 - T3: Basic Commands
 - T4: Advanced Commands
 - T5: Interactive Routing
 - T6: Constraint-Driven Flow and Power Routing
 - T7: Module Generator and Floorplanner
 - T8: Concurrent Layout Editing **NEW**
 - T9: Virtuoso Design Planner **NEW**

Layout Verification

- Pegasus Verification System **NEW**
- Physical Verification System (PVS)
- Physical Verification Language Rules-Writer
- Quantus™ Extraction Solution Transistor-Level Series
 - T1: Overview and Technology Setup **NEW**
 - T2: Parasitic Extraction **NEW**
 - T3: Extracted View Flows and Advanced Features **NEW**

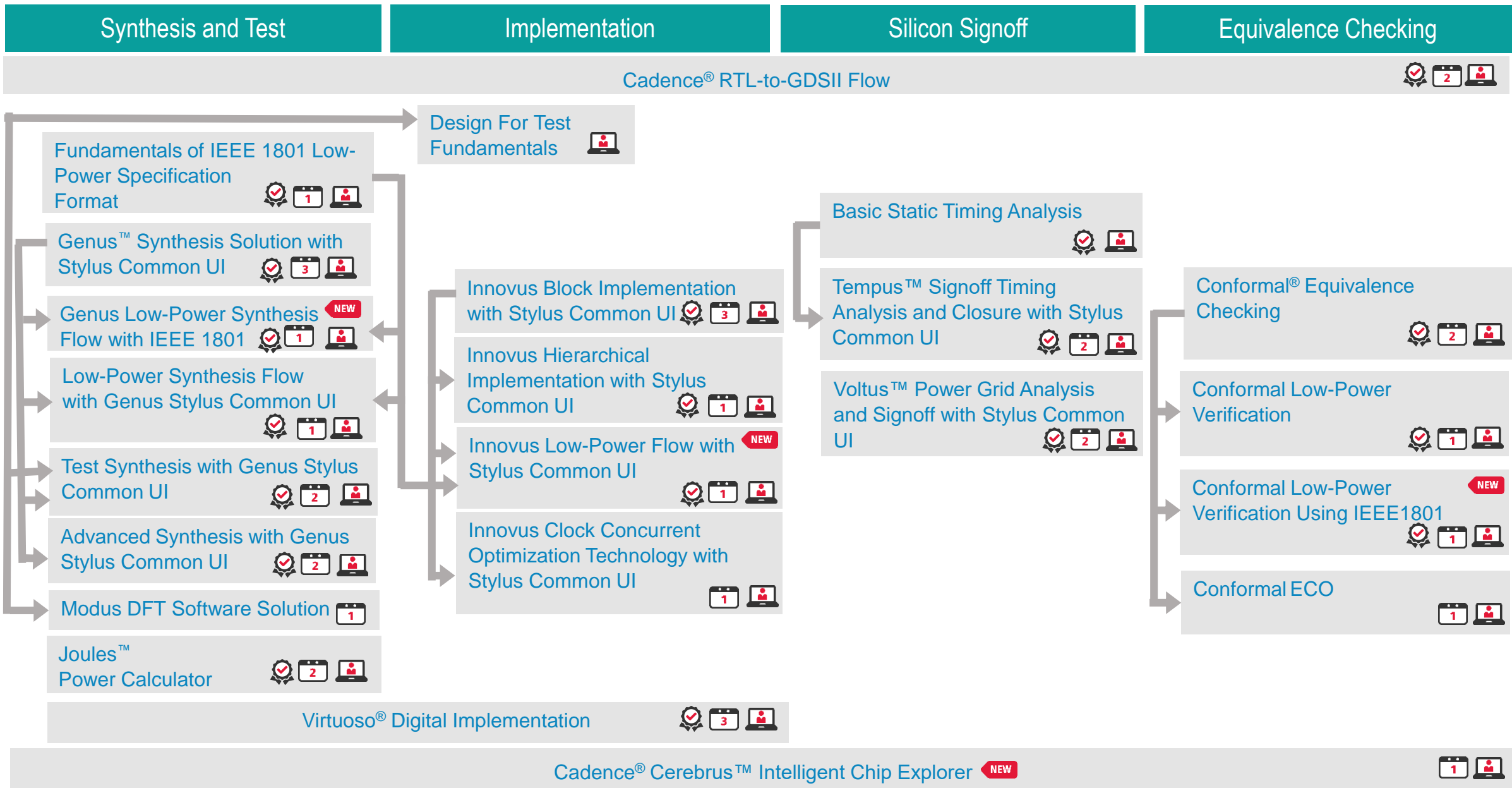
Digital Design and Signoff Learning Map

Beginner

Advanced

Beginner

Advanced

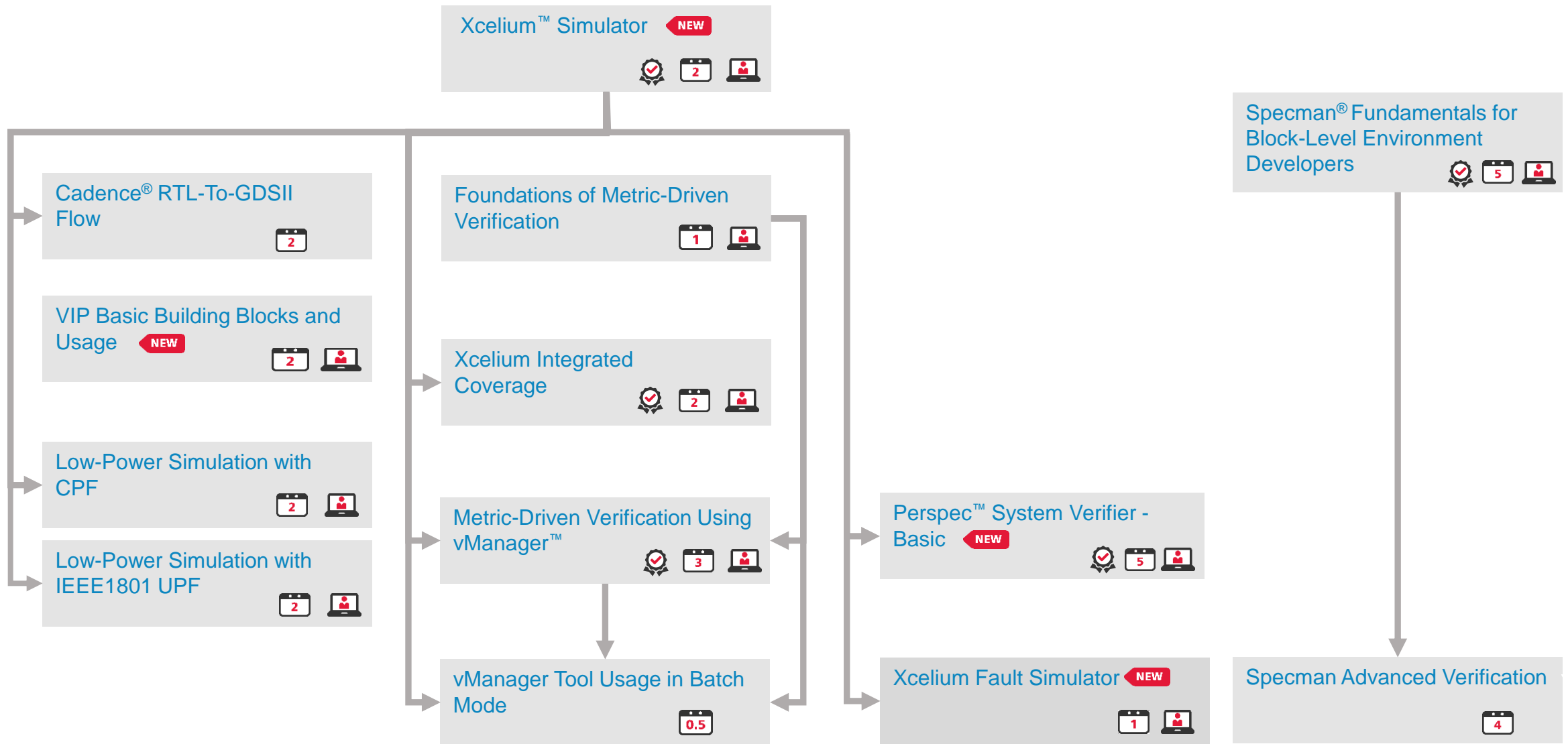


System Design and Verification Learning Map

Beginner

Beginner

Simulation, Coverage and Debug



Advanced

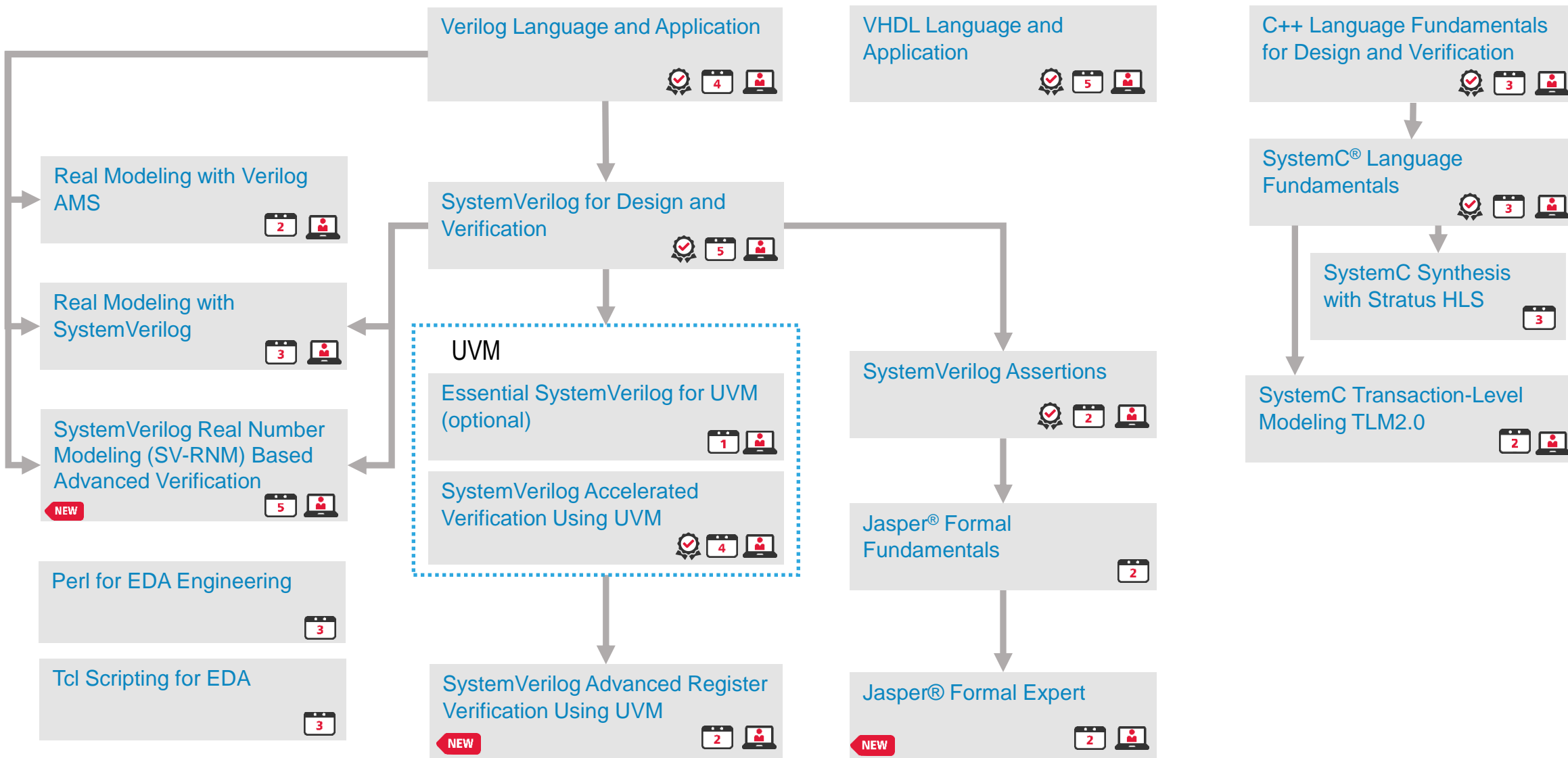
Advanced

System Design and Verification Learning Map

Beginner

Beginner

Design and Verification Languages



Advanced

Advanced

Tensilica Processor IP Learning Map

Tensilica Xtensa LX

ConnX DSP

Fusion & FloatingPoint DSP

HiFi Audio DSP

Vision DSP

[Tensilica® Xtensa® LX Processor Fundamentals](#)



[Tensilica Xtensa LX Processor Interfaces](#)



[Tensilica Xtensa LX Hardware Verification and EDA](#)



[Tensilica Instruction Extension Language and Design](#)



[Tensilica System Modeling using XTSC](#)



[Tensilica ConnX BBE16EP Baseband Engine](#)



[Tensilica ConnX BBE32EP Baseband Engine](#)



[Tensilica ConnX BBE64EP Baseband Engine](#)



[Tensilica ConnX 110 and 120 DSP Family](#)



[Tensilica Fusion F1 DSP](#)



[Tensilica Fusion G3 DSP](#)



[Tensilica Fusion G6 DSP](#)



[Tensilica FloatingPoint DSP Family](#)



[Tensilica Audio Codec API](#)



[Tensilica HiFi 2/EP/Mini Audio Engine ISA](#)



[Tensilica HiFi 3 Audio Engine ISA](#)



[Tensilica HiFi 4 DSP](#)



[Tensilica HiFi 5 DSP](#)



[Tensilica Xtensa Audio Framework](#)



[Tensilica Vision DSP Family](#)



[Tensilica Xtensa Neural Network Compiler v2](#)



[Tensilica DNA 100 Architecture and Programming](#)



New Course



Number of days for instructor-led course




Online Course Available


Tensilica Xtensa NX


ConnX DSP


Vision DSP



[Tensilica® Xtensa® NX Processor Fundamentals](#) 



[Tensilica Xtensa NX Processor Interfaces](#) 

[Tensilica Xtensa NX Hardware Verification and EDA](#) 



[Tensilica Instruction Extension Language and Design](#) 

[Tensilica System Modeling using XTSC](#) 

[Tensilica ConnX B10 DSP](#)  

[Tensilica ConnX B20 DSP](#)  

[Tensilica Vision DSP Family](#)  

[Tensilica Xtensa Neural Network Compiler v2](#)  



New Course



Number of days for instructor-led course



Online Course Available

Computational Fluid Dynamics


Beginner





Advanced


Fidelity		
Turbomachinery	Meshing	Auto Aero


Fine
Marine

Fidelity Turbo: Introduction 

Fidelity Automesh for Unstructured Meshing 

Fidelity Flow 

Fine Marine for Beginners 

Fine Marine for Advanced Users 

Beginner



Advanced



New Course



Number of days for instructor-led course



Tiers of Cadence products used in course



Online Course Available



cādence®

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