DATASHEET

cadence®

Specman Elite

Verification automation from block to chip to system levels

Part of the Cadence® Xcelium™ functional verification platform, Specman® Elite blends leading-edge process automation technology with the comprehensive Universal Verification Methodology (UVM) to simplify and speed verification. Specman Elite automates the entire verification process, from individual blocks to full chips to the project level. With Specman technology, designers benefit from increased productivity and a predictable path to high-quality silicon.

Specman Elite Testbench

Successful verification of today's multimillion-gate designs requires optimal speed and efficiency. But verification teams often struggle to squeeze in enough cycles to ensure that functional bugs won't surface in silicon. The Specman Elite testbench is a comprehensive environment that accelerates and simplifies all aspects of verification automatic generation, data and assertion checking, and functional coverage analysis, in addition to supporting the UVM. Verification teams can extend the functionality of Specman Elite with the Specman ESL testbench, which provides a high-throughput channel between the testbench and the device under test (DUT), and enables plan-to-closure verification automation of embedded software exactly as if it were another part of the DUT.

With other elements from the Xcelium platform, including Verification IP (VIP), hardware acceleration and emulation, analog/mixed-signal/RF verification, and formal assertion verification, Specman Elite supports any testbench, HDL, software, or assertion IP. Many engineers already create testbenches in C, VHDL, Verilog, and SystemVerilog, and may have invested time and effort in internal solutions. But, realistically, these tools are rewritten project to project without allowing for significant reuse. Nor do they contain the engines and aspect-oriented programming (AOP) support already built into Specman technology, such as the patented constraint solver that generates stimulus automatically.

With Specman Elite and UVM-*e*, engineers can use the powerful *e* verification language to capture rules from the specifications and use the information to automate verification. The Specman methodology finds even the subtlest corner-case bugs because it eliminates misrepresentations of specifications.

Benefits

- Leverages the *e* language's unique AOP capabilities
- "IntelliGen" constraint solvers automate test generation with unprecedented distribution control and scalability
- Speeds debugging via automatic data and assertion checking

- Increases predictability with functional coverage analysis
- Supports all IEEE-standard languages including *e*, SystemC®, C, C++, VHDL, Verilog, and SystemVerilog
- Supports built-in IP reuse to leverage existing investments in VIP
- Works with all major simulators

Features

Constraint-driven stimulus generation

Specman Elite provides constraint-driven test generation that automates the process of generating functional verification tests. By specifying constraints, engineers can target the generator quickly and easily to create any test in their functional test plan. They can also generate tests on the fly based on the current design state, making it possible to detect hard-to-reach corner cases.

Data and assertion checking

Powerful temporal constructs allow verification specialists and designers to capture complex protocols for assertion checking. On-the-fly data checking and generation provides context-specific expected values. With Specman Elite, verification engineers can use any combination of gray-, black-, or white-box checking to speed debugging.

Functional coverage analysis

An executable functional test plan measures the progress of verification, and functional analysis automatically identifies holes in the test coverage. Since functional coverage is a meaningful and direct measure of the completeness of verification, functional coverage analysis increases predictability in verification schedules.

Rapid creation of libraries of reusable tests

Specman Elite fully supports UVM Methodology, which describes how to create reusable verification components in any IEEE-standard language and provides guidelines for setting up multi-language interfaces to existing IP for maximum operational flexibility. The process is based on the time-tested *e* Reuse Methodology (*e*RM) and System Verification Methodology (SVM).

Testbench static analysis

Static analysis catches testbench bugs and coding surprises early in the verification cycle. It performs more than 200 checks to flag syntactic, semantic, and functional errors. A flow that includes testbench analysis before simulation will check the code for reusability per UVM-compliance rules, testbench performance issues, race conditions, pre-defined coding style rules, generation constraints, and semantic ambiguities. These rules can be expanded to include corporate style guidelines. The result: With the powerful rule-definition GUIs and graphical analysis tools, engineers write working code correctly the first time.

HDL simulator interfaces

Specman Elite integrates with all leading HDL simulators and supports a high-performance, direct kernel interface to all Xcelium simulators. Users can sample and drive internal signals of the DUT.

Transaction-level modeling and SystemC support

Specman Elite provides SystemC interface mechanisms to drive and monitor transaction-level models (TLMs) as well as signal-level models. You can apply Specman verification methodologies to the verification of SystemC architectural models using TLMs and reference models including mixed SystemC/RTL environments, and co-verify SystemC models used for software development. In addition to supporting Xcelium simulators, Specman Elite provides interface adaptors for SystemC simulators including OSCI and CoWare ConvergenSC. With Specman Elite, engineers can create a single verification environment to verify their SystemC model and then reuse it throughout the entire downstream flow, from RTL simulation to acceleration and emulation.

C and Python interface

Specman Elite provides interfaces to C and to Python, including one-call C/Python functions from *e*, and call *e* methods from C/Python code. Using the C/Python interface, users can integrate checkers or any other applications implemented in other languages.

HW/SW co-verification

Specman Elite supports all leading hardware/software co-verification tools. They also integrate seamlessly with Xcelium software extensions in the Specman ESL co-verification environment to enable functional testing of both hardware and software. Early integration and debugging of HW/SW systems eliminates errors and shortens time to market for the combined system.

Specifications

Language support

- Testbench
  - *e* (IEEE 1647)
  - Interface to SystemVerilog (IEEE 1800) testbenches

- Device under test
  - Verilog (IEEE 1364-1995 and IEEE 1364-2001 extensions)
  - SystemVerilog (IEEE 1800)
  - VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 (VITAL 2000))
  - SystemC (OSCI SystemC v2.2, IEEE 1666)
  - PSL (IEEE 1850)
  - SVA (IEEE 1800)
  - C and C++ models
  - MATLAB models
  - Analog models in Verilog-A, VHDL-A, or SPICE formats
  - Post-silicon hardware
  - Specman ESL supports embedded software and high-throughput connections to accelerated and emulated DUTs

Testbench analysis

- 200+ checks to lint and analyze code for:
  - Code reusability as per UVM compliance rules
  - Performance analysis
  - Race conditions
  - Pre-defined coding style rules
  - Generation constraints
- Graphical interface to sort, filter, and analyze messages with source code

Support for Cadence IP

- VIP—Supports all simulation-based Universal Verification Components (UVCs), transaction-based VIP, assertion-based VIP, and SpeedBridge® rate adapters used in emulation
- Direct kernel interface to all Xcelium platform simulators
- Direct C language interface
- Socket interface
- PLI (IEEE 1364)
- DPI (IEEE 1800)
- VPI (PLI 2.0, IEEE 1364)
- VHPI

Platforms

- Sun Solaris
- HP-UX
- Linux

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 30 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, Rapid Adoption Kits, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.

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