Cadence Palladium Z1 Enterprise Emulation Platform

Built for resilience, scalability, and productivity

A state-of-the-art enterprise emulation platform, the Cadence® Palladium® Z1 platform is a successor to the Palladium XP series. The new product unifies best-in-class simulation acceleration and emulation technologies into a platform that is 8X more densely integrated and is optimized for multi-user emulation throughput and efficiency. Its unique and massively parallel processor-based compute engine, along with software automation, accelerates verification of SoCs, subsystems, and IP blocks, as well as system-level validation, helping to improve your development cycle while maintaining high product quality and performance. The rack-based platform is easy to manage and scale, making it convenient to deploy in data centers while offering remote access to globally distributed teams.

Overview

Scale up with the Palladium Z1 platform, built for resilience, scalability, and productivity. The platform comes with new industry-first features like dynamic target relocation and flexible job placement to deliver the most effective use of system resources. Compared to competing solutions, the Palladium Z1 platform also offers, in a single environment to boost emulation throughput and productivity:

- Compile speeds of up to 140MG/hr. with a single workstation
- The best utilization due to its allocation scheme
- Runtime performance of up to 4MHz
- Faster upload speeds
- Enhanced debug capabilities

The processor-based compute engine and Verification Xccelerator Emulator (VXE) software in the platform have been designed for up to 2X faster compiles, to run higher performance verification, and to enable flexible new use models that transcend traditional emulation compared to the already state-of-the-art Palladium XP platform. The Palladium Z1 platform optimizes system design and verification with features including a capacity for up to 9.2 billion gates, advanced debug and coverage, hardware/software co-verification, interactive offline debug with Virtual Verification Machine (VVM), and support for Dynamic Power Analysis (DPA), hard and soft intellectual property (IP), and metric-driven verification.

Figure 1: Palladium Z1 platform

System-Level Verification Challenge

Traditional verification tools have not kept pace with the rapid rate at which SoC/ASIC design size and complexity are growing. This widens the hardware/software verification gap, limiting reusability and productivity, which can increase the likelihood of re-spins and schedule delays. As RTL/gate design size increase, traditional simulators slow down significantly, which delays hardware/software (system) integration and prolongs the overall verification cycle.

Today's SoC designs can be complex in terms of number of IP blocks and other components (see Figure 2). As systems grow more sophisticated, the risk associated with not adequately verifying hardware/software interaction

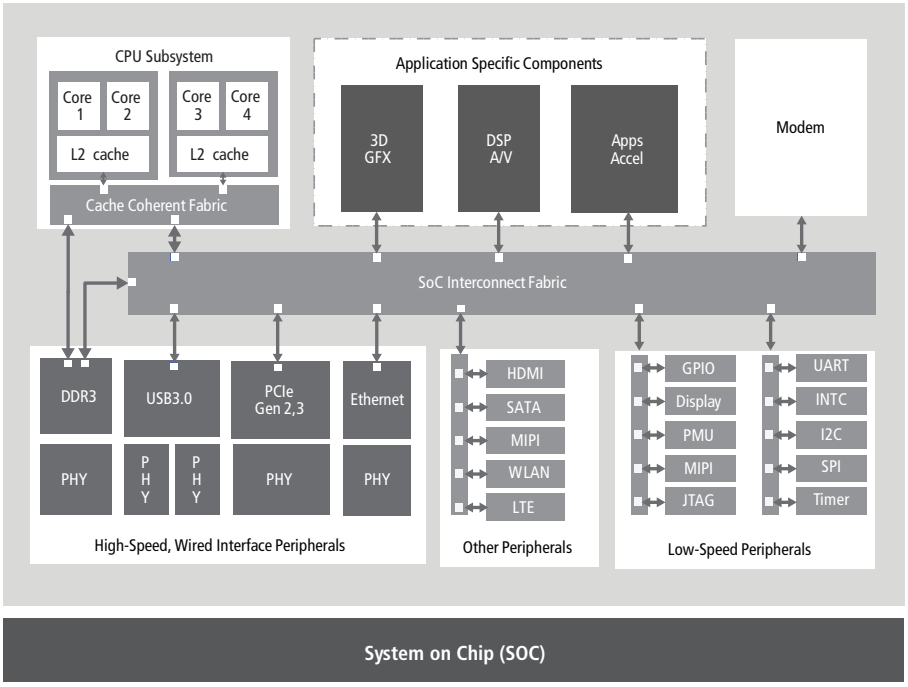

Figure 2: This example SoC design includes hardware and software

also grows. Scalable performance is critical to eliminating these risks. Traditional hardware-assisted verification tools can take you outside of your native simulation environment with steep learning curves, lengthy setup times, difficult debug methods, and reuse issues. Furthermore, there is no easy way to transition among simulation, simulation acceleration, and emulation environments without re-compilation.

Enhancing Productivity

Productivity of a good verification engine is measured by considering four defining factors (Figure 3):

1. **Build:** With design sizes in the multi-million gates, you can spend hours/days compiling your designs before they can be run on the emulator. This task also often requires multiple host resources. If you can reduce the time taken to compile jobs, you can also reduce your overall verification time, so you can have a higher number of design turns in the allocated verification time.

   With its advanced VXE software capabilities, the Palladium Z1 platform enables compile speeds of up to 140MG/hr. with a single workstation, helping with multiple design turns in one day.

2. **Allocate:** Emulation resources are very precious, with multiple users looking to access these systems to complete their verification tasks. Efficient resource management can maximize the number of jobs running on the system. System granularity of job allocation plays a big role in determining the number of concurrent jobs that can be run on a system with minimal or no waste of resources. In practical use-case scenarios, different jobs often complete at different times, creating resource availability in different parts of the system.

   Features like dynamic job allocation and relocation can simplify resource allocation for new jobs while even re-arranging existing jobs. This ensures maximal utilization.

   The Palladium Z1 platform has advanced, industry-first job re-shaping, relocation, and target relocation capabilities that allow you to very efficiently manage system resources for high utilization. High job parallelization is also available with the Palladium Z1 platform due to its industry-best 4MG job-size granularity. This enables you to run in parallel multiple simultaneous jobs, ranging from IP blocks to sub-system to system-level designs.

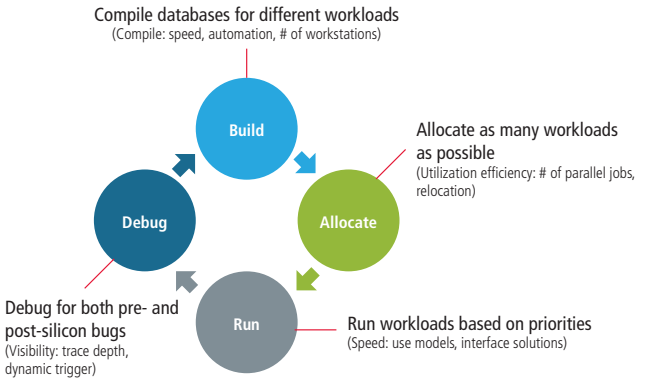

Figure 3: Measuring productivity of a verification engine

3. **Run:** Often, runtime performance is considered to be the most important parameter in determining system productivity. However, factors like runtime debug, which affect runtime performance significantly, should not be overlooked. Versatility in use models supported by the system ensures that the verification task covers all elements involved with hardware-

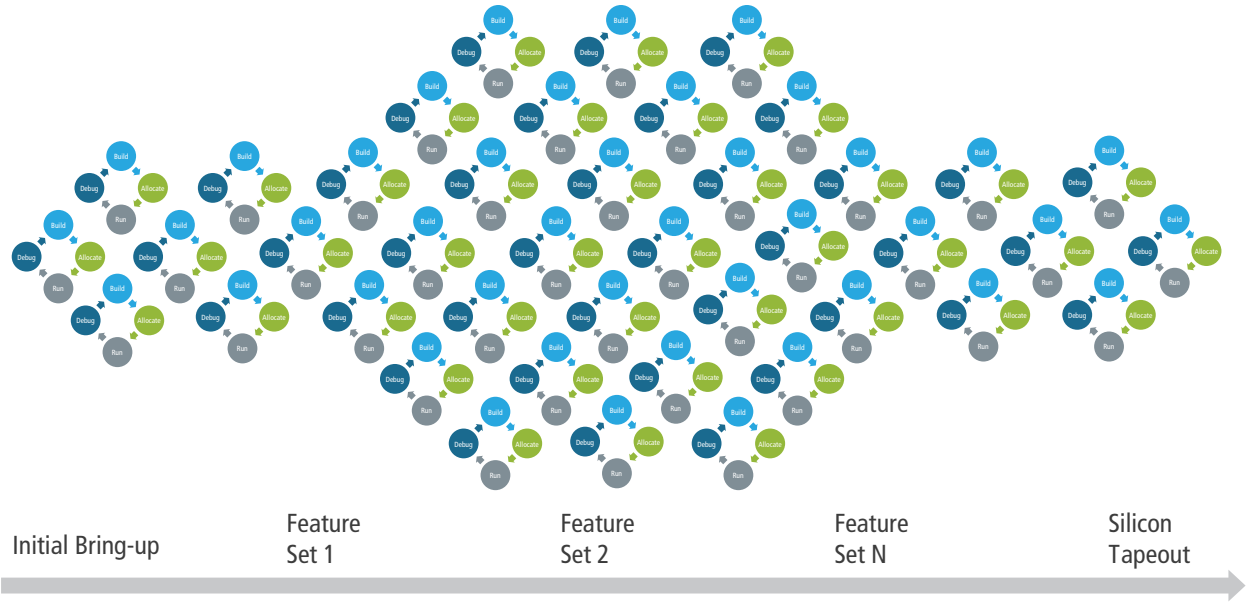

Figure 4: Verification loops through the product design and verification stages

software integration. A comprehensive interface support to cover major industry-supported protocols both via speed-rate adapter or verification IP custom-tuned for hardware-assisted verification enables you to thoroughly test your designs well before tapeout and silicon availability, so you can avoid any late surprises and improve time to market.

The Palladium Z1 platform has a runtime performance of up to 4MHz, which allows you to quickly run designs to identify any potential issues with the design.

4. **Debug:** A system's debug capabilities can be classified as runtime debug and offline debug. Having a good feature set with deep trace depth available with dynamic triggering allows you to catch bugs at runtime, saving valuable time and directly translating into time-to-market savings. Unlike many industry systems, the Palladium Z1 platform doesn't suffer from a drastic drop in runtime performance when runtime debug is enabled. In addition, offline debug features allow you to capture recordings of the run and then take the captured database offline to debug, freeing up the valuable emulation resource for other jobs. The key requirement for maximizing productivity is to have most of the feature set that you would have during online debug available in an offline mode. For example, flexibility to have trigger events and to capture flip-flop and memory states would enable you to effectively perform offline debug tasks.

The Palladium Z1 platform has advanced debug capabilities for both online and offline use modes like FullVision, InfiniTrace, dynamic probes, SDL trigger, and a new state-of-the-art VVM for efficient offline debug while most of the online debug features are available.

Following this approach, each design turn would involve going through the entire cycle of build, allocate, run, and debug. Typically, there are multiple stages of a project, starting from IP block verification to integration of individual IP blocks to form a sub-system, combination of multiple sub-systems into a full system, software bring-up on the hardware design, and, finally, tapeout (Figure 4). Depending on the stage of the project, multiple iterations of this loop (build, allocate, run, and debug) need to be performed simultaneously in order to bring the SoC to market on time without any surprises. Any incremental time saved with any of the stages will lead to significant savings in the overall design cycle.

With the Palladium Z1 platform, you'll have the flexibility of quick compile, very efficient allocation, fast runtime, and comprehensive debug to quickly verify your designs without cutting any corners, so you can confidently take these designs to tapeout.

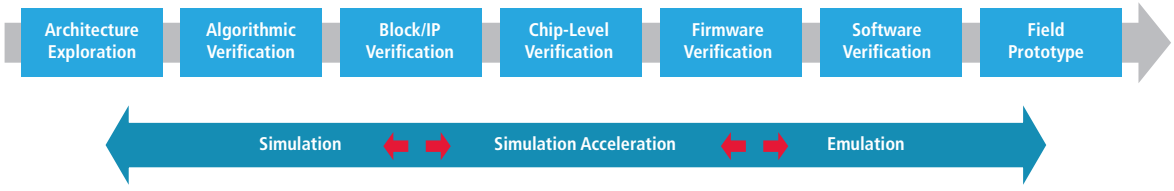

Figure 5: The Palladium Z1 platform offers an enhanced, unified flow and allows users to transition between simulation, simulation acceleration, and emulation for better performance and enhanced debug.

IP to System-Level Verification Solution

To keep pace with the demands of advanced SoC development and to close the hardware/software verification gap, the Palladium Z1 platform is the industry's most comprehensive for verification. The platform enhances the verification flow and capabilities and removes the barrier to entry in acceleration and emulation by offering a unified environment that leverages the native simulation environment. The environment also allows a Cadence Incisive® simulator user to hot-swap from simulation to acceleration, or emulation environments at runtime without re-compilation (Figure 5). The Palladium Z1 platform can be used at various design and verification phases, from early architectural analysis to block, chip, and system-level integration to software development and system verification.

The Palladium Z1 platform offers enhancements above and beyond what traditional acceleration and emulation use models offer. The platform supports use models to improve verification productivity through:

- Metric-driven verification (MDV) acceleration
- Hardware verification language-based testbench acceleration
- In-circuit emulation (ICE)
- In-circuit acceleration (ICA)
- Universal Verification Methodology (UVM) acceleration
- Vector-based acceleration (VBA)
- Comprehensive coverage capabilities
- Power shutoff verification (PSO)
- Dynamic Power Analysis (DPA)
- And other techniques for RTL and gate level emulation (Figure 6)

Palladium Z1 Features

Feature	Benefits
Highest scalability and versatility	• Enables centralized or locally distributed verification computing with scalable resources to serve a single user or as many as 2304 simultaneous users for a capacity up to 9.2 billion gates • Supports versatile executable functional models at various abstraction levels (C/C++, SystemC®, instruction set or cycle accurate, silicon, RTL, gates)
Highest flexibility	• Dynamic job relocation allowing you to flexibly move jobs within the system on-the-fly to accommodate new incoming jobs to maximize system utilization and productivity • Dynamic target relocation to virtually connect to any target of choice without any physical re-cabling, allowing full flexibility of verifying designs with real-time traffic

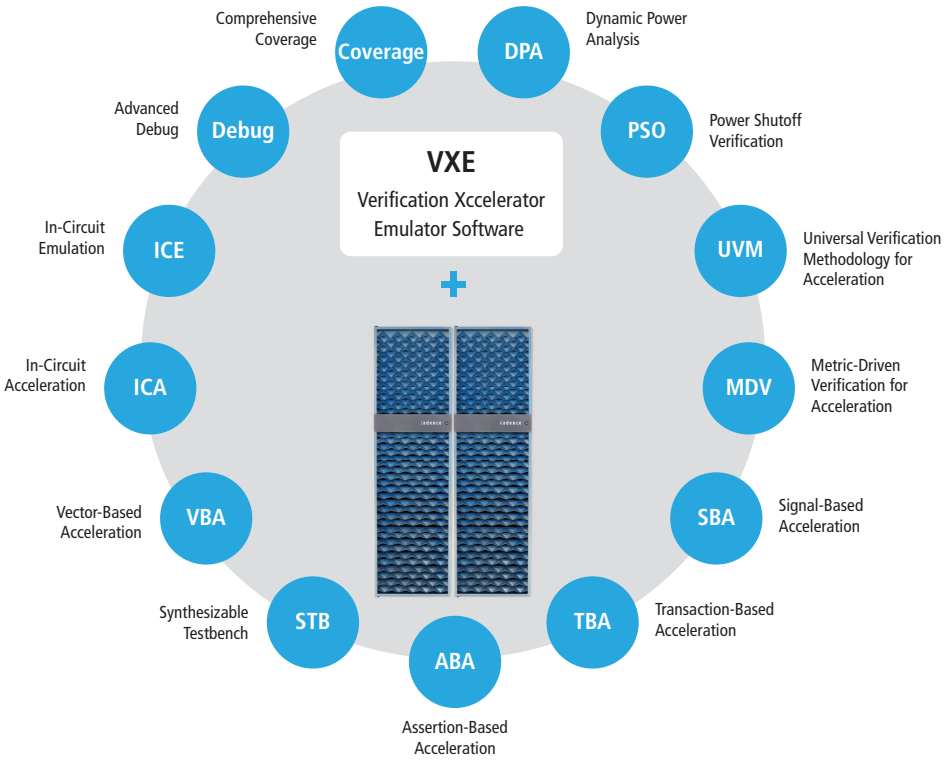

Figure 6: Palladium Z1 platform offers comprehensive use models for HW/SW co-verification and system realization across RTL and gate-level designs

Feature	Benefits
Unparalleled verification computing productivity	• Enables quick bring-up with its fast, automated, intelligent compiler that includes a rich set of behavior construct support and congruent (match) behavior between simulation and hardware
Better design bring-up predictability	• Boosts runtime predictability with "hot-swap" to acceleration or emulation and the most flexible use models • Enables quick system-level bring-up with the comprehensive and proven Cadence SpeedBridge® portfolio (comprising hardware rate adapters for standard protocols) and Accelerated VIP • Enables early software/firmware/driver development and verification with Emulation Development Kit (EDK)
Platform extension	• Supports MDV for acceleration with coverage and advancements in hardware verification/hardware design languages • Supports the most comprehensive hard or soft verification IP for standard protocols • Enhances system-level low-power analysis with DPA option and power-verification techniques such as power shutoff
Superior debug capabilities	• Supports advanced debug capabilities like SDL trigger, FullVision, dynamic probes, Infinitrace, and Virtual Verification Machine (VVM) to identify any design bugs

Comprehensive Enterprise Emulation Platform

The Palladium Z1 compute engine consists of an advanced custom processor grid. This processor grid allows the Palladium Z1 platform to support up to 9.2 billion ASIC gates of design capacity, supporting a single user or up to 2304 simultaneous users, and running up to 4MHz with 18.4TB of built-in memory.

The VXE software component of the Palladium Z1 platform integrates simulation, acceleration, and emulation in a single environment, thereby enabling fast bring-up, superior debug, hot-swap capability, and fast, fully automated, predictable design compile on a single workstation.

Flexible Resource Allocation and Model Support

The Palladium Z1 platform offers verification computing resources with best-in class flexibility for an enterprise. It can be utilized for multiple projects/tests as it can support multiple concurrent jobs—including those with a mixture of acceleration and emulation—without affecting other jobs. You can set up jobs queuing for regression or interactive use and relocate jobs to other available symmetrically configured resources without re-compilation. Furthermore, you can respond to on-demand resource allocation requirements as project needs evolve.

With its dynamic job relocation capabilities, the Palladium Z1 platform allows you to assign large incoming jobs into non-consecutive parts of the system, thus fully utilizing the system resources. Often, different jobs get completed at different points in time, creating gaps in system utilization and reducing efficiency of usage. With the platform, you can move existing jobs seamlessly and on-the-fly to other parts of the system.

Dynamic target relocation is an industry-first feature introduced in the Palladium Z1 platform. This capability allows you to fully benefit from in-circuit-emulation with the flexibility of virtually switching between targets. Jobs being run on any part of the system can now connect to any target without any physical re-cabling required, so users from remote locations can easily complete their verification tasks on designs with multiple interfaces.

A highly flexible verification platform is critical for assembling the SoC rapidly. The Palladium Z1 platform allows rapid integration of various abstracted IP models on the basis of performance, accuracy, availability, reuse, hard/soft IP, or legacy environment-support requirements. It supports industry interface standards such as the Standard Co-Emulation Modeling Interface (SCE-MI), SystemVerilog DPI, and Virtual Interface (VIF), which provide even more flexibility in expanding the system-level verification environment.

Since the Palladium Z1 platform supports concurrent use of different types of IP, testers, debuggers, and test stimulus generators, it significantly reduces the development schedule (Figure 7). You can comprehensively verify system interactions

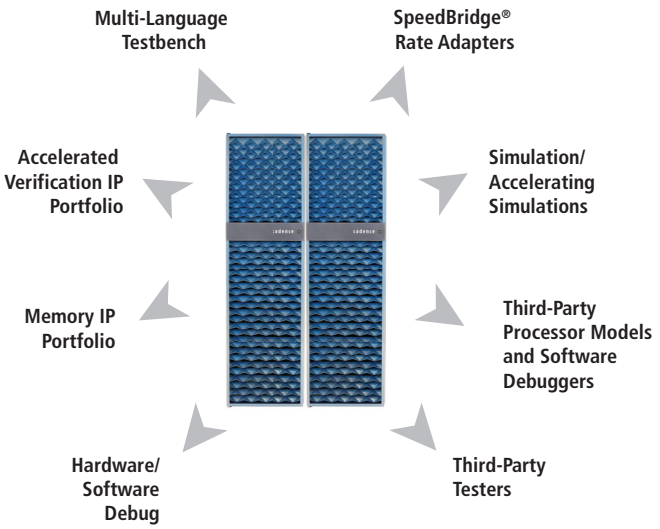

Figure 7: Palladium Z1 platform allows concurrent use of different types of models

with a real-world environment and/or a testbench for a directed, constrained-random, or MDV environment while significantly improving emulation throughput.

Power Analysis

The Palladium Z1 platform offers system-level power verification in which the common side file is read to help you verify power intent through the integrated Cadence SimVision™ waveform viewer and log file messages.

- **Dynamic Power Analysis (DPA):** Identifies "true peaks" during long runs, which are often not captured in simulation. Integration of the Cadence Genus™ Synthesis Solution power estimation engine with the Palladium Z1 platform provides the first high-performance, cycle-accurate, integrated solution delivering full-system power analysis of hardware/software designs.
- **Unified Power Format (UPF/IEEE1801) and Common Power Format (CPF):** Specifies the low-power intent modeled into UPF/IEEE1801/CPF, so low-power activities can be captured and shown in waveform for debugging. Also aids in effective low-power verification including memory/flip-flop (FF) randomization after power shut off (PSO). Let's you complete UPF-/CPF-aware DPA tasks for true power analysis.

Advanced Debug

The Palladium Z1 platform enhances the design debug process with its easy-to-use, high-performance debug features. Its advanced debug capabilities support hardware/software co-verification and various assertions languages.

Feature	Specification
FullVision	• At-speed full visibility of any nets for typically up to 2 million samples during runtime
Dynamic Probes	• Fast waveform upload of up to 80 million samples • Select signals to analyze before run
InfiniTrace	• Unlimited trace-capture depth • Allows you to revert back to any checkpoint and restart emulation from that point
State Definition Language (SDL)	• Allows simple or complex trigger on set of events • Dynamic netlist creation for accurate trigger mechanism without recompilation
Save and Restore	• Save valuable cycle time and restore run from a "save" point. (e.g., OS boot completion)
Virtual Verification Machine (VVM)	• Capture long traces at runtime into an offline database for debug at a later point in time • Captures FF/memory states and allows using SDL to set triggers and observe interesting scenarios in an offline mode

Specifications

	Palladium Z1 (XL)	Palladium Z1 (GXL)
Scalable capacity and I/O	• Capacity: Up to 6.1 billion gates • I/O: Up to 147,456 • CMOS 3.3V, 2.5V, 1.8V, 1.5V, LVDS, HSTL, SSTL	• Capacity: Up to 9.2 billion gates • I/O: Up to 221,184 • CMOS 3.3V, 2.5V, 1.8V, 1.5V
Default dedicated user memory	Up to 12.3TB	Up to 18.4TB
Simultaneous users	From 1 to 1536 users	From 1 to 2304 users
Architecture	Custom advanced processors	
Design format and language support	• HDL: RTL (VHDL, Verilog, SystemVerilog) and gate-level netlist • HVL: C++, SystemC, Specman e, SystemVerilog, and Universal Verification Methodology (UVM) acceleration • Assertions: System Verilog Assertions (SVA), Property Specification Language (PSL), Incisive Assertion Library, and Open Verilog Library (OVL)	
Memory transformation and Memory Model Portfolio (MMP)	• Options for memory placement, compaction, squeezing, read port splitting, and merging • Comprehensive portfolio supports most industry-standard memory models	
Hardware/software interfaces, connecting to third-party tools/IP/environment	• Various standards: SCE-MI 2.X and TLM support • Most comprehensive SpeedBridge and Accelerated VIP portfolio for standard protocols supporting most market segments • Application-specific interfaces: C/C++, PLI, VPI, SystemVerilog DPI, DPI-SystemC, VHPI, etc. and support for third-party interfaces to the standalone VXE model	
Fast compile	Up to 140 million gates per hour with a single workstation for RTL	
Performance	Up to 4MHz, with built-in IXCOM profiler that tunes performance for acceleration	
Advanced debug	FullVision, InfiniTrace, dynamic probes, SimVision Debug, virtual verification machine, SDL, DPA, etc.	
Flexible clocking	Supports a very large number of synchronous, asynchronous, and gated clocks	

Ecosystem Support

- Verification IP (VIP), Accelerated VIP, and in-circuit emulation for system-level and application software testing prior to silicon availability. Includes full compatibility with the SpeedBridge hardware adapter product that connects real-world systems with the design being emulated to provide simple and direct integration.
- Cadence Joules™ RTL Power Solution integrates seamlessly with the Palladium emulation platform for early RTL power analysis and optimization
- Hybrid environment of hardware and software for efficient hardware/software debug, faster boot, and early software/system validation with RTL/netlist
- MDV acceleration and embedded testbench to enable you to follow a comprehensive plan-to-closure methodology that increases verification predictability, productivity, and quality
- Cadence Stratus™ High-Level Synthesis (HLS) for quick design and verification of high-quality RTL implementations from abstract SystemC, C, or C++ models, providing 10X better productivity than traditional RTL design and reducing IP development cycle from months to weeks
- Case-based verification with Cadence Perspec™ System Verifier, reducing complex system-level coverage-driven test development time from weeks to days

Supported Workstations and Operating Systems*

- X86 instruction set architecture workstations
- OS type: Linux
  - RHEL 6 (64 bit)
  - SuSE 11 (64-bit)

** Please check with your Cadence representative for the latest information and additional details as they are subject to change without notice.*

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet. In addition, they provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

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