APPLICATION **NOTE**

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Ensuring Accurate Broadband EM Analysis with Allegro PCB Designer

This application note outlines the electromagnetic (EM) simulation and verification flow between the Cadence® Allegro® PCB Designer and Cadence AWR Design Environment® platform, specifically AWR® Microwave Office® circuit design software and the AWR AXIEM® EM simulator for a PCB design. The example uses a simple transmission line with known response to validate the approach and demonstrate interoperability between design and analysis tools. Following the export/import steps, the creation of an EM simulation structure is shown and the tradeoffs between design complexity and simulation time are discussed. Lastly, an introduction to basic EM port configuration and simulation settings is provided and a comparison of the AWR AXIEM EM simulation against measured results is shown.

Design Overview

One of the less complex PCB structures for RF applications is the two-port, 50 Ω transmission line, also known as a "thru line". The thru line is often used to calibrate test equipment, such as a vector network analyzer, supporting calibration of a reference measurement plane at the middle of the PCB when combined with other PCB-based calibration standards. The structure used in this application note varies from a simple thru line by including two narrower, slightly higher impedance transmission line sections to address the impedance mismatch introduced by the coax-to-microstrip transition, as well as a pair of transmission line discontinuities separated by small section of 50 Ω line. The supporting coax-to-PCB transitions and discontinuities can be replicated and modeled with a combination of planar and 3DEM simulation tools. The PCB consists of a transmission line, two discontinuities, and ground via arrays. Step-by-step instructions are provided for how to export a PCB design created in Allegro PCB Designer via an IPC-2581 compatible file and then import the file into AWR Design Environment platform through the PCB import wizard.

Step 1: Export an IPC-2581 Compatible File from Allegro PCB Designer

The design file *AWR-Allegro-Demo-1.brd* is shown in the Allegro PCB Designer in Figure 1. The PCB layers include a top metal signal (RF) layer, ground plane, power layer, and bottom ground. Each metal layer is separated by dielectric layers consisting of FR-4 material (.36 and .71mm thick). The grounds on the top, bottom, and center ground planes are connected by vias. Verify that the correct PCB layer stackup has been entered into the cross-section editor of Allegro PCB Designer. The project layer information shown in the cross-section editor will be exported as part of the IPC-2581 file (Figure 2).

Figure 1: Allegro PCB file

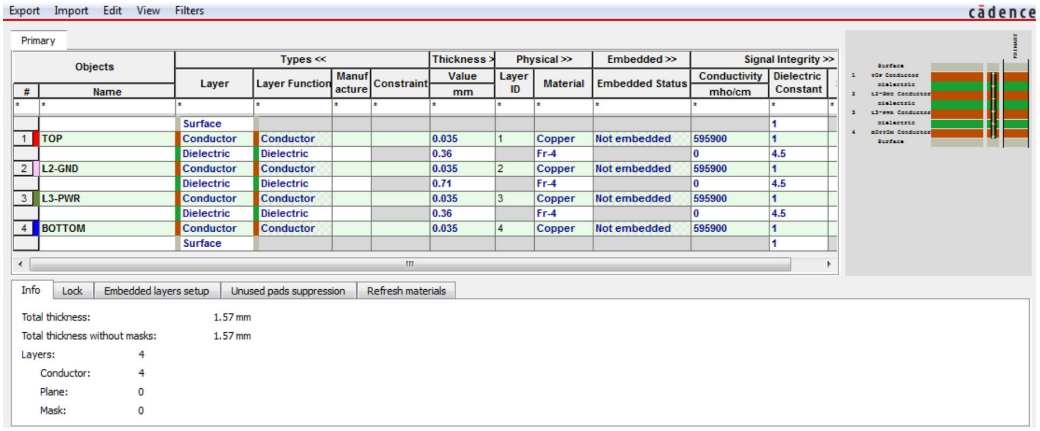

Figure 2: Allegro Cross-Section Editor dialog box

In Allegro PCB Designer, select *File – Export – IPC-2581…* to open the dialog, as shown in Figure 3. Select the desired output file name, the IPC-2581 version (IPC-2581-B), and the functional mode (USERDEF).

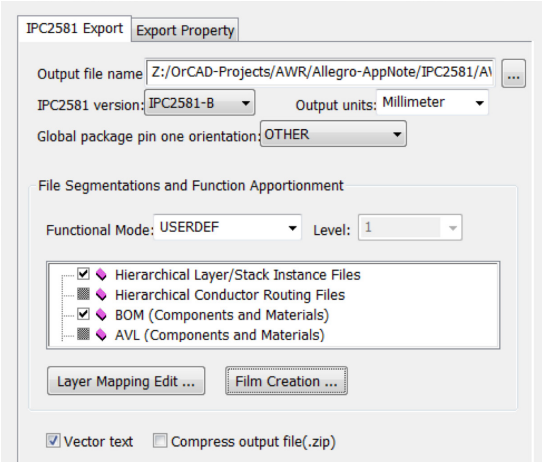

Figure 3: Allegro Export Editor dialog box

Utilize the layer mapping editor to select the layers to be exported. (Note: To streamline the import and simulation setup for EM simulations using AWR AXIEM software, the number of layers should be minimized to contain only the relevant metal structures.) Assembly and paste mask layers should not be exported. Selecting *Export* in the IPC-2581 dialog exports the specified layers of the board file into a compatible file.

Step 2: Import the IPC-2581 File into AWR Design Environment

In the AWR Design Environment, open the PCB Import wizard that is located in the wizard section of the project manager (Figure 4).

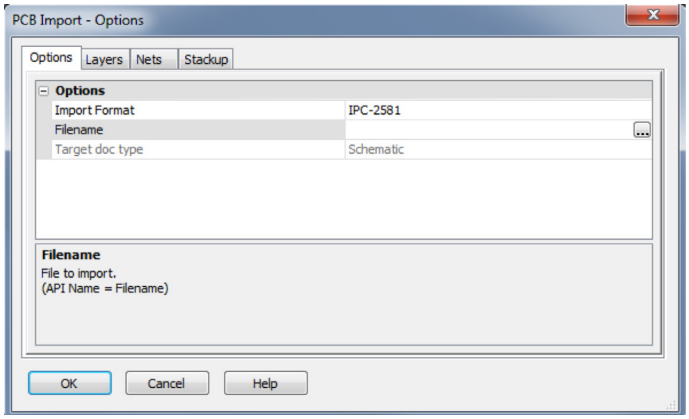

Figure 4: PCB Import wizard

For this application note, open the IPC-2581 demo file *AWR-XFL3010_Through.xml* and select the layers to be imported on the layers tab of the import wizard (Figure 5). The Nets tab (Figure 6) provides an option to import only a subset of selected nets of a project. Select the nets *GND* and *Through*.

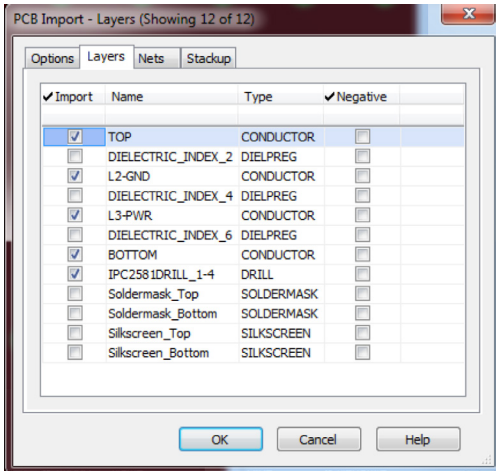

Figure 5: Layers tab of the PCB Import wizard

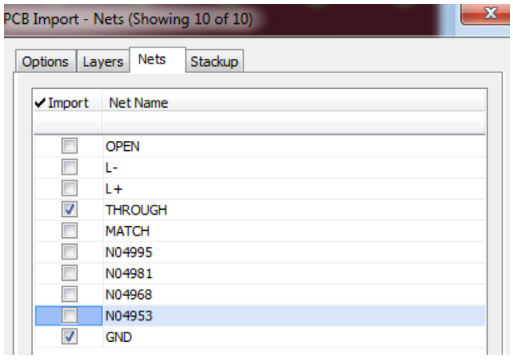

Figure 6: Nets tab of the PCB Import wizard

Step 3: Ready the PCB Layout Data for EM Simulation/Verification

Using the layout editor within the AWR Design Environment platform, the imported file can be reviewed, edited, and prepared for an EM simulation. It is a best practice to review each layer individually and verify for proper import of all metal and via structures. An EM simulation structure can now be created either by selecting all of the imported metal structures or a subsection of the metal structures. In the layout editor, select all metal structures on layer 1 and layer 2, including all vias, and then select *Layout – Copy to EM Structure*.

In the new EM structure dialog box, convert the layout data into an EM simulation structure by selecting the desired EM simulator, for example, *AWR AXIEM - Async*. Set the initialization options to *From StackUp* and select the desired PCB stackup, in this example *SUB1* (Figure 7).

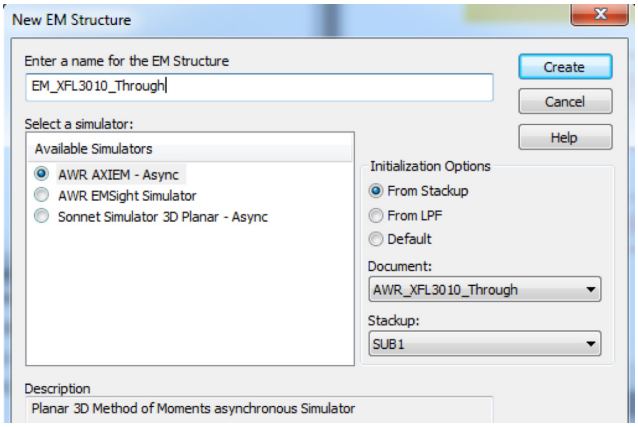

Figure 7: New EM Structure dialog box

Next AWR Microwave Office and AXIEM software will attempt to assign ports automatically and provide an overview list of all possible port connections that were detected (Figure 8).

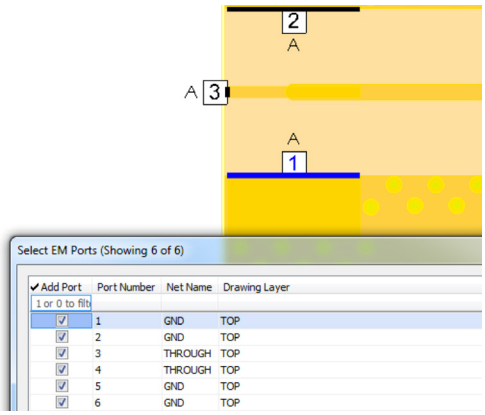

Figure 8: EM Ports overview list

For this example, all ports except the ports connected to the nets Through and GND will be disabled and the port numbers 3 and 4 will be re-labeled to ports 1 and 2, as shown in Figure 9.

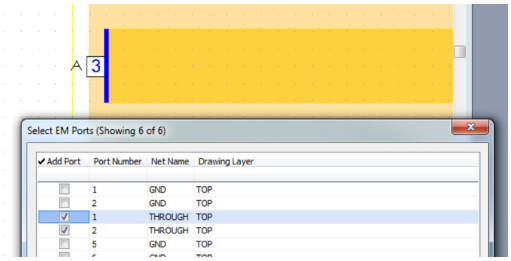

Figure 9: All ports except the ones connected to Through and GND are disabled, ports 3 and 4 are re-labeled to 1 and 2

Select *OK* in the EM ports dialog box to create the EM simulation structure with the pre-defined ports 1 and 2. To open the 3D EM Layout view, select the EM structures in the EM structures folder in the project manager and select *View 3D EM Layout* (Figure 10).

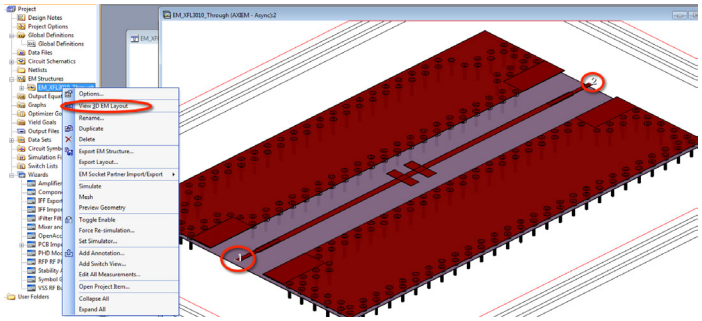

Figure 10: 3D EM Layout view

The original Allegro PCB board file contained four metal layers, but only layers 1 and 2 have been imported into the AWR Design Environment platform. The length of the via that extend below the metal of layer 2 provides an indication that the Allegro layout file has been successfully imported. It should be noted that the PCB layer stack information does not have to be reentered after the IPC-2581-B file is imported, provided that the Allegro PCB Designer cross-section contained all the required PCB stackup data (thickness of each layer, permittivity, conductivity).

The renamed EM port labels 1 and 2 are now correctly displayed in the AWR AXIEM 2D and 3D views and their properties can be verified or edited by first selecting a port in the 2D view, followed by a right mouse click *(RMB) -> Shape Properties* (or double click on the port). The port types will be assigned with the auto property per default.

For this example, the auto property can be left unchanged since the EM simulation is set up as a two-layer board, where layer 2 is a dedicated ground plane. For EM structures that utilize more layers, these port properties must be accurately set to reflect the correct ground reference of each port.

To generate the mesh for this EM structure, first specify the frequency range for the EM simulation. Set the frequency range to 1-6001MHz with 100MHz steps under the options setting of the EM structure in the project manager (Figure 11). Select *Mesh* from the project manager (RMB on the desired EM structure), as shown in Figure 11 (right). This will produce the result shown in Figure 12.

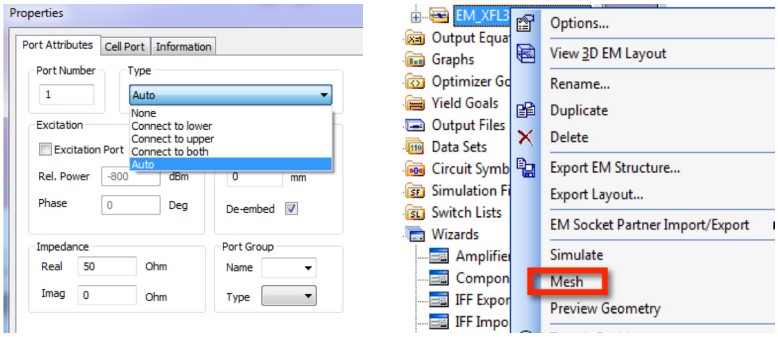

Figure 11: Options setting of the EM structure in the project manager (left) and project manager showing mesh selection (right)

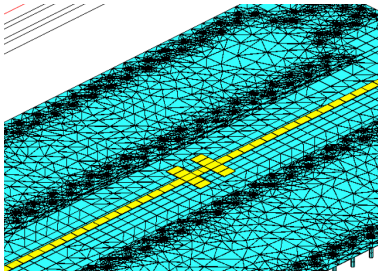

Figure 12: Mesh of the EM structure in AWR AXIEM software

Mesh Complexity and EM Simulation Run Time

The meshed structure (Figure 12) can now be simulated but it will require a significant amount of memory and lengthy run times. While Allegro PCB Designer provides an elegant method to place via arrays around metal structures, traces, and transmission lines to improve shielding between nets and traces, this approach is not friendly to EM simulation/verification. Vias are represented as circular tubes inside of EDA layout software. This representation can present unnecessarily long simulation run times for EM analysis tools. Thus, the de facto approach for EM software is to approximate a via with a polygon. While the number and shape of the vias in the design can be reduced manually, a better approach is to invoke "rules" to simplify the layout and speed up the simulation without sacrificing accuracy.

Step 4: Using Import Rules to Simplify EM Structures

The PCB import wizard that was used to import the IPC-2581-compatible Allegro layout file automatically creates a schematic that contains a *STACKUP option* element (Figure 13) with the PCB properties contained within the Allegro cross-section editor.

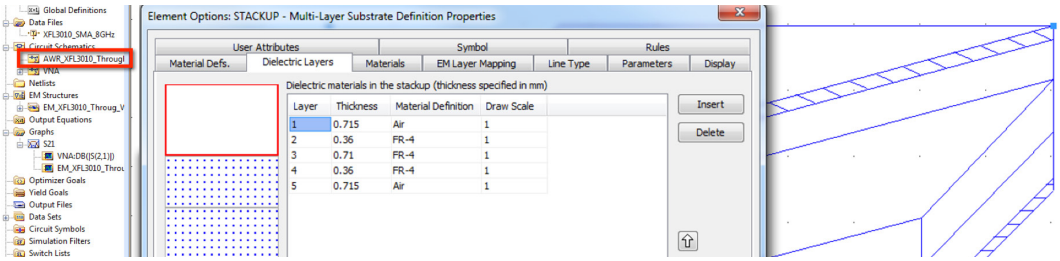

Figure 13: Cadence layout file — STACKUP option element revealing board properties

The dielectric layer tab shows the thickness and material definition of each layer, while the *Materials Defs* lists the detailed material properties that are used in this design.

The rules tab enables the user to specify additional rules that can be applied when the layout is copied to an EM structure within the AWR Design Environment platform. A few example rules are shown below to provide a quick-reference starting point for simplifying the EM structure.

RESHAPE_CIRCLE_DIVS <number-of-edges>

- The *RESHAPE_CIRCLE_DIVS* setting specifies the <number-of-edges> to be used to approximate all circles, either on a particular layer or all layers. For the rule *RESHAPE_CIRCLE_DIVS = 4,* via(s) will be approximate with a square.

RESHAPE_CIRCULAR_ARCS_DIVS <num-divs-on-360>

- The rule *RESHAPE_CIRCLE_ARCS_DIVS = 8* will specify the number of divisions for each 360-degree circle.

MERGE_VIA_RADIUS_MULT <radius-multiple>

- The *MERGE_VIA_RADIUS_MULT* can be used to merge all vias into a solid metal connection (for instance, a metal "wall"), which significantly reduces the complexity of the EM structure.

The use of rules significantly reduces the complexity of the EM structure, as shown in the meshed layout view in Figure 14.

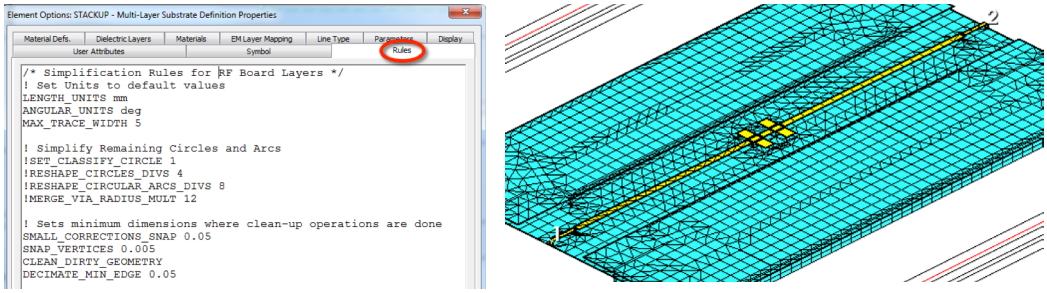

Figure 14: STACKUP options element in Allegro software (left) and meshed graph of the EM structure (right)

Step 5: Simulation vs Measured Data

For this instance of the design, the EM simulation was finished in just a few minutes on a standard Office of Technology Services (OTS) Windows-based PC, since all ground vias were replaced by solid ground metal shapes.

The EM simulation results were then compared against network analyzer measurements and simulation results versus measured data correlation are revealed in Figure 15. Note: In this example, the coax connector/transition was not included in the EM simulation, resulting in slightly different results between simulation and measurement. The AWR Analyst™ simulator could have been used to simulate the response of the 3D coax alongside the response of the PCB structure with transmission line discontinuities.

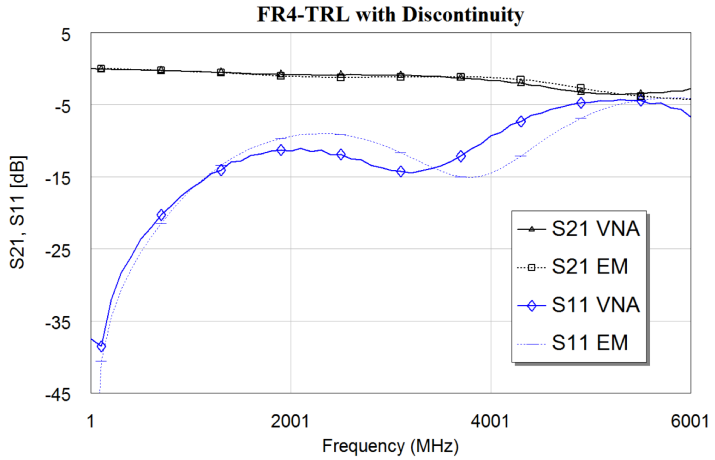

Figure 15: AWR AXIEM EM simulation results versus network analyzer measurements

Conclusion

This application note has presented a step-by-step method for using the EM simulation and verification flow between the Allegro PCB Designer and the AWR Design Environment platform to analyze the performance of a simple PCB, inclusive of a transmission line, two discontinuities, and ground via arrays. The creation of an EM simulation structure has been illustrated, as well as the tradeoffs between design complexity and simulation time. An introduction to basic EM port configuration and simulation settings has been provided and a comparison of the AWR AXIEM EM simulation against measured results has been shown.

Acknowledgment

Special thanks to Oliver Werther of Effective RF Solutions for his contributions to this application note.

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