APPLICATION **NOTE**

cadence®

EM Verification of Complex Board Structures in the AWR Design Environment Platform

This application note presents a streamlined method for verifying complex board structures using the PCB import wizard within the Cadence® AWR Design Environment® platform.

Design Overview

The densely populated, multi-layer PCBs needed for complex functionality in next-generation commercial and military applications require integration of high-speed data lines and RF circuitry. This integration can compromise system performance because of coupling (crosstalk) and other parasitic behavior along the signal traces. As PCBs grow more and more intricate, electromagnetic (EM) analysis is becoming critical for verifying performance and enabling designers to mitigate the effects of parasitic behavior in PCB designs. The PCB import wizard within the AWR Design Environment platform helps designers simplify and accelerate EM analysis of complex PCBs by isolating and characterizing critical traces within complex multi-layer configurations.

PCB Design Example

A Zuken-designed PCB is used as an example to demonstrate how the PCB import wizard works. The board design is imported into AWR® software using the wizard, and then, in order to streamline the EM analysis/verification process, the parts of the board that do not impact the performance are cut out.

Import PCB XML Files

The process begins by selecting the file. The wizard imports XML files using the IPC-2581 standard format developed by the ICP-2581 Consortium for PCB and assembly manufacturing description data and transfer methodology. The wizard also supports 3Di and ODB++ formats. Once the file is selected, all layers, nets, and stackup information that are in the PCB file are directly read by the wizard and imported into AWR software. Designers can specify exactly which layers and nets they want to import (Figure 1). By executing the *Copy to EM Structure* command, the layout is then sent to the EM simulator of choice, in this example the AWR AXIEM® planar EM simulator within the AWR Design Environment platform. Ports can easily be added to the component pins and pads by selecting *Create Ports From PCB Pins*. The wizard then runs the information specified by the designer, imports the file, and produces a layout of the entire board, ready for EM simulation.

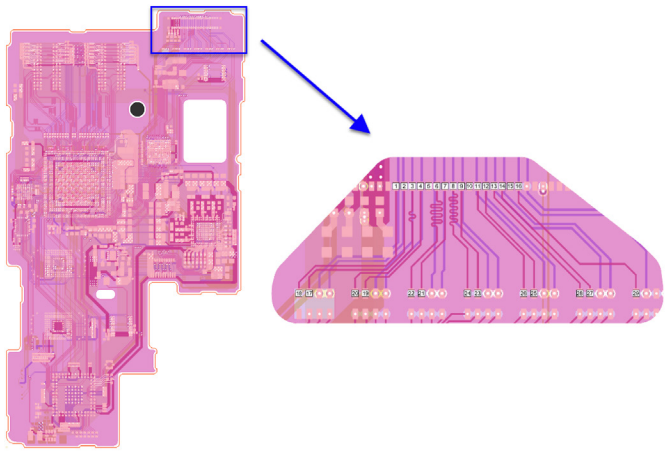

Figure 1: The complete PCB layout (courtesy of Zuken) and the selected region of interest (pop out) for further analysis

Select Layer Visibility Options and Net Routes

Once the board is imported, layer visibility options can be selected to make it easier to see exactly what is to be simulated (Figure 2). The *Select Net Routes* command propagates the selection of nets based on the net names, thereby selecting anything that has the same net names, i.e., the entire trace. For complex PCBs, there are many traces running between pins and so the objective is to use EM simulation on only critical nets on the board, thus saving considerable simulation time. This is accomplished by isolating the area of interest from the rest of the layout.

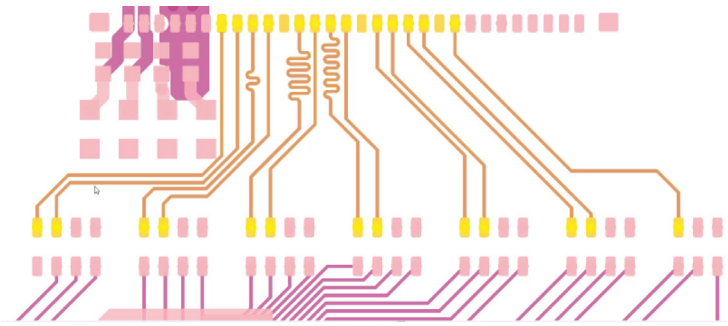

Figure 2: Critical traces set for further analysis

In this design, some of the pins have nets that connect to different ground or power planes at the port. If this is the case, the user has an alternative method of selecting nets that applies further automated intelligence. The PCB EM setup wizard works similarly to the *Select Net Routes* command in that it propagates the selection down nets omitting (not select) shapes that are connected to either power or ground nets.

The EM setup wizard can also propagate net selection through open gaps in the net where (series) surface-mount components would be located. For complicated boards with many components, this capability makes net selection much faster than manually trying to select individual common nets that are interconnecting multiple components.

The wizard also highlights the areas containing the nets selected for EM simulation. The PCB EM setup wizard can be used to confirm visibility of layers and select the kind of cutout style desired, i.e., details of the PCB area surrounding the selected trace(s). The default is a bounding box, but in this case, to avoid selecting areas that are not of interest, which adds unnecessary simulation time, the user can specify a bounding polygon. This feature also allows the user to adjust the distance from the selected trace metals to the edges of the bounding box.

Next, the simulation space can be trimmed to a reasonable size using the *Create EM Clip Region* command, which provides different options for the size and shape of the simulation space. These simplification tools provide users with choices, and the wizard looks at the nets and geometries and offers suggestions based on the geometries. Designers can edit the suggestions or accept them all. The premise here is to enable faster EM simulation without compromising accuracy.

Add Ports

Now that the EM structure exists, ports can be added, and the simulation can be performed. The PCB EM setup wizard assists with this task as well. The pins of interest have already been selected, and rather than repeating, they can be restored in the EM structure through the wizard. Once the simulation is done, it is easy to bring the results into a schematic and wire up components that automatically show up on the subcircuit and schematic. Even better, it is easy to create custom symbols based on the layout of the PCB EM structure so that is easy to visually know what port is where in the layout. In just a minute or two, it is possible to import a PCB design into the AWR Design Environment platform, intelligently trim down the problem to the region of interest, get it ready for EM simulation, hook up the surface-mount components in a schematic, and look at the performance. A simplified diagram of the available design flow for EM verification of PCB layouts from third-party computer-aided design (CAD) tools is shown in Figure 3.

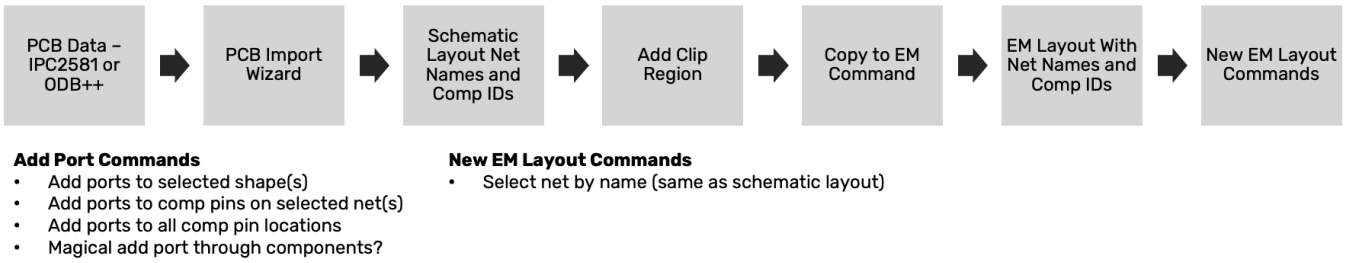

Figure 3: Design flows for EM verification of PCB layouts from third-party CAD tools

For this structure, the resulting mesh is around 20,000 unknowns (Figure 4). With the use of the wizard, the mesh and resulting unknowns are reduced, significantly shortening simulation time so results are obtained more quickly—without losing accuracy.

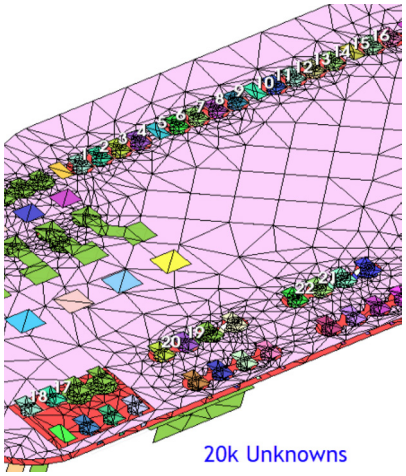

Figure 4: Shape simplification reduces the number of unknowns in the mesh, thereby reducing simulation time

Structure in Circuit Schematic

When the simulation is complete, and the EM structure is viewed within a circuit schematic, it is then ready to analyze further and connect components across the board. Component pin names are indicated in the schematic, so each pin is easily identified. In addition, custom symbols that match the layout of the structure can be created to ensure that components are connected correctly (Figure 5).

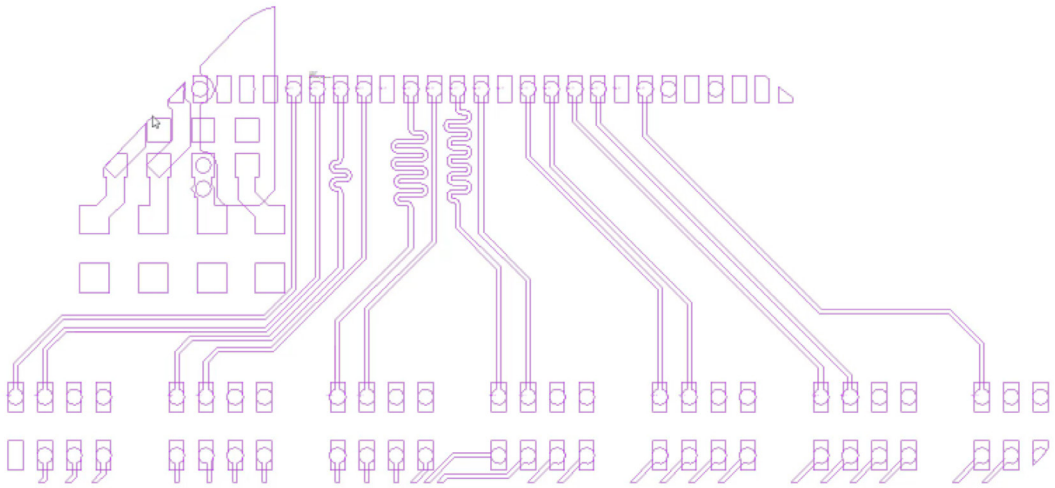

Figure 5: Custom schematic symbol for the select region of the PCB

Conclusion

The example presented in this application example showcases the powerful capabilities in theAWR Design Environment platform's PCB EM import wizard that help designers streamline the EM verification process for complex multi-layer PCBs. Designers can now select and import a PCB file and run a full EM simulation using a simple and automated process that significantly cuts simulation time without compromising accuracy.

Acknowledgment

Special thanks to Zuken for providing sample PCB files from which to develop this application example.