AWR Design Magazine

Vol.19.4

cadence®

AWR Is Now Cadence

AWR Corporation has been purchased from National Instruments by Cadence Design Systems in order to expand Cadence's reach into 5G RF communications for the aerospace/defense, automotive, and wireless market segments. While Cadence has industry-leading expertise in chip design and IP, AWR fills in gaps with design tools for millimeter-wave (mmWave) and microwave products at the board and system level, as well as in III-V semiconductor designs, which outperform silicon in high-frequency devices.

The foundations of the combined product lines will be Cadence's Virtuoso layout software for analog, digital, and mixed-signal design and Allegro for packaged circuit design.

Cadence has also entered into a strategic alliance with NI to serve mutual customers in the communications sector by tightly connecting its software with NI LabVIEW and PXI modular instrumentation systems and semiconductor data platform.

"By joining forces with Cadence, our goal is to be able to leverage the strength and heritage of the Virtuoso and Allegro platforms along with the AWR Design Environment platform to deliver complete solutions for complex ICs, packages, and boards."

Dr. Joseph E. Pekarek, Former GM of AWR Group, NI

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MITSUBISHI ELECTRIC

"AWR software provided us with immense benefits for early development of our new 5G PA."

-Keigo Nakatani, Yutaro Yamaguchi, Yuji Komatsuzaki, and Shintaro Shinjo

High-Efficiency 5G PA

Mitsubishi Electric is one of the world's leading names in the manufacture and sales of electrical and electronic products and systems used in a broad range of fields and applications.

Challenge

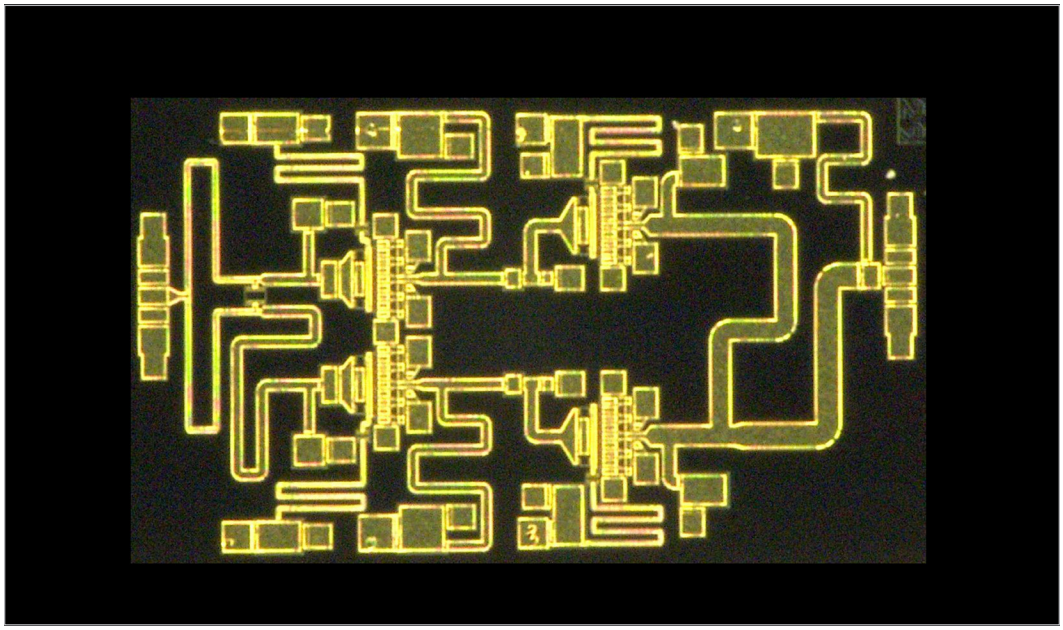
The Ka band is a popular frequency for mmWave applications for 5G. High efficiency and high output power amplifiers (PAs) are required to reduce power consumption and increase data transmission distance. Mitsubishi Electric engineers were challenged to meet the requirements for a PA with high output power and high efficiency at backoff output power by designing a 28-GHz PA monolithic microwave integrated circuit (MMIC) using a high-efficiency Doherty architecture.

Solution

The designers chose AWR Design Environment software for this exacting design and believe that the resulting Doherty PA device is the state of the art in 5G amplifier devices for the Ka band.

The parameters of the Doherty output combiner, which consisted of microstrip lines and metal-insulator-metal (MIM) capacitors on a 50-µm thickness silicon carbide (SiC) substrate, were calculated using Microwave Office circuit design software. Electromagnetic (EM) simulations were performed on the Doherty output combiner using the AXIEM planar EM simulator. The fabricated 2-stage Doherty PA using a gallium nitride (GaN) high electron mobility transistor (HEMT) achieved a measured saturation output power of 35.6 dBm (3.6 W) and peak power-added efficiency (PAE) of 26%. PAE of 23% and 20% was obtained at 6 dB and 8 dB backoff, respectively.

To read the full story, visit awr.com/customer-stories/mitsubishi-electric-5g-pa



Photograph of the GaN Doherty amplifier MMIC.

K-Band Satcom MMIC PA

Arralis, headquartered in Limerick, Ireland, is a rapidly scaling technology company providing industry-leading expertise in RF, microwave, and mmWave technology.

Challenge

K/Ka-band satellite communications (satcom) systems can provide constant, uninterrupted access to information, driving companies to invest heavily in this spectrum for global broadband services. These systems are enabled through high-power amplifiers (HPAs), which form the final link in the RF power chain of next-generation, satellite-based, RF front-end components. Arralis has developed the Leonis chipset to address the growing demand for lower cost K/Ka-band satellite equipment. The chipset includes IQ and sub-harmonic mixers, upconverter and downconverter core chips, switches, phase shifters, low-noise amplifiers (LNAs), and PAs.

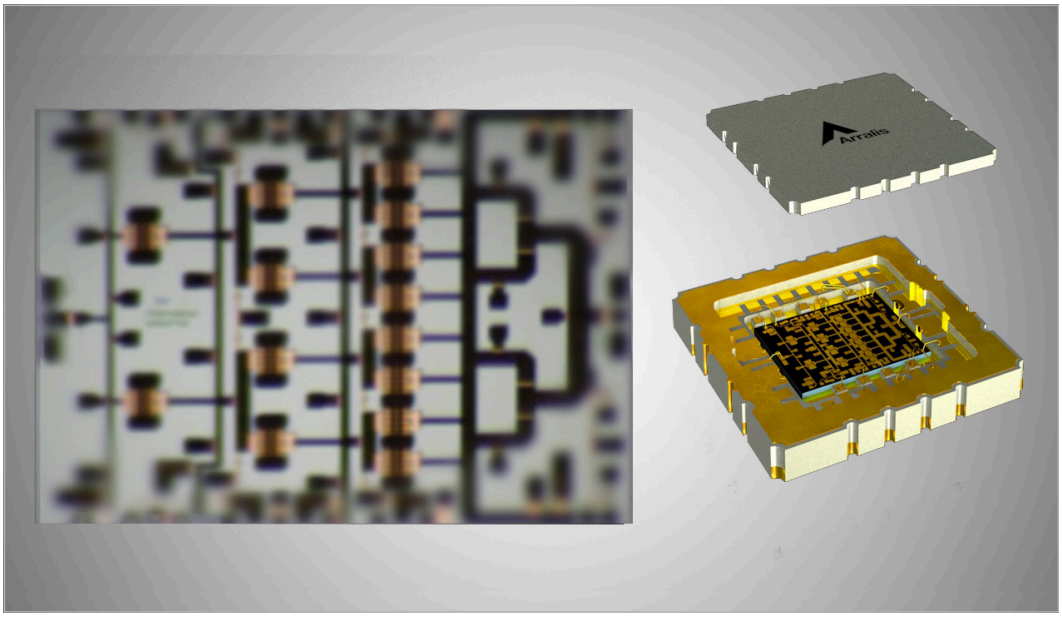
Solution

During the design phase, extensive circuit design and simulation was performed using the AWR Design Environment platform, specifically Microwave Office circuit design software, the AXIEM EM simulator for 3D planar structures (MMIC manifold feed network, on-chip passives, and evaluation board), and the Analyst™ EM simulator for 3D EM analysis of the package. Arralis designers used the simulation software to work with the active and passive MMIC component models developed by the foundry and organized into process design kits (PDKs) developed through collaboration between the AWR and UMS modeling teams.

To read the full story, visit awr.com/customer-stories/arralis

"AWR software enabled us to work with active and passive MMIC component models developed by the foundry to design and optimize the Arralis HPA."

-Thomas Young



Proposed packaging (Kyocera SGMR-B1193) for K-band HPA. Image courtesy of Kyocera Corporation.

Power Amplifier Designers Tackle High Peak-to-Average Power Ratio With Digital Predistortion

Targets for 5G New Radio (NR) require the use of cyclic-prefix orthogonal frequency-division multiplexing (CP-OFDM) waveforms, as well as inter- and intra-band carrier aggregation (CA), to enhance spectral efficiency, especially for the crowded sub-6 GHz bands. The high spectral efficiency and wide bandwidths in communication systems employing these techniques can result in signals with high peak-to-average power ratio (PAPR), which creates challenges for PA designers struggling to simultaneously meet bandwidth, linearity, and efficiency requirements.

In addition to linearity, high PAE is needed to reduce power consumption in order to extend mobile device battery life and reduce base station operating expenses. Designers are also challenged to maintain high PAE while at the same time achieving low signal distortion under high PAPR.

Addressing the Design Challenge

Different PA design strategies can be employed to improve linearity and efficiency performance, including the use of different architectures. Visual System Simulator™ (VSS) system simulation software can be used to understand the impact on PA performance due to CA and different modulation schemes (Figure 1).

VSS system design software, along with Microwave Office circuit design software, provides designers with simulation tools from which to develop front-end components, including PAs employing different linearization technologies. VSS and Microwave Office software tools together allow designers to pursue optimum linearity and efficiency for a comprehensive PA characterization and design flow, integrated with custom digital predistortion (DPD) solutions.

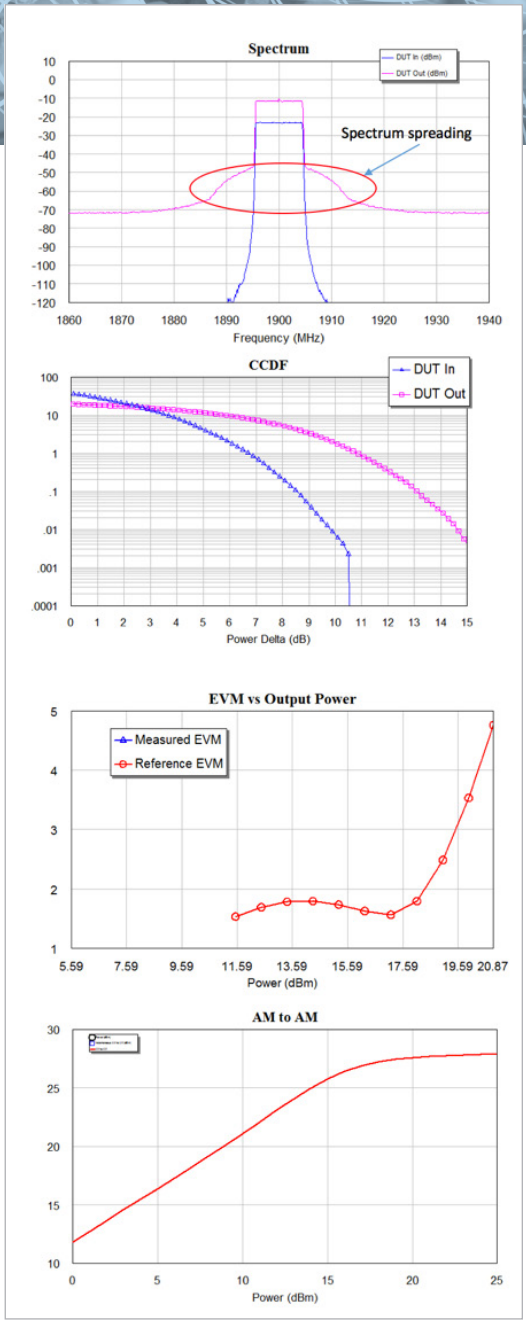


Figure 1: Various aspects of signal distortion and impact on the system arising from nonlinearities.

Lookup Table Example

It is important for designers to understand the nature of the signal distortion introduced by the amplifier in order to implement a sufficient DPD solution. They must select an accurate (behavioral) model structure that can best represent the nonlinearity and memory effects to implement the appropriate predistortion. PA baseband behavioral models can be classified in three categories:

- Memoryless models
- Models with linear memory
- Models with nonlinear memory

Memoryless models assume that the instantaneous output signal depends only on the instantaneous input signal of the amplifier. These models are based on the quasi-static AM/AM and AM/PM properties of the PA. Various memoryless models have been proposed in the literature, including the power series or polynomial model and the lookup table (LUT) mode. VSS software supports several DPD algorithms, (inclusive of a commercially available NanoSemi model), however for purposes of this article, the focus will be on a LUT DPD example.

The VSS predistort network example project, Predistort_Network, is a practical example that shows how to use the software to construct a DPD system for reducing spectral regrowth at the output of an amplifier. This project uses an LUT-based DPD constructed from the AM/AM and AM/PM characteristics of the amplifier, which in this case was simulated with Microwave Office software in situ at the transistor level through co-simulation with VSS.

The AM/AM and AM/PM of the PA graph plots the large-signal transfer characteristics of the project amplifier, calculated by VSS measurements using the PA characterization test bench driving the AMP_1900 PA defined in the Microwave Office circuit schematic (Figure 2).

The VSS example project also contains a script that automates LUT coefficient generation by automating the AM/AM and AM/PM measurements, calculating the LUT coefficients, storing them in the data file, and then restarting the simulation with the updated coefficients.

Designers can thereby insert a new Microwave Office PA design in place of the default one and implement a new LUT predistorter for their own particular device.

Conclusion

5G NR is driving the trend of enhancing data rates and capacity through the use of spectrally efficient modulation waveforms and CA, resulting in high PAPR and wider bandwidths. To maintain higher efficiency, PA designers must adopt advanced linearization techniques that enable the amplifier active device to operate closer to saturation. Microwave Office circuit simulation software specializes in PA analysis and works directly with VSS system simulation software to quantify the linearity measurements such as complementary cumulative distribution (CCDF), error-vector magnitude (EVM), and adjacent channel power ratio (ACPR) that are essential in meeting these emerging technical challenges.

The examples mentioned in this article are available for download at the URL address listed in the references and work with an active license of VSS software. Software evaluations are available at awr.com/tryawr.

By David Vye
Technical Marketing

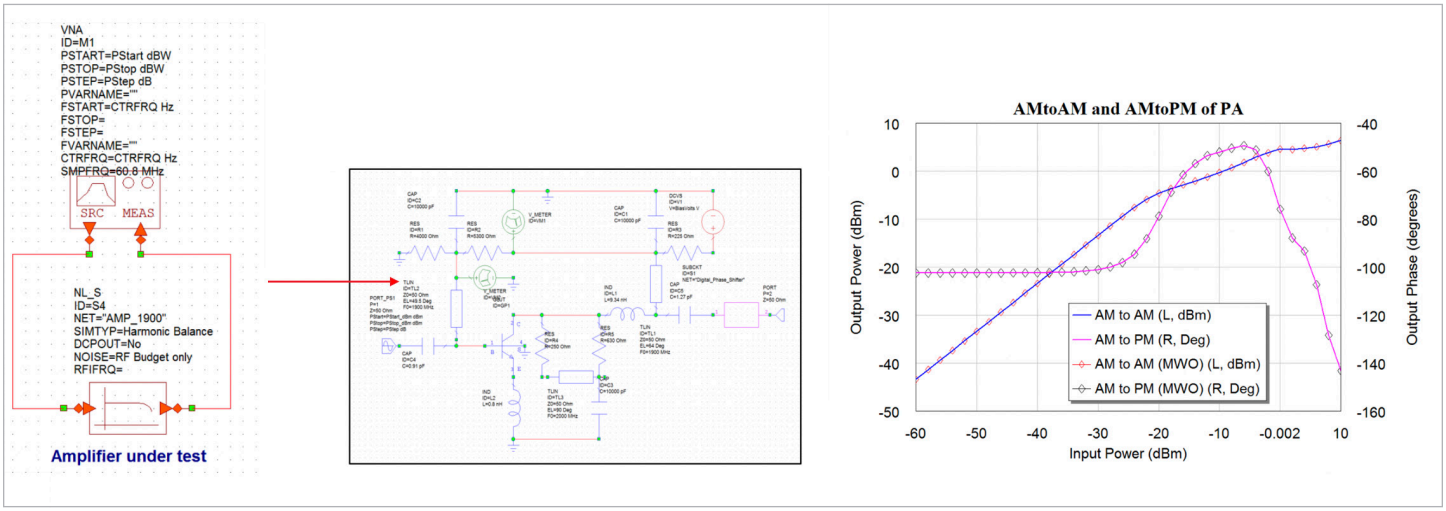


Figure 2: VSS PA characterization test bench driving the AMP_1900 Microwave Office circuit schematic to generate AM/AM and AM/PM PA characterization data for the LUT.

Best Practices for Efficient and Effective Planar EM Simulation

Designers of today's complex, multi-featured communications products require accurate and fast EM simulation to deliver cost-effective, high performance products to market in ever-shrinking windows of opportunity.

The AXIEM 3D planar method-of-moments (MoM) EM analysis simulator within the AWR Design Environment portfolio delivers the accuracy, capacity, and speed designers need to characterize and optimize passive components on RF printed-circuit boards (PCBs), modules, low-temperature co-fired ceramics (LTCCs), monolithic microwave integrated circuits (MMICs), RFICs, and antennas.

This eBook presents 10 best practice tips for using the AXIEM simulator that will help designers effectively and efficiently use the software to overcome the most commonly encountered issues when running EM simulations. The tips address four main design areas: ports, EM environment, meshing, and simulation. A list of helpful references is provided at the end of the eBook for interested readers to find more detailed information.

Ports

The AXIEM simulator has many port options, which differ based on their grounding type, their ability to be de-embedded, and their grouping with other ports for mutual de-embedding schemes.

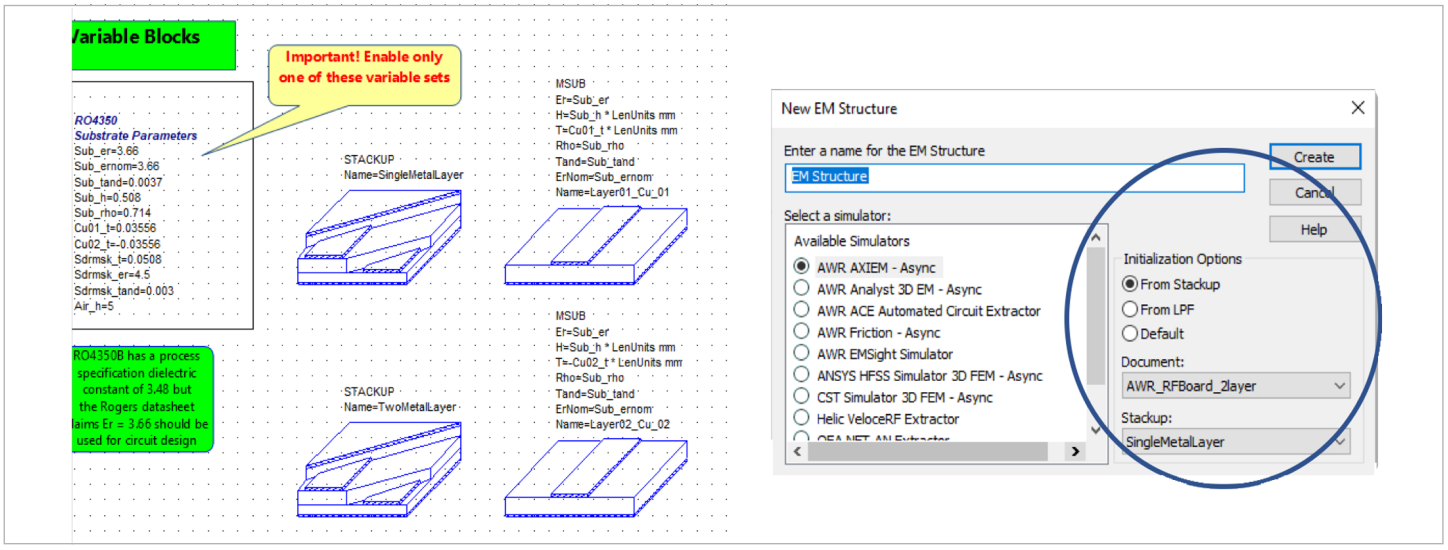
Best Practice Tip #1: Use the AXIEM autoports feature, which will usually choose a reasonable port ground reference by considering potential ground planes and nearby metal.

EM Environment

A STACKUP block should be used when EM projects are created in Microwave Office circuit design software.

Best Practice Tip #2: Understand how EM layer definitions work in the STACKUP block.

Best Practice Tip #3: Use parameters to control shapes in the drawing environment. Either shape modifiers, which work directly on the polygons, or parameterized cells (PCells), which are pre-defined shapes controlled with parameters, can be used.



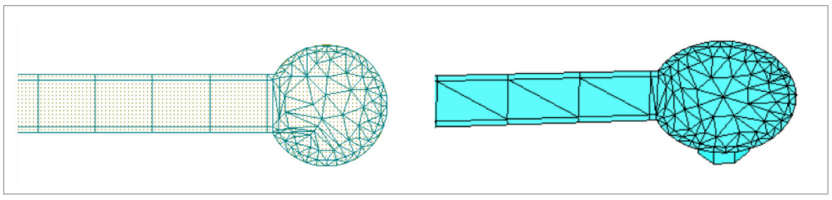
Two different STACKUP blocks on a global definitions page (left) and STACKUP block creation in a new EM project (right).

Best Practice Tip #4: Use geometry simplification rules to simplify the layout before it is meshed. Complicated polygons are simplified, and unnecessary layout details are removed, resulting in a faster simulation.

Meshing

The AXIEM simulator, or any other EM simulator, is only as good as its mesh. There are several ways to obtain a reasonable mesh, by which is meant one of reasonable size with well-formed triangles and rectangles.

Best Practice Tip #5: Understand how the mesh is set. The minimum facet size and mesh density can be controlled in a variety of ways.



2D view (left) and 3D view (right) of an edge mesh on a line and via.

Best Practice Tip #6: Understand the issues regarding thick versus infinitely-thin metal. The mesh count is lower for non-zero thickness metal, but accuracy can be affected.

Simulation

The AXIEM simulator produces S-parameters, which can be viewed in a graph or used in a circuit simulation. The designer places the S-parameters into the schematic as a subcircuit and the resulting circuit is then simulated using a circuit simulator, most typically harmonic balance (HB), although a time-domain simulator will have the same issues as HB.

Best Practice Tip #7: When results from the AXIEM simulator are used in nonlinear circuit simulations, make sure a DC simulation and enough harmonic frequency simulations are included in the answer.

The AXIEM simulator is usually set to run over a frequency range. The designer sets the number of frequencies so that the results can be accurately interpolated to any frequency in the specified range.

Best Practice Tip #8: Understand how frequency interpolation works in the AXIEM simulator. Advanced frequency sweeping (AFS) can be configured to reduce the number of required simulation frequencies while maintaining a specified accuracy over the frequency range.

The designer has control over how the AXIEM simulator uses resources on the computer and can even use computers on remote machines.

Best Practice Tip #9: The AXIEM simulator can be set to use various available computer resources. Understand how to set the number of cores, simulation priority, and remote simulation options, if available.

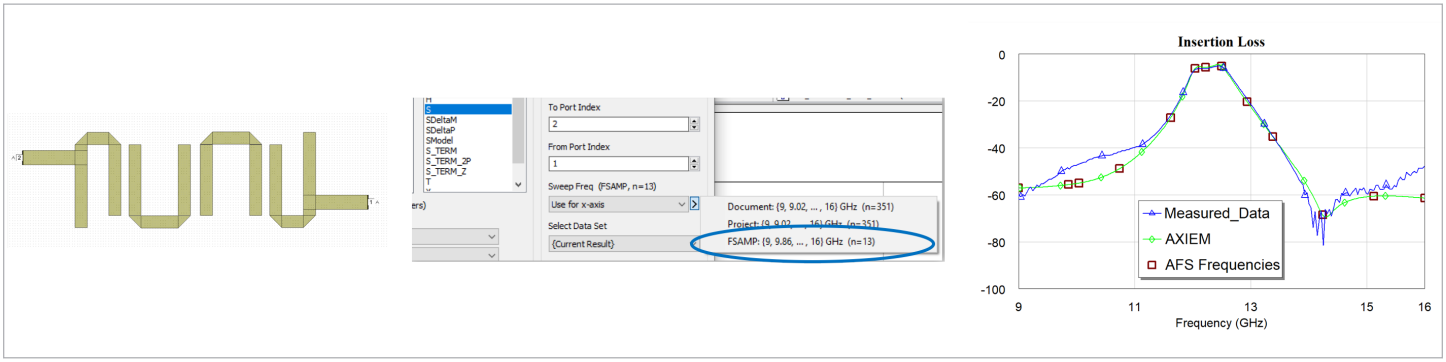
There are two quick measurements, passivity and energy conservation (or the sum of powers) that can be used on any S-parameter file. They will not tell the designer if an answer is correct, but they can indicate if there are problems or at least if the answer makes some physical sense.

Best Practice Tip #10: Check results with the passivity and energy measurements.

Conclusion

The AXIEM EM simulator is a key design tool for engineers addressing the passive structures, transmission lines, large planar antennas, and patch arrays that comprise today's complex 5G communications products and IoT and automotive smart devices. Designers of RF components rely on AXIEM software to meet the challenging goals for next-generation products and successfully bring products to market.

This eBook addresses many of the design problems advanced AXIEM users encounter and provides 10 key best practice tips for overcoming these issues and efficiently bringing their products to market.



Hairpin filter on a PC board and menu and graph showing FSAMP frequencies used by AFS.

RichardsonRFPD
An Arrow Company

"The stability analysis and optimization features of AWR software are powerful and efficient in yielding the desired results. Network synthesis and iFilter wizards enabled a fast turnaround time between simulation and bench testing."

-Elias Ghafari

Automotive SDARS Design Challenges

Richardson RFPD, an Arrow Company, is a specialized electronic component distributor providing design engineers with deep technical expertise and localized global design support for the latest new products from the world's leading suppliers of RF, wireless, internet of things (IoT), and power technologies.

Challenge

The need to add new antenna elements to a vehicle rooftop antenna module to keep up with customer demand for in-vehicle information/entertainment is increasing. Crosstalk (coupling) between those antenna elements within the module is one of the most critical and challenging issues that antenna engineers are faced with and struggle to overcome.

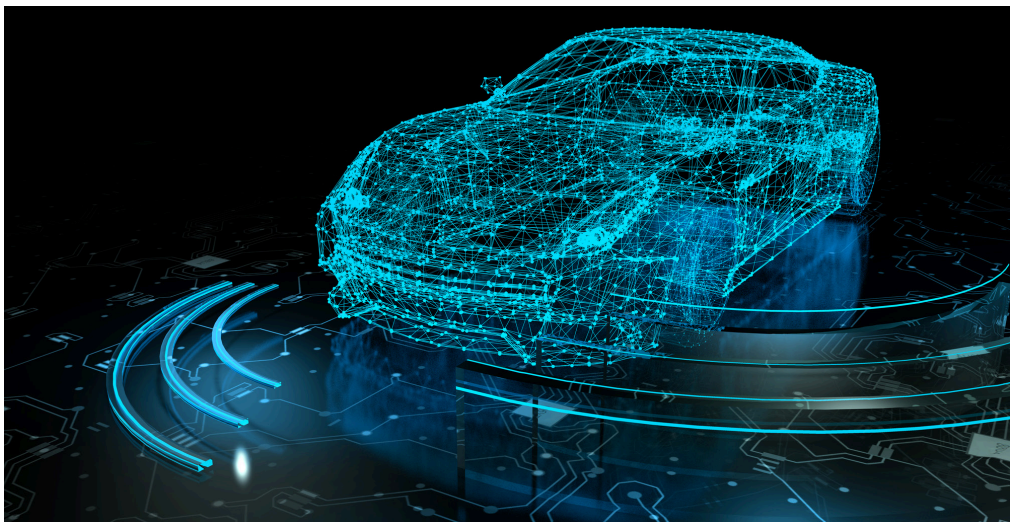
This crosstalk between the antenna elements results in leakage of unwanted signals, which are picked up by an antenna. A specific example is the influence of the cellular antenna element, which causes interference, overloading, and added noise in the LNAs of the rest of the antenna elements.

Richardson Electronics designers were tasked with developing a robust LNA lineup for a satellite digital audio radio service (SDARS) antenna that has higher immunity to external interfering signals. The LNA lineup was for the SDARS antenna designed for multiband antennas for rooftop automotive applications, , which must fit in a very small footprint to satisfy automotive market requirements.

Solution

The designers used AWR software, specifically Microwave Office circuit design software, inclusive of the network synthesis wizard and iFilter™ integrated filter synthesis wizard, to simulate the complete LNA circuit.

To read the full story, visit awr.com/customer-stories/richardson-rfpd



Phased Arrays for Radio Astronomy Applications

Divisions of the National Institute for Astro Physics of the Institute of Radio Astronomy (INAF-IRA) and the Cagliari Astronomical Observatory conduct research into the physics of radio sources such as active galactic nucleus (AGN) and galaxies, clusters of galaxies, the galaxy stars and star formation, and cosmology.

Challenge

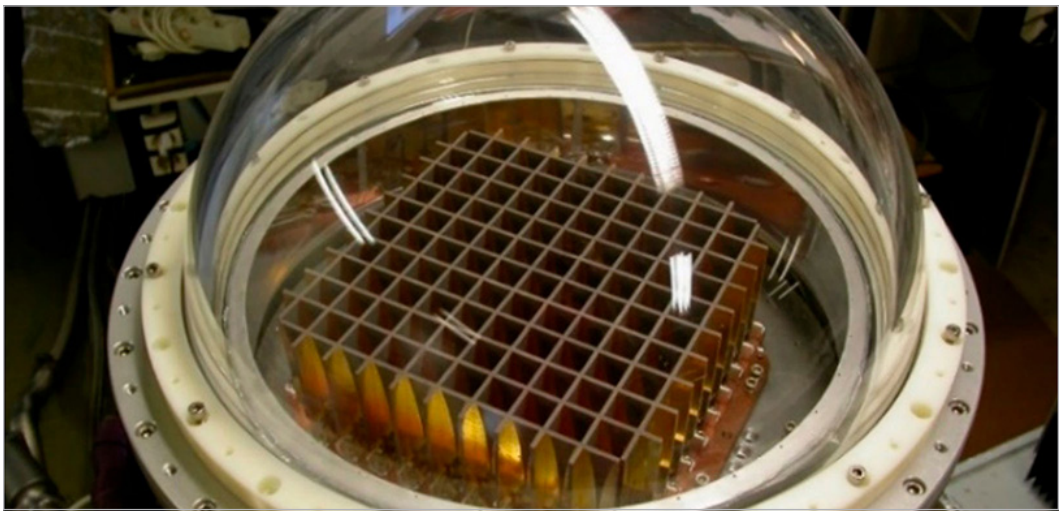
High-sensitivity, large-scale surveys are an essential tool for new discoveries in radio astronomy. INAF designers were challenged to develop, fabricate, and test a room temperature, multi-channel heterodyne receiver operating across the 2.3–8.2 GHz RF band for radio astronomy applications. A phased-array feed placed at the focal plane of an antenna can increase the field of view and mapping efficiency by fully sampling the sky. The new upgraded version, PHAROS 2, utilizes new components to reduce the system noise temperature, enhance the aperture efficiency, and digitize the signals from a sub-array of 24 single-polarization PAF antenna elements that synthesize four independent single polarization beams.

The wide bandwidth and high-performance receiver requirements call for precise electrical modeling of the individual components and RF characterization of the multi-layer printed-circuit board (PCB) substrate in order to achieve the accurate simulation results necessary for successful design.

Solution

INAF-IRA designers used the Microwave Office to design the PCB circuitry of the receiver chains. AXIEM software was used to simulate the EM response of all interconnecting transmission lines and distributed bandpass filters (BPFs). Microwave Office was employed to optimize the overall performance of the entire receiver chain of a PCB populated with surface-mount technology (SMT) components.

To read the full story, visit awr.com/customer-stories/inaf.



PHAROS 2 focal plane array and dome-shaped vacuum window attached to the cryostat.

"The test results for our 32-channel receivers performed well and according to specification. Our success is due in part to AWR software for the design and EM verification of the filters and splitters in the antenna PCBs."

Scalambra Alessandro and Navarrini Alessandro

Solid-State Transmit/Receive Module Design and Modeling for Radar Applications

Transmit/receive (T/R) modules are at the heart of all radar systems employing beam-steering phased-array antennas. These active phased-array radars (APARs) typically require solid-state T/R modules with high-output power, low-noise figure (NF), high third-order intercept (TOI), and sufficient gain in order to function properly. Since the T/R module is 40-60% of the overall RF front-end cost, it is imperative to use an architecture that meets all requirements with the most cost-effective technology, such as monolithic MMICs, and a minimal bill of materials (BOM). This article overviews various solid-state semiconductor technologies for T/R module development and describes a design methodology that includes the modeling/analysis of a T/R module. A basic functional block diagram of a simple T/R module structure is shown in Figure 1.

This article examines several design challenges, including the impact of architecture selection, determination of performance parameters, and methods for modeling the individual module components at the behavioral level for reliable system simulation. Three T/R module architectures are analyzed to highlight the tradeoffs that must be made between different performance parameters. Tradeoffs for an optimal architecture for a given set of requirements will be considered. The proposed T/R module architectures are based on commercial off-the-shelf (COTS) components suitable for X-band and Ku-band applications. Modeling and analysis of the T/R module is performed using VSS system design software.

Solid-State T/R Module Technologies

Solid-state T/R modules are critical elements in active-passive antennas (APAs) used in radar and electronic warfare (EW) applications. Popular RF semiconductor processes include gallium arsenide (GaAs), Si, silicon germanium (SiGe), GaN, and indium phosphide (InP). Among the many suitable semiconductor technologies, modules using GaAs MMICs, developed to serve commercial mobile communication markets, have been in mass production for some time.

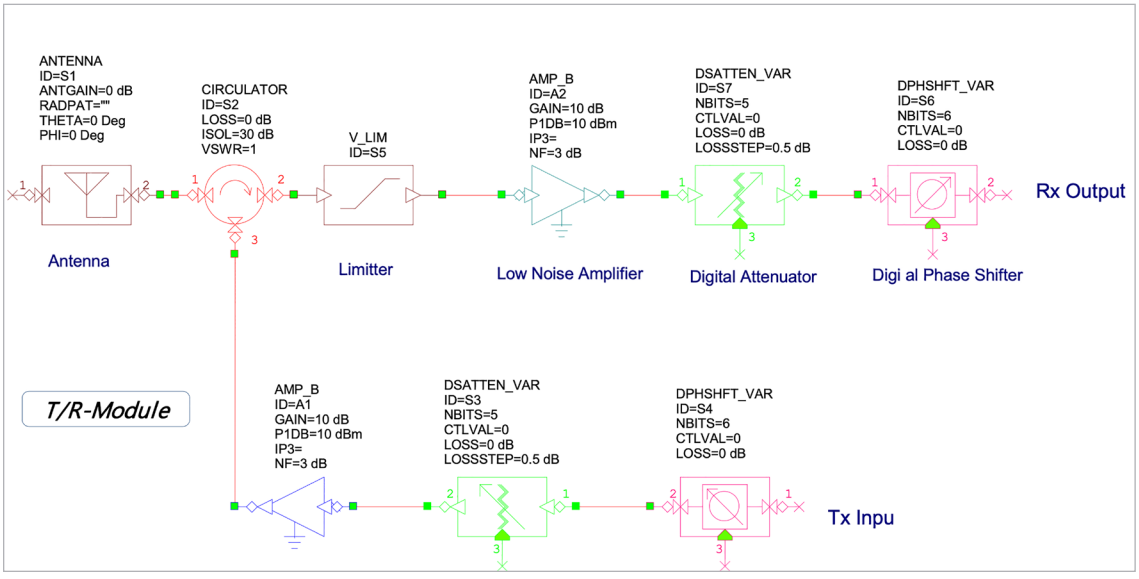


Figure 1: T/R module block diagram.

To fulfill future demands for power, bandwidth, robustness, weight, multifunctional sensor capability, and overall sensor cost, emerging semiconductor and packaging technologies are being implemented with the next generation of T/R modules, including GaN MMICs for high-power amplifiers (HPAs) and robust LNAs. Higher integration at the amplitude and phase control blocks is being realized with GaAs core chips and/or SiGe multifunction MMICs and RFICs.

The choice of a particular process is based on the required performance parameters of the module and type of functionalities being considered for the implementation.

There are numerous technical issues involved in developing T/R modules, including:

- Understanding of IC fabrication technology such as GaN and LTCC/SiP process technology for multi-chip integration and miniaturization
- Precise control of amplitude and phase, achieving high-dynamic range
- Providing sufficient T/R path isolation
- Power handling capabilities of available passive and active surface mount devices
- Thermal dissipation issues
- Packaging and assembly considerations
- Meeting compact size requirements

T/R Module Modeling and Simulation

By providing designers with the means to define a virtual prototype for analysis and design optimization, system-level computer-aided design (CAD) tools play a critical role in addressing the technical concerns above. Individual component blocks, represented by models that capture their expected electrical performance, can be configured into various architectures to determine the component values and arrangements for optimum performance. By using high-level behavioral models, designers can easily perform RF link budget analysis, adding greater component performance details as they become available.

Three possible T/R module architectures are described in this application and the optimal choice depends on the requirements of the particular antenna system. The first architecture features completely separate transmit and receive chains, the second shares several components between the transmit and receive chains, and the third, called the common-leg approach, shares major functional groups between the transmit and receive chains. With a requirement of constant receive gain, there are some obvious differences in NF and TOI performance, as well as in module and antenna complexity. Each of the architectures studied has advantages and disadvantages, which will be weighed against different applications. Figure 2 presents the simulation results for all three architectures.

Conclusion

Three T/R module architectures have been presented in this article, each having advantages and disadvantages depending upon the application. The modeling and analysis capabilities in VSS system design software provided simulation results that enabled detailed parameter versus performance tradeoffs between the different architectures, including a cascaded RF budget measurement for gain, cascaded NF, cascaded TOI, and cascaded intermodulation distortion (IMD).

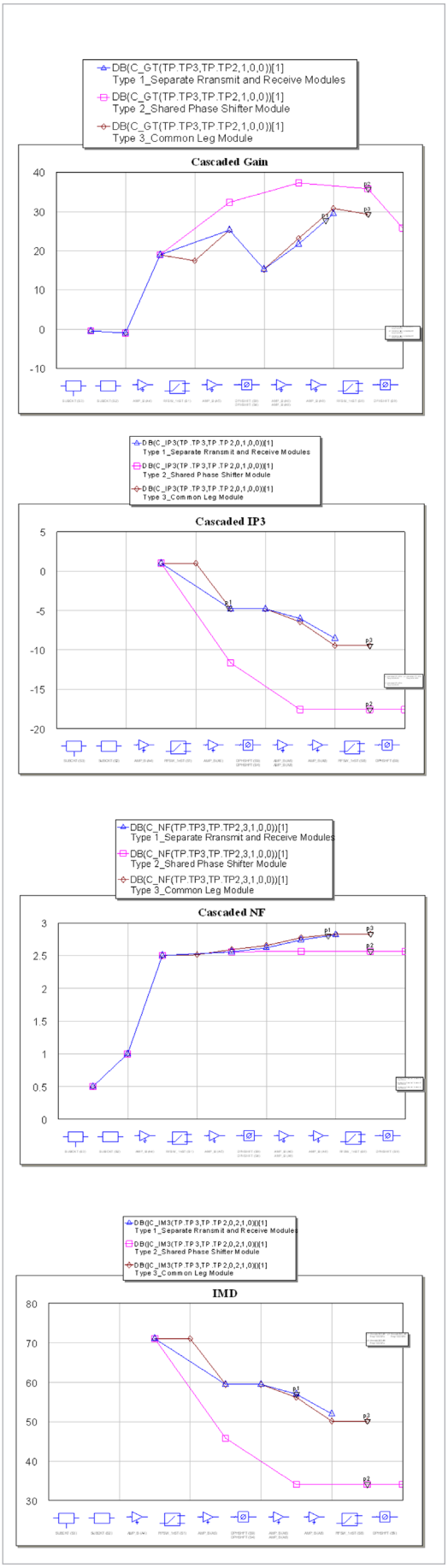
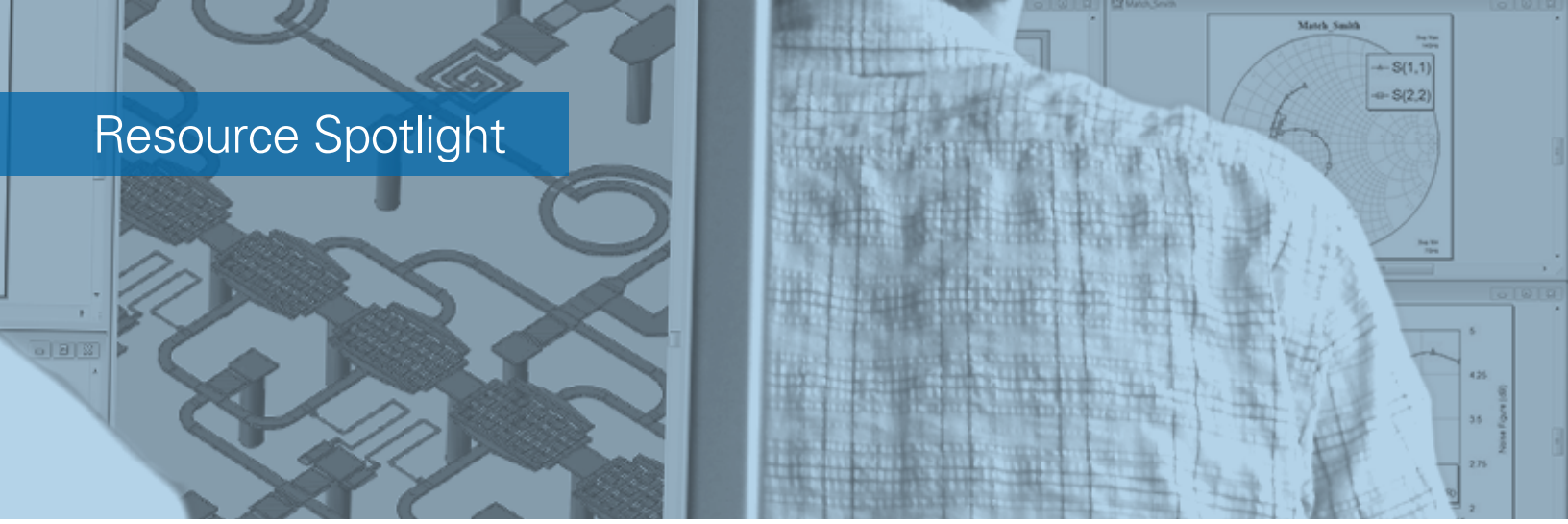


Figure 2: Simulation results for all three architectures.



Resource Spotlight

Resource Library

The resource library on awr.com is a dedicated and searchable landing page for technical content on AWR software products, and solutions. Recent additions to the resource library include:

Webinars

- Instability in Wide Bandwidth High-Power Amplifiers

White Papers/eBooks

- Design of a T/R Module for Radar Applications
- eBook: 10 tips for Fast & Accurate EM Simulation
- eBook: X-Band Push-Push Oscillator Simulation
- eBook: Practical Antenna Design
- Textbook: RF/Microwave Circuit Design (Chinese language)

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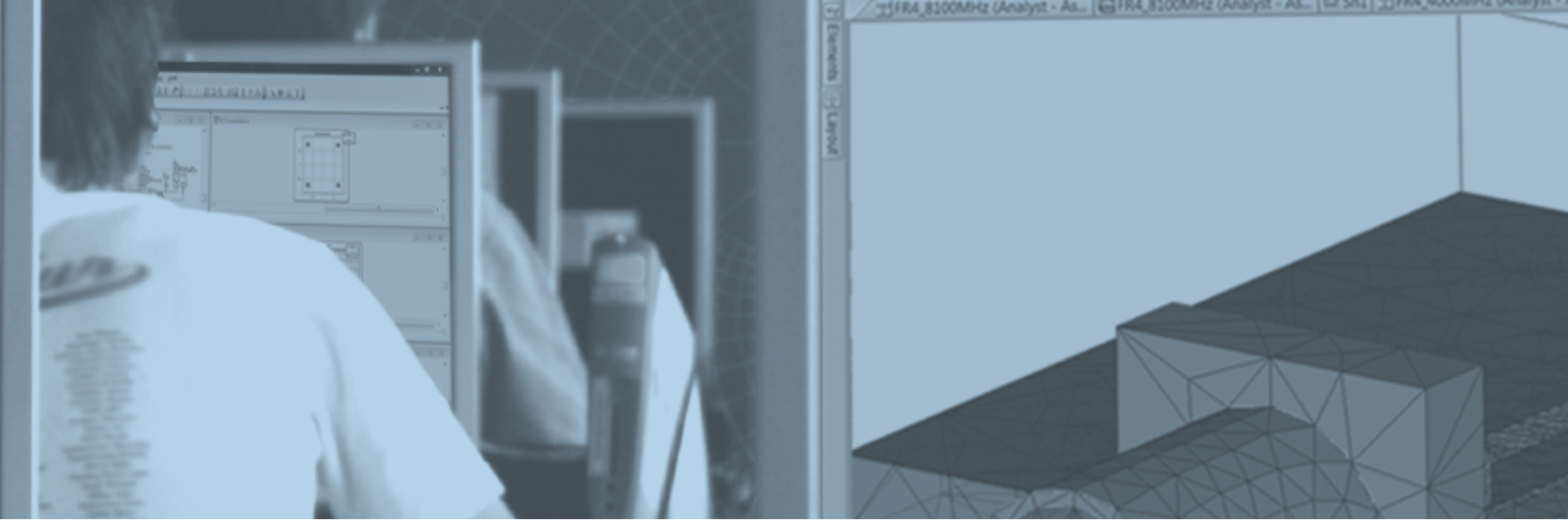

E-Learning Portal: VSS RF Link Budget Analysis

This four-part AWR software e-learning video series demonstrates how to use VSS system simulation software and its impedance-mismatch aware, linear, and nonlinear RF/microwave behavioral models to perform budget analysis. These design tools are useful for system architecture development and RF component specification for communications system design.

The tutorials demonstrate how to build a basic RF chain, define the characteristics of amplifier, filter, and mixer components using behavioral models based on parameter-defined, data file, and subcircuit implementations, perform budget analysis, including cascaded NF, IP3, 1 dB compression point (P1dB), and more, and use spectral analysis to simulate spurious tones due to device nonlinearities. In the final video a modulated signal from the VSS library is passed through the RF link, demonstrating the ability of VSS to run concurrent time- and frequency-domain analyses.

- **Part 1 –** demonstrates how to build a basic RF link in VSS using a behavioral filter model and how to replace it with an actual circuit model derived from Microwave Office circuit design software and the iFilter™ filter synthesis wizard
- **Part 2 –** demonstrates how to model a filter with the VSS behavioral filter model
- **Part 3 –** demonstrates how to model a mixer with the VSS powerful and intelligent mixer model
- **Part 4 –** shows a modulated signal passing through an RF link path and system metrics in the time domain like the eye diagram and spectrum plot, as well as EVM, ACPR, ACLR, and BER measurements

Learn more at awr.com/elearning.

AWR-MG-V9-4-2020.2.24