AWR Design Magazine

Vol.19.3

Partner Spotlight:
TMYTEK 5G NR Phased-Array Solutions

Application Spotlight:
GaN HPA Design Success Using EM Analysis

Software Spotlight:
5G PA Design and Modeling for mmWave GaN Devices

Application Spotlight:
Design of a Highly Integrated LTCC Receiver

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NATIONAL INSTRUMENTS

Table of Contents

Customer Spotlight

TMYTEK

5G NR Phased-Array Solutions

Challenge

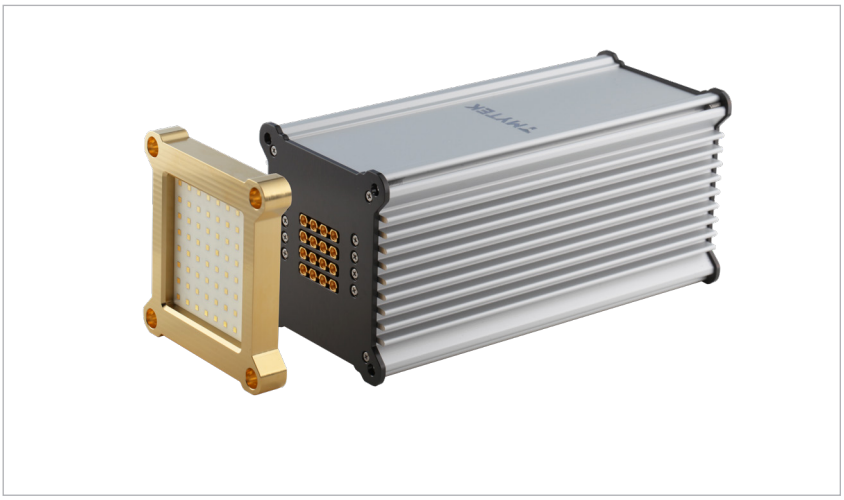
5G New Radio (NR) millimeter-wave (mmWave), unlike previous standards, uses dynamic beam steering to maximize connectivity by directing as much of the signal directly to the mobile device as possible. As a result, beamforming antennas represent a new area of development for many commercial manufacturers.

Solution

TMYTEK used NI AWR software to develop its groundbreaking BBox beamformer box product line, a highly modulized 28/39-GHz beamforming system that enables 5G developers to successfully develop innovative antenna designs and baseband technology. The BBox™ system provides reliable steerable beams to test and support development of phased array antennas and associated electronics, which must undergo rigorous calibrations and measurements under a large number of configurations through advanced over-the-air (OTA) testing to ensure optimum connectivity. BBox, a scalable and flexible system that includes a standard antenna kit, phase and amplitude controller, channel selector, up/down conversion and control host, is a comprehensive solution for both 5G NR mmWave antenna designers and baseband and protocol developers.

Conclusion

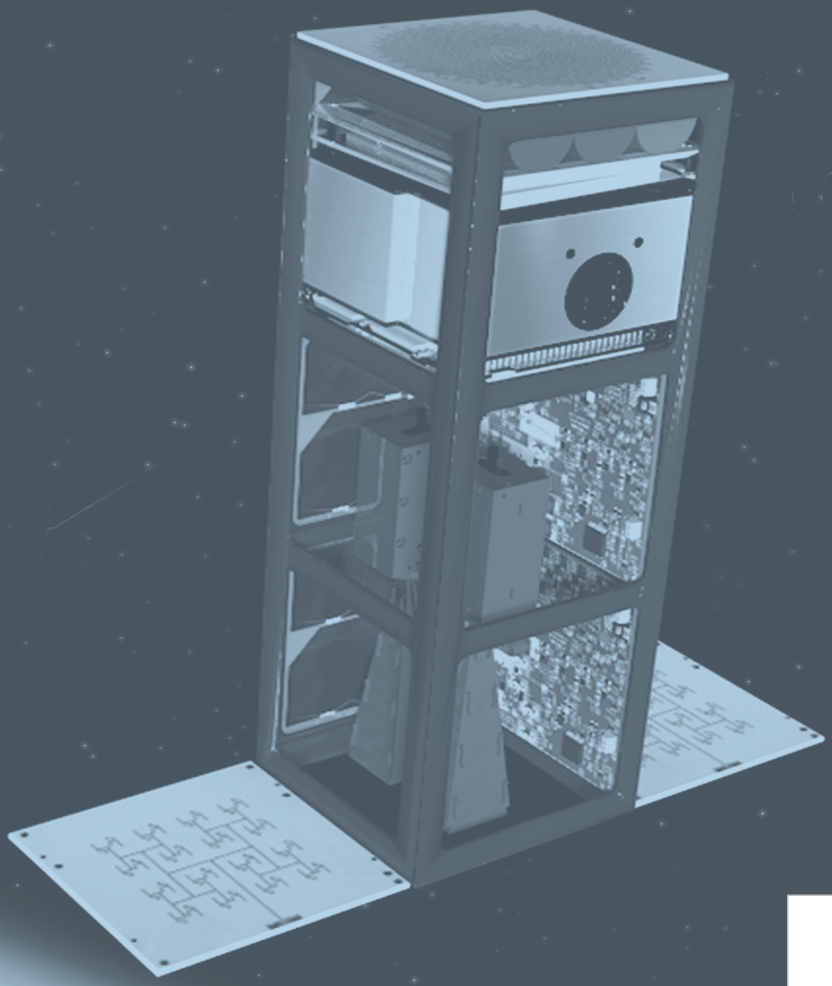
TMYTEK, as a fabless RF/microwave monolithic microwave integrated circuit (MMIC) design team, leverages the NI AWR Design Environment platform with solid-state IC technologies, including silicon germanium (SiGe), bipolar complimentary metal-oxide semiconductor (BiCMOS), gallium arsenide (GaAs) high-electron mobility transistor (HEMT), gallium nitride (GaN), indium phosphide (InP), and CMOS, from world-leading foundries to develop state-of-the art performance. Supported by process design kits (PDKs) developed for NI AWR software in partnership with leading MMIC foundries, TMYTEK technologists can offer high reliability for military, space, and mmWave commercial applications.



TMYTEK BBox beamformer box.

"NI AWR software is a very useful tool that helps us in each phase of a design project. It has many good technologies that streamline our design process. I am glad we choose NI as our partner."

Su-Wei Chang, TMYTEK



GaN HPA Design Success Using EM Analysis

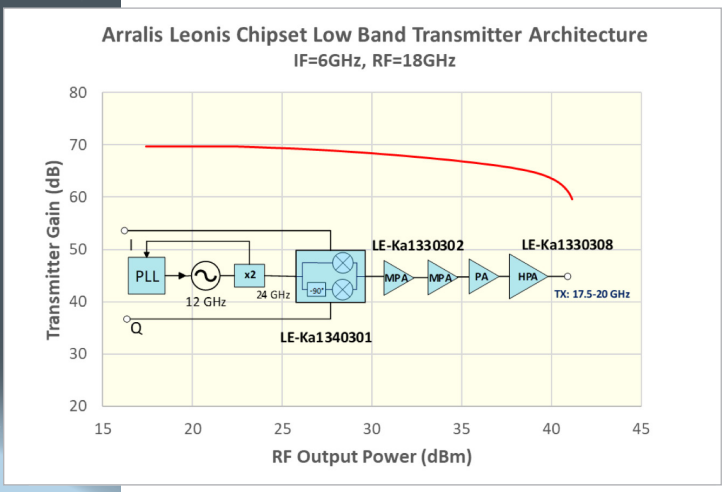
Overview

K/Ka-band satellite communications (satcom) can provide constant, uninterrupted access to information, driving companies like Facebook, Amazon, Inmarsat, and SpaceX to invest heavily in this spectrum for global broadband services.

These systems are enabled through high-power amplifiers (HPAs), which form the final link in the RF power chain of next generation, satellite-based, RF front-end components. The Leonis chipset from Arralis Ltd. (Limerick, Ireland), initially developed as part of the European Space Agency (ESA) ARTES program, addresses the growing demand for lower cost K/Ka-band satellite equipment.

The chipset includes mixers (IQ and sub-harmonic), up and downconverter core chips, switches, phase shifters, low-noise amplifiers (LNAs), and PAs. Within this chipset, the company's LE-Ka1330308 is a high-power monolithic microwave integrated circuit (MMIC) amplifier fabricated on space qualified 0.25 µm GaN on silicon carbide (SiC).

Arralis successfully demonstrated transceiver architectures for both uplink and downlink communications.



Arralis Leonis chipset for lowcost K/Ka-band satcom applications.

GaN MMIC Technology

Through the use of GaN technology, Arralis offers higher efficiencies, power density, and thermal conductivity compared with equivalent GaAs parts. In addition, GaN can operate at higher temperatures without loss of reliability, making it especially well-suited for satellite communications. Device thermography measurements of the die show a thermal resistance of 2.62 °C/W, resulting in a lifetime estimate of 5e7 hours.

The LE-Ka1330308 operates from 17.5-20 GHz and typically delivers 10 W saturated output power, with power-added efficiency of 25% and large-signal gain of 20 dB in a compact die size of 3.7 x 3.0 mm. The three-stage MMIC amplifier, which is fabricated on the United Monolithic Semiconductors (UMS) International Traffic in Arms Regulations (ITAR)-free, space-qualified 0.25 µm GH25-10 GaN on SiC process, is matched to 50 Ω with integrated DC blocking capacitors on RF ports and incorporates an output power detector to assist with system integration.

During the design phase, extensive circuit design and simulation was performed using the NI AWR Design Environment platform, specifically Microwave Office circuit design software, AXIEM EM simulator for 3D planar structures (MMIC manifold feed network, on-chip passives, and PCB evaluation board), and Analyst™ electromagnetic (EM) simulator for 3D EM analysis of the package.

The simulation software works with the active and passive MMIC component models developed by the foundry and organized into process design kits (PDKs) developed through collaboration between the NI and UMS modeling teams.

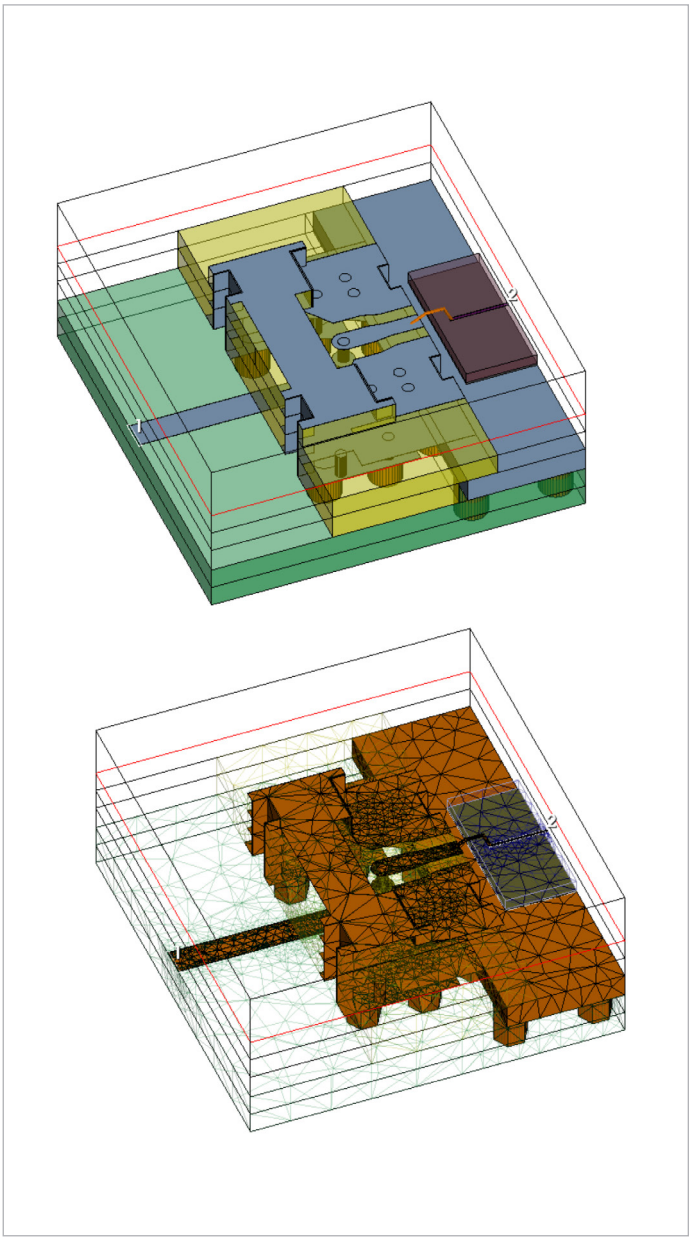
The MMIC die was represented in simulation using foundry-verified, schematic-based models and EM analysis, allowing the designers to reliably predict and optimize key performance metrics. Significant EM analysis and design optimization was carried out at the component and subcircuit level to ensure that parasitics and inadvertent EM coupling between structures is incorporated into the simulation. Towards the end of the design phase, larger and more integrated EM analysis was used as final verification and to ensure that all interactions were captured in simulation. These EM simulations were conducted using the AXIEM EM simulator.

The characterization and modeling methods implemented by the foundry have been validated through a well-established process/model qualification procedure, developed over years, that has been proven to yield reliable device models for the foundry's family of semiconductor processes. The extracted nonlinear models account for trapping phenomena and transistor self-heating. In addition to electrical characterization, the UMS modeling team performs a comprehensive study of the thermal device behavior and other non-stationary effects to improve the quality of its nonlinear device modeling.

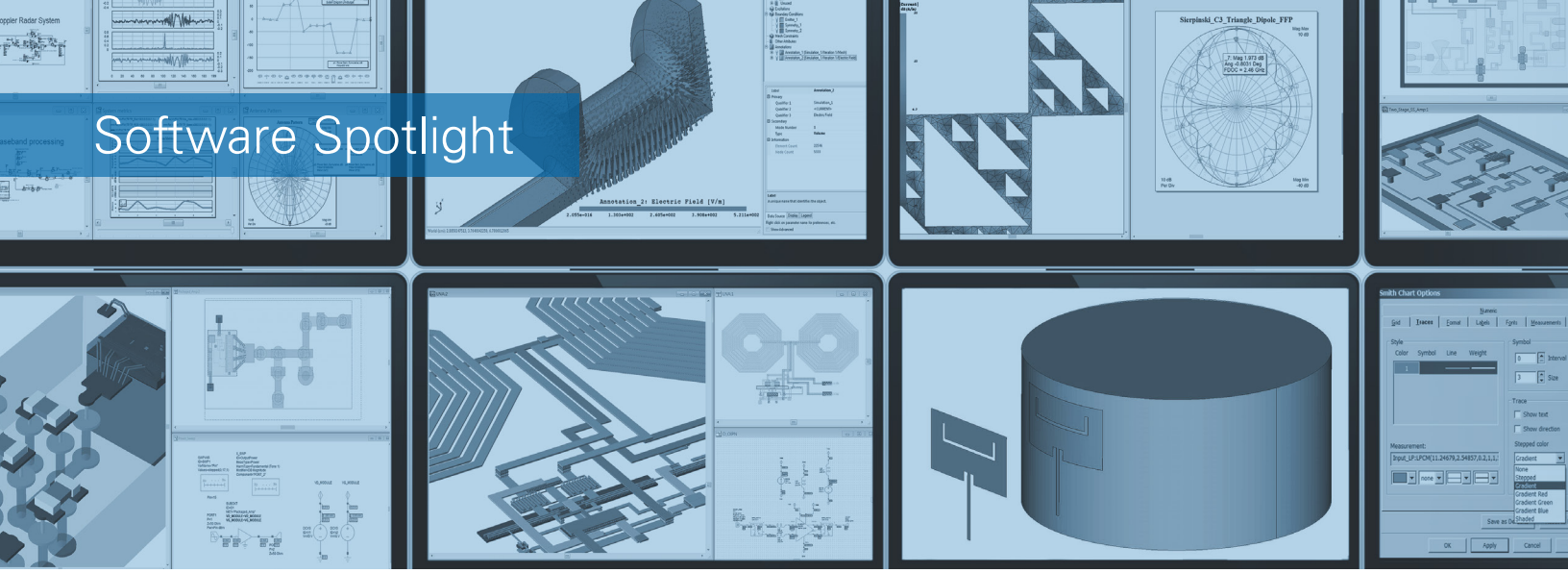
Packaged Device

The success of the bare die MMIC has fuelled the subsequent development of a packaged part that will facilitate a more convenient solution for system integration.

This package will provide a hermetically sealed solution with enough space to accommodate the die and decoupling capacitors, while also minimizing the RF I/O bond-wire length. The RF transition was simulated using the Analyst EM simulator to minimize return loss due to impedance mismatches between the MMIC, the package, and the evaluation board. The simulation results show a well-matched transition with insertion loss of 0.25 dB. This will translate to an overall gain reduction of 0.5 dB and power reduction of 0.25 dB for the packaged part compared to bare die option.



Details of package model I/O port simulation setup (top) and resulting mesh in Analyst software (bottom).



5G PA Design and Modeling for mmWave GaN Devices

Overview

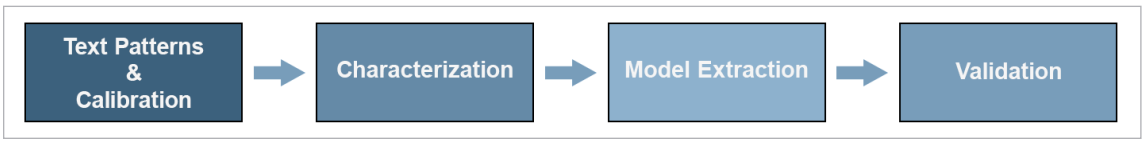
Advanced semiconductor technology plays an important role in evolving RF and microwave applications for 5G and satellite communications where the next generation of systems is moving towards mmWave frequencies. Support of design flows and model availability for these semiconductor technologies is critical to designers for successful product development. In response, EDA software vendors offering MMIC and RFIC design solutions must work closely with leading foundries to ensure their products provide increased integration and higher performance while lowering cost and size requirements.

This article highlights techniques supporting device modeling of III-V wide bandgap semiconductor technology, specifically the United Monolithic Semiconductors (UMS) GH25 (0.25 µm gate length), GaN on SiC process for mmWave PAs targeting new communication and defense systems. Model accuracy is validated through simulation and measurements of multiple designs that were developed using the GH25 PDK, serving as a development framework that will guide future work in support of evolving process node technologies like the GH15 (0.15 µm gate length) GaN on SiC process currently in the qualification phase.

GH15 technology is an ideal candidate for 5G applications, as demonstrated by a 10-W Ka-band (29.5 – 36 GHz) PA and a 2-W front-end module (24 – 30 GHz) that integrate a GH15 PA with other RF functions implemented in a GaAs process.

GaN Technology and Modeling Challenges

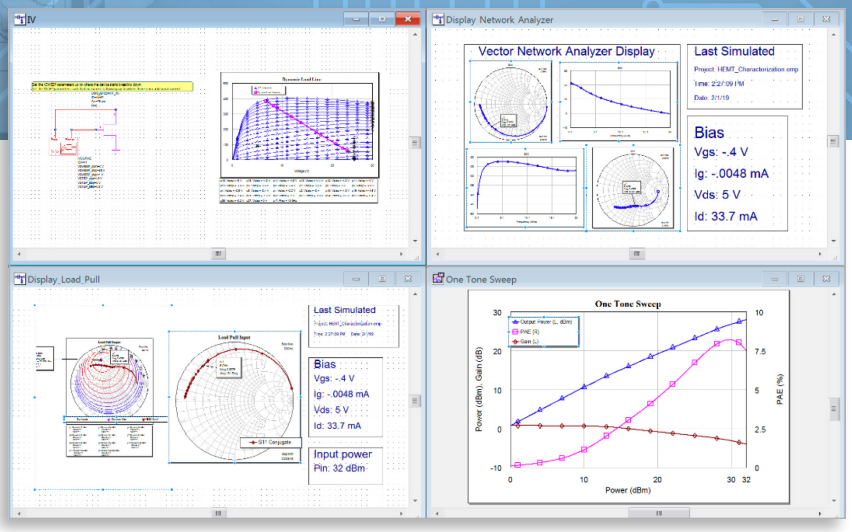
Short gate-length GaN devices have demonstrated excellent performance for mmWave PAs. Offering higher operating voltages and reduced device parasitics, these GaN transistors provide higher output power densities, wider bandwidths, and improved DC-to-RF efficiencies than their GaAs counterparts. In order to take advantage of this enhanced performance, designers need a scalable model that accurately captures the complex behaviors of the device during circuit simulation. The behavior of the trapping and thermal phenomena in GaN devices represents a real challenge for transistor modeling.



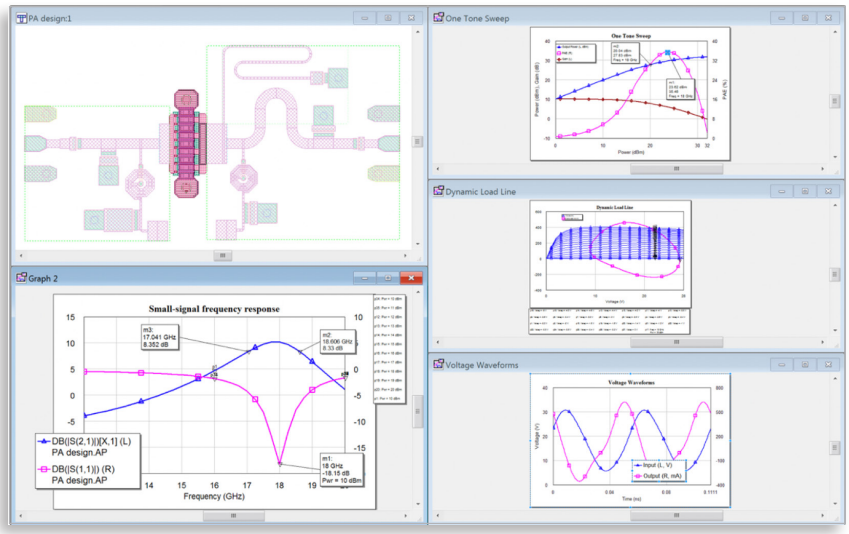
The figure illustrates the main steps to active device modeling incorporating measurements, model extraction and validation. This fitting process and characterization data supports the development of transistor models used by software design tools such as the NI AWR Design Environment platform to predict the overall MMIC behavior when these devices are embedded in a matching/biasing network and excited by RF signals. Models are organized into PDKs supported in Microwave Office circuit design software with electrical and physical layout information to enable the design of MMICs using the UMS GaN or GaAs process.

PDKs for Circuit Simulation

Active device models and passive on-chip components, along with their parametric layout cells (PCells) are organized into PDKs to support MMIC development using these technologies. These PDKs provide simulation-ready device models to design ICs and generate layout masks for fabrication. The PDKs for Microwave Office software are available directly from UMS and include a layout process file (LPF), which defines the material stackup and metallization layers for EM simulation.



Microwave Office software offers a pre-configured example project for field-effect transistor (FET) characterization that designers can use to investigate basic functioning of the transistor model before beginning their design. The default device can be replaced with the UMS nonlinear hot FET model and simulations to observe the device DC and RF performance can immediately be launched. After adding the UMS PDK to the process library, the project layout browser will be populated with the UMS LPF file.



The PDK models will appear in the elements browser for user placement in the schematic design window. The FET characterization project is configured to simulate standard device measurements, including DC IV curves, S-parameters, single- and two-tone swept power such as gain, output power, and power-added efficiency (PAE), and power-dependent output load-pull contours.

With the 0.25 µm PDK installed, the designer is able to apply a combination of linear/nonlinear and load-pull analyses. The recently introduced network synthesis feature in Microwave Office software supports the development of the bias and matching networks from frequency response (S-parameters) or load-pull analysis to achieve optimum power, linearity, and/or efficiency performance. This capability was used to determine the appropriate source/load impedance for an 8 x 75 µm (0.25 µm) GaN device operating at 18 GHz. An approximate short circuit was presented to the output of the device at the second harmonic (36 GHz) via a shunt capacitor to improve the peak PAE (~36%).

Along with the UMS PDKs currently available for Microwave Office software, the foundry will shortly release the GH15 process and is also developing the GH10 0.1-µm GaN process.

PDKs From Foundry Partners

Before 5G communication systems and automotive radar can benefit from the bandwidth and range resolution offered by mmWave spectrum, RF front-end designers will need to develop PAs, LNAs, filters, switches, and other critical radio components that work at these frequencies. Technologies developed for sub-6 GHz communications or X-band radar simply won't meet the performance requirements at 28, 39, or 77 GHz.

Fortunately, semiconductor process engineers, material scientists, and their fellow researchers have developed and/or enhanced technologies with the performance that designers need to address mmWave applications. Short-gate length GaN on SiC and glass-based passive microelectronics are two emerging technologies that deliver the performance to meet these mmWave system requirements.

Going hand in hand with the emergence of these new technologies, designers rely on supporting simulation models, schematic symbols, and layout/ manufacturing information in the form of PDKs to develop front-end products. 3D Glass Solutions, Inc. (3DGS) and UMS are working directly with technologists from NI to provide foundry authorized PDKs for their respective mmWave processes. The PDKs allow designers to develop critical front-end components such as amplifiers and filters for 5G, automotive radar, and other mmWave applications.

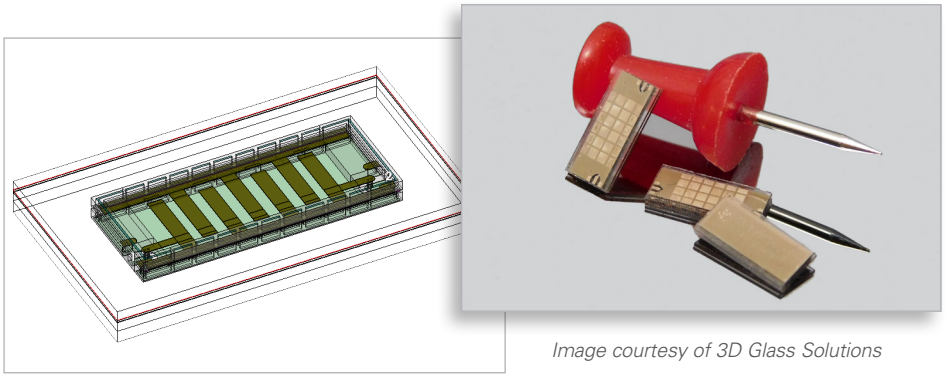


Image courtesy of 3D Glass Solutions

PDKs for NI AWR software are available directly from 3DGS and UMS as well as other leading foundries. To learn more, visit awr.com/awr-connected-foundries.

AWR.TV

AWR.TV is a comprehensive, multimedia resource for technical and product information pertaining to NI AWR software features, applications and solutions. Recent additions to AWR.TV include:

- Industry Insights: 3D Glass Solutions
- Industry Insights: Richardson RFPD
- Industry Insights: UMS

Resource Library

The resource library on ni.com/awr is a dedicated and searchable landing page for technical content on NI AWR software products, and solutions. Recent additions to the resource library include:

Webinars

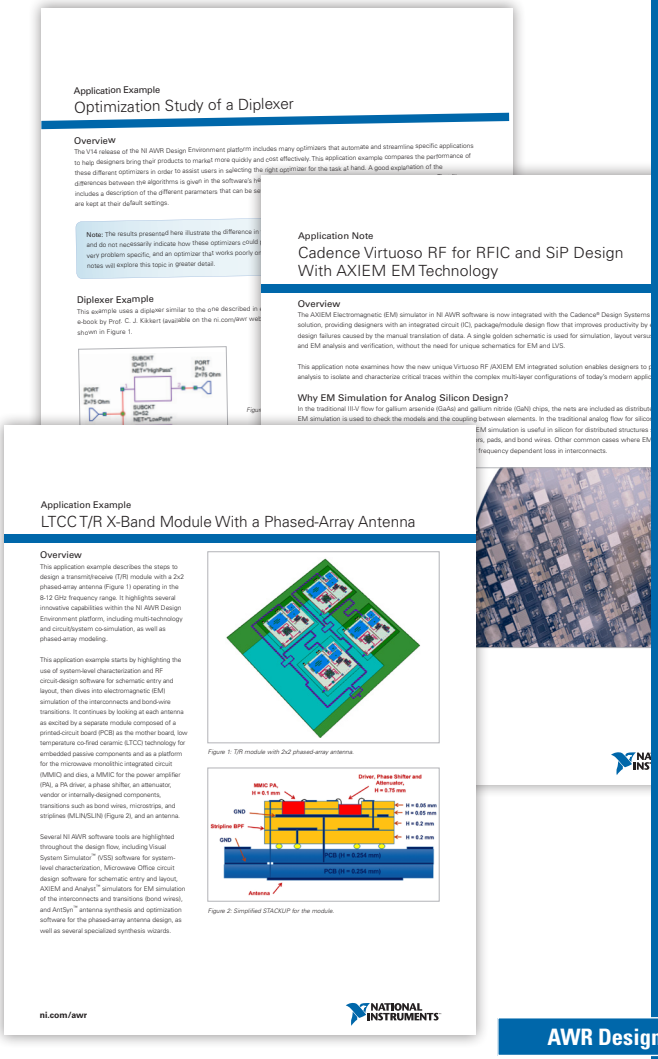
- An Enhanced Design Flow for Cavity Combline Filters
- Reappraisal of RFPA Modes
- Virtual Antenna Matching-Circuit Design

White Papers

- A Designer's Primer on Radar Systems
- Microstrip Antenna Design eBook
- A Designer's Primer on IoT

Application Notes

- Optimization Study of a Diplexer
- AXIEM EM Simulator Within Cadence Virtuoso RF for RFIC/SiP Design
- LTCC T/R X-Band Module With a Phased-Array Antenna



Application Spotlight

Design of a Highly Integrated LTCC Receiver

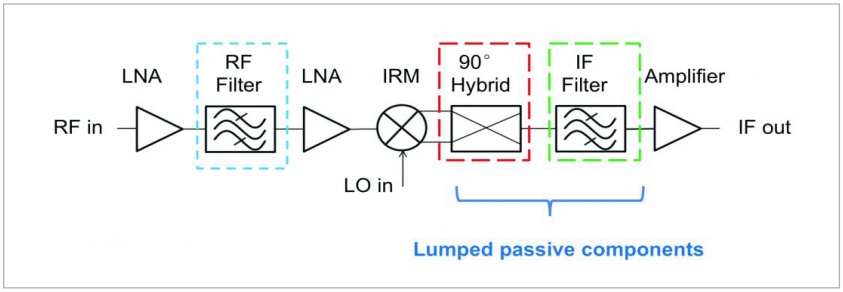
Overview

The X-band frequency range is widely used for satellite communications (satcom) because it provides a number of advantages over lower-frequency systems, including resilience to interference and weather, smaller terminal size, higher data rates, and ability to provide remote coverage. Satcoms are further enhanced through the use of active phased-array antennas, which are made possible by advances in electronic packaging technology and semiconductor device performance. By employing space-saving, high-functionality system-on-chip (SoC), system-in-package (SiP), and low-temperature co-fired ceramic (LTCC)-based modules, satcom systems with active-phased arrays offer greater flexibility and robustness, as well as the ability to detect targets more accurately through electronic beam scanning.

This article describes the design of a highly integrated X-band receiver module based on a 10-layer LTCC substrate using NI AWR Design Environment software. The design achieved the key design goals by integrating surface-mount components with embedded distributed (passive) components built directly into the receiver module substrate.

LTCC Circuit Design Flow

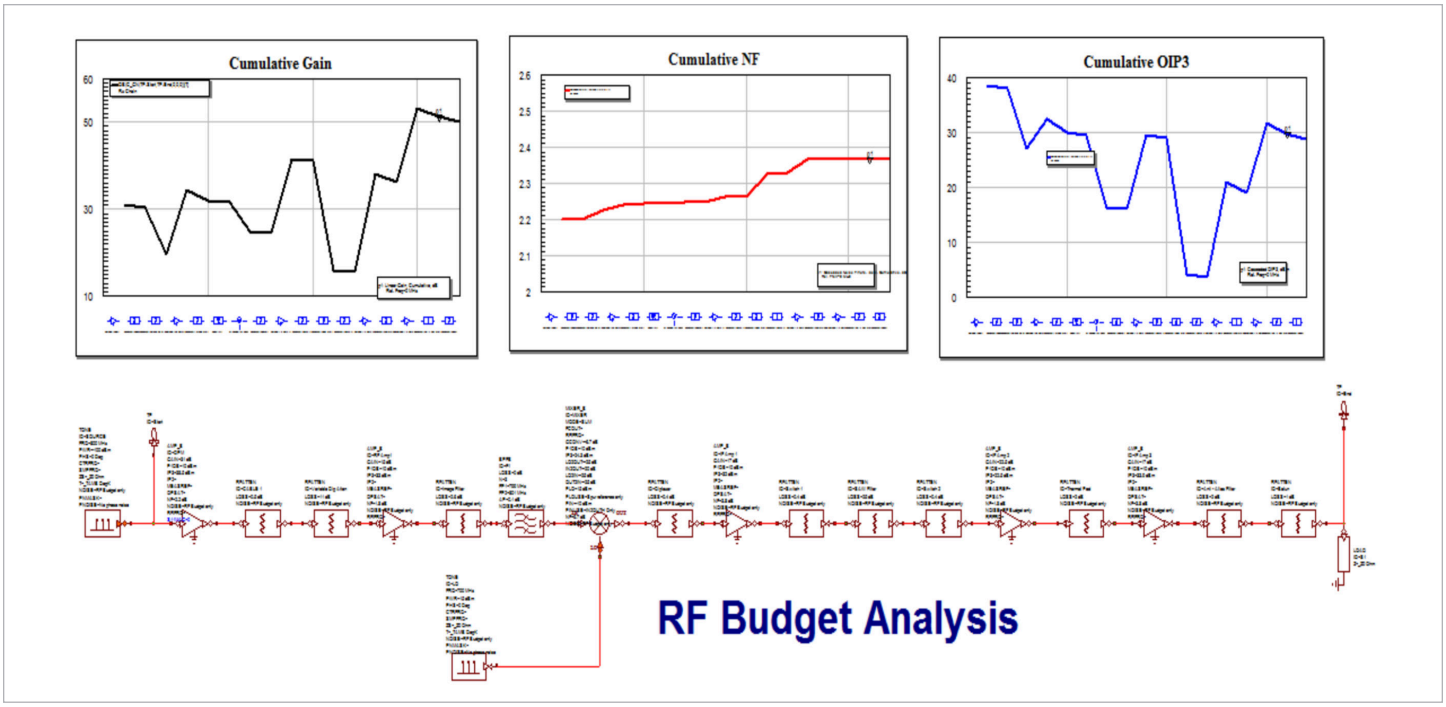
The X-band receiver architecture in this design downconverts signals at a center frequency of 9 GHz to the intermediate frequency (IF) center of 60 MHz. The receiver was designed to achieve a gain over 51 dB, a noise figure (NF) below 2.5 dB, and image rejection above 37 dB. The overall size of the receiver module was restricted to a 54 mm × 15 mm × 1 mm form factor. The 15 mm width of the receiver module was predicated on the element spacing in the phased array, which called for a half-wavelength distance between adjacent antenna array elements at the design frequency. Since size reduction was a key goal, an initial design task was to choose an appropriate RF link with a minimal number of circuit elements.



Block diagram of the X-band receiver module.

The system was composed of two LNAs, two X-band BPFs, one image rejection mixer (IRM), one quadrature hybrid coupler, one IF BPF, and one IF amplifier. This configuration and lineup of devices provided an overall path gain of about 51 dB.

The 10-layer LTCC structure provided an excellent medium for developing a compact, high-density module with integrated passive components constructed from multiple stacked layers of metallization and dielectric substrate forming the capacitive and inductive elements from which passive devices (BPFs/couplers) could be designed. Vias and trace metals provided the interconnects between elements in the receive module.



Block diagram of 9 GHz receiver and RF budget analysis.

Link Analysis with Visual System Simulator

Visual System Simulator™ (VSS) software helps designers establish the right system architecture and formulate suitable specifications for each of the underlying components in communications systems. They can perform rapid exploration of system architecture and component specification options in order to achieve ideal cost, performance, reliability, and size tradeoffs.

The designers of this X-band receiver module used behavioral models to represent the RF properties of each component in the receiver, enabling them to investigate the individual contribution of each component, as well as the overall system performance, and to make any necessary adjustments in order to achieve the required specifications. The figure below shows the block diagram (top) and RF budget analysis (bottom) for the 9 GHz receiver, which includes the overall performance for a given measurement type such as NF, gain, or OIP3, as a function of cascaded components in the RF signal chain.

RF and IF BPF Design

While the dual-mode BPFs reported in the literature suppressed the upper stopbands, the orthogonal orientation of the I/O feed ports was not well-suited for making an RF connection to the adjacent components and therefore a modified dual-mode LTCC BPF with nonorthogonal I/O feed ports was developed.

The AXIEM simulator software was used to simulate the structure's frequency response and obtain the physical dimensions based on filter performance optimization. The parameterization of the filter dimensions allowed the filter geometry to be modified not only for passband/reject-band performance, but also for yield optimization, which was improved to over 85% for the known manufacturing tolerances.

Conclusion

Three passive microwave components were proposed and integrated into a 10-layer LTCC receiver module with high integration. The combined use of VSS software for system simulation of the link budget analysis, Microwave Office for linear/nonlinear RF component synthesis and simulation, and the AXIEM EM simulator for passive device characterization proved critical in the successful development of this compact, LTCC X-band receiver for phased-array applications. The use of 10-layer LTCC substrates for a compact design using stacked passive components was made possible with the LTCC design flow and PDKs available with NI AWR software.

AWR-MG-V9-3-2019.11.11