APPLICATION **NOTE**

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RF Module Design and Development with Cadence AWR Software

RF modules offer a large amount of functionality in a small space, but they can be an engineering challenge for development teams. When combining multiple integrated circuits (ICs) into a single package, it is necessary to model the electrical behavior of many different technologies, such as interconnects (transmission lines) and embedded distributed components, as well as RF, analog, and digital components. The choice of Electronic Design Automation (EDA) software can be critical for achieving simulation results that are closely matched to final measured results.

Design Overview

This application note explores the fundamental design challenges faced when creating and producing high-frequency modules for a range of wireless system applications, and the tools required for an effective workflow supporting the design and integration of these modules in the shortest time possible. Much of this capability can be addressed using the Cadence® AWR Design Environment® platform to define and manage the electrical and physical attributes of a wireless module and to perform circuit, system, and electromagnetic (EM) co-simulation within a single integrated environment that also supports interoperability with industry-leading CAD layout tools.

Trends Driving Module Development

Developing the many wireless devices and supporting infrastructure that will connect future smart hardware such as internet of things (IoT), advanced driver assistance system (ADAS)-enabled vehicles, wearables (Figure 1), and biomedical devices will be a massive engineering effort requiring cost-effective RF front-ends that can be manufactured for mid- to high-volume production. Much of this RF connectivity will be achieved through ICs combined into multi-functional modules containing all of the circuitry needed to transmit and receive RF signals.

Figure 1: Miniaturized consumer electronics will be among the devices requiring radio modules to provide wireless connectivity (Image courtesy of Striiv)

As a self-contained subassembly, today's RF modules are drop-in components that provide wireless connectivity for all types of systems, including monitoring and remote-control equipment. These modules may include an integrated antenna or a connector for an external antenna, as well as a serial interface for communication to the host processor. They are typically shielded to limit unintended emissions and increase electromagnetic compatibility (EMC) immunity.

RF design is notoriously complex due to radio-circuit sensitivity and the accuracy needed to simulate components and associated layouts when targeting a desired performance at a specific frequency. In addition, reliable RF circuits require tight tolerances of the manufacturing process to ensure that the performance is not adversely affected. Radio circuits are usually subject to limits on radiated emissions, requiring conformance testing and certification by a standardization organization such as European Telecommunications Standards Institute (ETSI) or the U.S. Federal Communications Commission (FCC).

Consequently, engineers will often design a circuit that requires radio communication using a premade radio drop-in module rather than attempting their own discrete design. This approach often saves time and money on development. To serve this design trend, manufacturers of discrete RF components may need to consider adding modules with integrated RF functionality into their own product portfolios.

Integrating Functionality – Systems/Subsystems Approach

Creating new, multi-die heterogeneous modules and corresponding system boards involves multiple engineering teams with different perspectives. Module designers, organized into a multidisciplinary team, must cooperate to solve numerous optimization problems, including system input/output (I/O) requirements, thermal and signal integrity constraints, die placement and orientation, stacking configurations, package substrate and interposer design, and interconnect design at the IC and package level, all while taking into account the constraints on the system's PCB.

Although it is possible to organize the different design disciplines in a coordination meeting, a successful joint plan really requires a methodology, a process, and the design technology/automation for tying these worlds together. When integrating transmit/receive (TX/RX) functionality into a single device, a system approach helps delegate individual radio-block development while managing the overall electrical, mechanical, and thermal design.

System simulation tools that operate in conjunction with physical realization tools support top-down/bottom-up analysis that enables these different engineering teams to obtain design requirements from a single 'master' plan and compile individual results into an evolving simulation model of the entire module. The system architecture defines the arrangement of the individual radio blocks and their performance requirements, while system simulation based on behavioral models supports first-pass component specification from RF-budget measurements that include gain, power level, IP3, noise figure, and more, as shown in Figure 2.

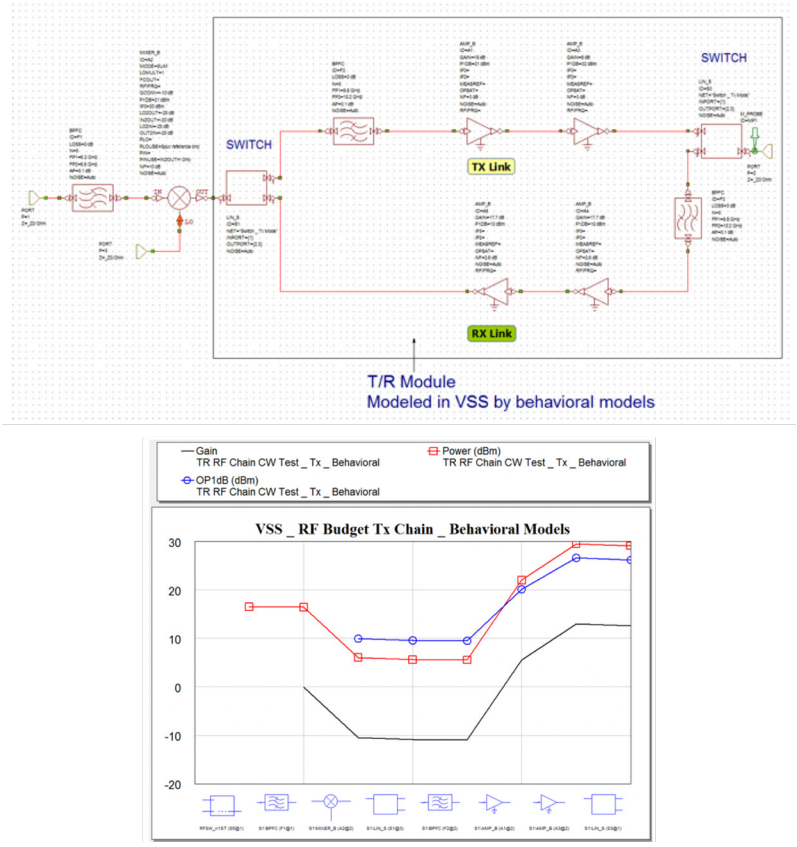


Figure 2: System-level budget analysis based on behavioral models supports system development and component specification

Cadence AWR® Visual System Simulator® (VSS) system simulation software provides designers with a comprehensive library of RF and digital signal processing behavioral models to create and analyze end-to-end communication systems or module-based TX/RX subsystems. Operating within the AWR Design Environment platform, AWR VSS software also supports co-simulation with detailed circuit- and EM-based designs from the Cadence AWR Microwave Office® circuit simulator, as well as the Cadence AWR AXIEM® 3D planar and Analyst™ 3D finite element method (FEM) EM simulators. This system/circuit/EM co-simulation capability provides the design verification necessary when integrating functionality into a small form factor.

Design Partitioning

Early in the module design process, the exact capabilities of the module must be determined, including the overall footprint, location of I/O ports, available power supplies, and underlying architecture. Engineering teams can then focus on the physical, electrical, and thermal aspects of the module development (which include physical partitioning such as component placement,orientation, and shielding), as well as the electrical partitioning (which breaks down to power supply distribution, RF routing, placement of sensitive circuits and associated signal paths, and providing adequate grounding), as shown in Figure 3.

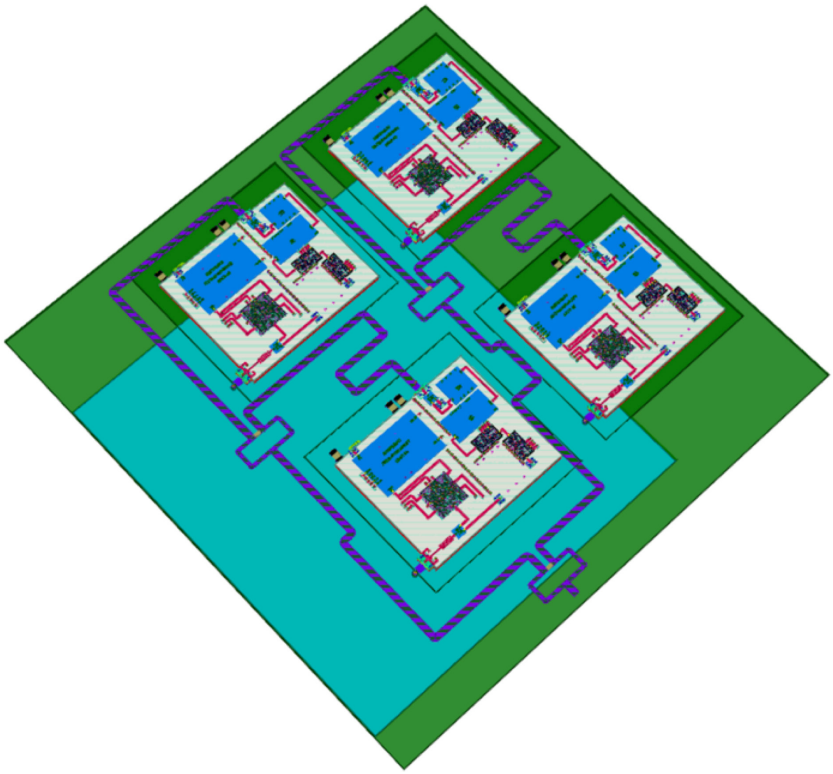


Figure 3: Module development must provide required functionality within a given form factor and I/O port alignment such as this feed network for a 2 x 2 phased array patch antenna

For RF designs, physical and electrical considerations are intertwined. For example, designers will try to separate high-power RF amplifiers (HPAs) from low-noise amplifiers (LNAs) as much as possible in order to reduce their interactions. Shielding and placement of components on opposite sides of the module substrate are among the techniques used to keep high-power RF transmitter circuits from interfering with low-power RF receiver circuits.

When possible, RF outputs generally need to be well separated from RF inputs and sensitive analog signals should be kept well away from high-speed digital and RF signals. In addition, a module should have at least one ground plane that is as solid as possible, generally without partitions and with a minimum of voids (cutouts).

In addition to physical implementation, system verification is a critical part of module design. Accurately simulating high-frequency electronics requires system-level analysis that captures the behavior of diverse physical structures using a range of modeling technologies. Simulation of a complete signal path (or channel) requires accurate circuit/netlist or system-level behavioral modeling of ICs, all chip-to-chip interconnects (including IC packages, PCB traces, connectors, and vias with associated bypass capacitors), associated power-distribution structures (planes in the package and PCB, decoupling capacitors, and stitching vias), and embedded (off-chip) passive components.

Integrating Heterogeneous Technologies

The integration of one or more ICs onto multi-level substrates is a challenging task at higher frequencies where electrical characterization must be performed using EM simulation of structures implemented via layout-focused design tools, as shown in Figure 4. In this design phase, the focus is on electrical modeling of the floor plan while addressing the physical I/O requirements of the IC, integrating the package substrate constraints and variables, and considering the multiple PCB platforms (form factors) with which the module is intended to work.

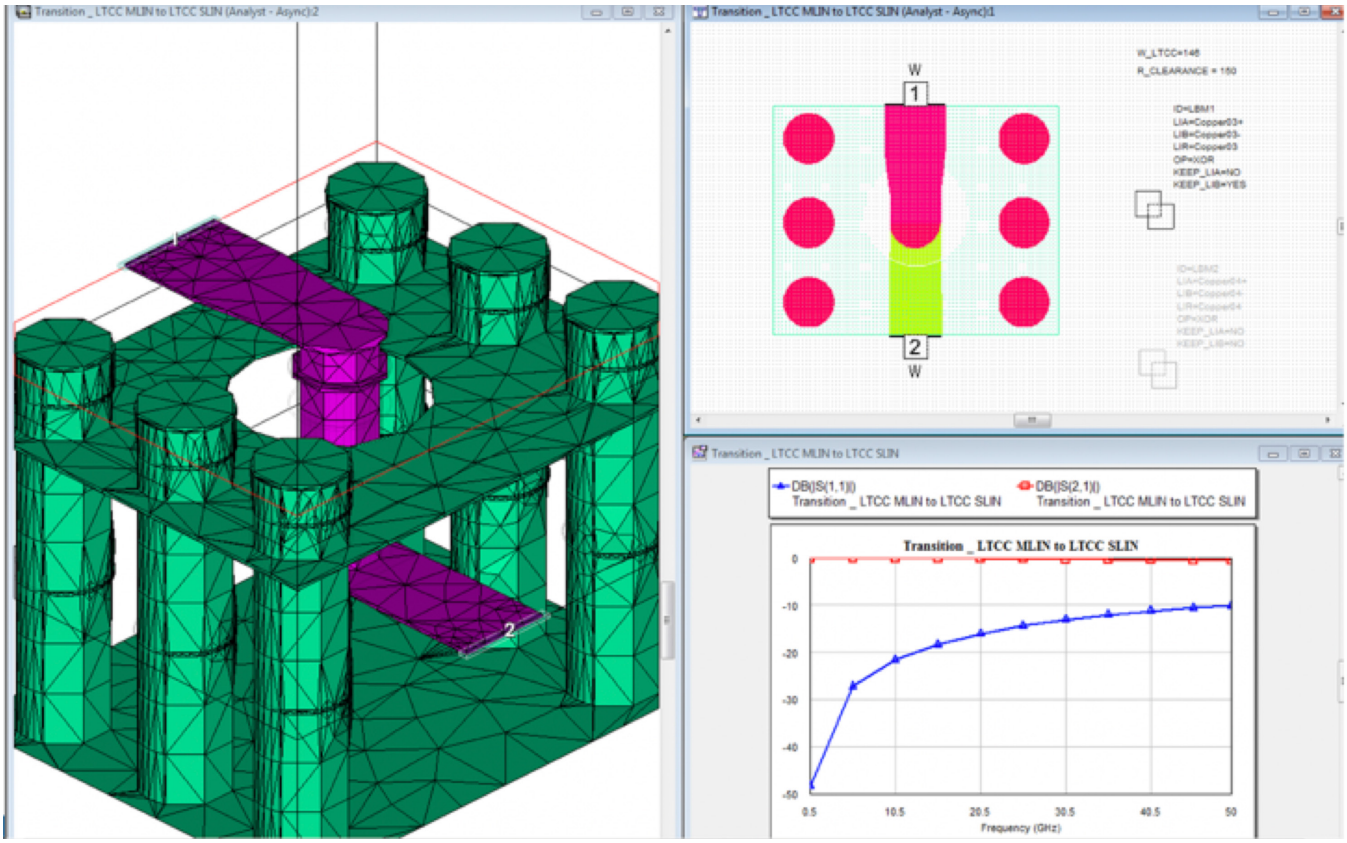


Figure 4: EM simulation is often required to electrically characterize passive components and interconnects such as transitions between layers of multi-layer substrates

Given how frequently traces are rerouted to suit the repositioning of components within a module during the design phase, circuit/EM co-simulation allows the electrical impact of trace rerouting to be addressed in real time. To support the physical design, many layout tools offer powerful place-and-route automation, which helps designers efficiently place electronic components within a limited amount of space. This is followed by routing, which determines the optimum wiring path based on a set of defined rules and limitations of the manufacturing process. Since the width and length of these traces will influence the electrical performance for RF designs, their influence needs to be accounted for in simulation, but not necessarily in a schematic, where a shorted wire between element nodes may be preferable.

The iNet intelligent net technology within AWR software enables a designer, for instance, to draw a simple short-circuit interconnect in the electrical schematic diagram and then in the layout route that interconnects with the internal knowledge of the technology being used. With iNet technology, designers can have a wire on the schematic that is routable over many layers, with an auto via insertion capability that knows how to terminate the route on whatever pin(s) to which it is connected. iNet technology lets users route a wire in their schematic, which ultimately enables them to incrementally model it as they refine their design along the way to tapeout. This enables them to address interconnects right up front in the schematic and dynamically synchronize them with the rest of the flow, from layout to EM simulation and verification.

Advanced packaging research and development teams must work closely with system and circuit design teams to optimize interconnect and embedded passive technologies for size, reliability, and performance, and to develop and incorporate parametric-based RF models within existing design flows. Considerable research activity is dedicated to characterizing and modeling the RF properties of various assembly techniques in order to reduce parasitics and optimize the signal transmission characteristics. Special interest focuses on different bonding techniques such as wire bonding, flip chip, ribbon bonding, embedded chip solutions, and more, as well as on-passive components such as resistors, capacitors, inductors, transformers, and transmission lines. Substrate technologies such as low-temperature co-fired ceramic (LTCC) and multi-layer organics are among the more popular materials being developed for RF applications.

Depending on the intended functionality of the module, integration may require a set of technologies such as wafer thinning, embedded passive components, vertical system integration, assembly of thin components, thin interconnect technologies, bumping/ball placing, and dicing. All these technologies need to be optimized and adapted in a modular integrated process flow. Advanced module packaging acts as a system-integration carrier, with the potential to reduce the packaging cost and increase the functionality of a system at the same time (Figure 5).

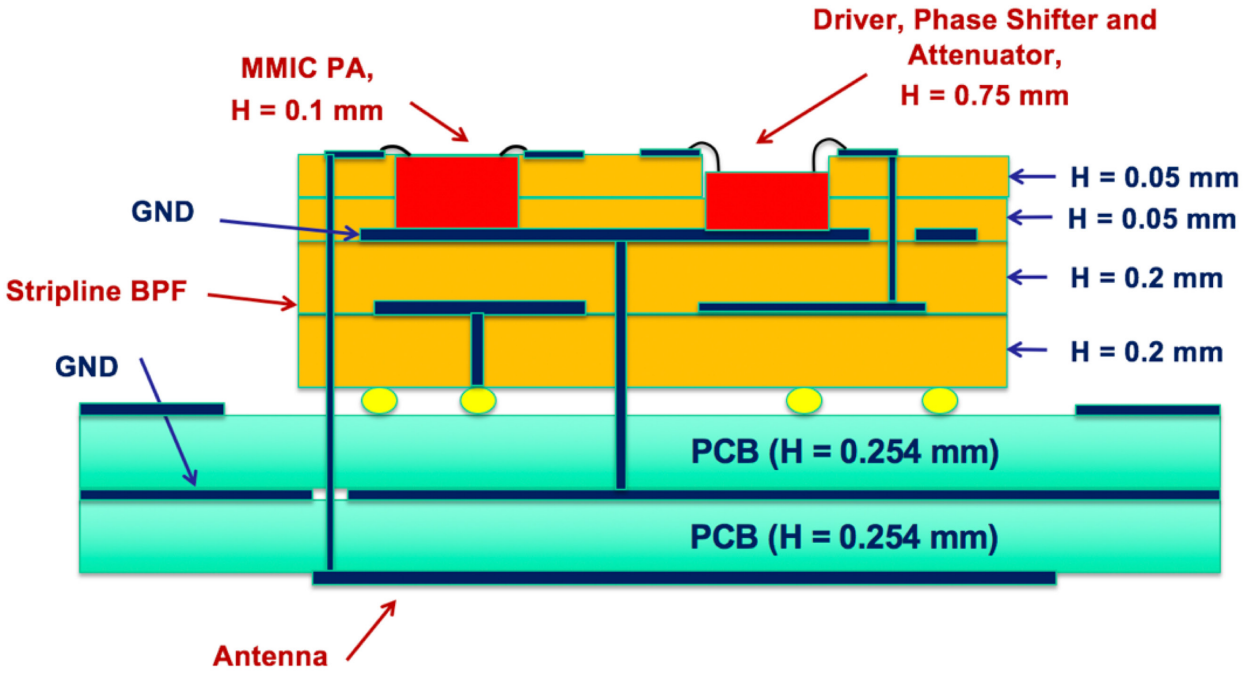


Figure 5: Modules rely on advanced interconnect technology, multi-layer substrates, and component stacking to reduce the device footprint while increasing overall functionality

Interconnect Technology – EM Simulation and Modeling

Optimizing the performance of the transition between different substrates is a common design requirement for module designs with different IC and PCB process technologies. For example, a designer might be interested in the transition between a board and a ball-grid array module, or between a quad-flat no-leads (QFN) package and a chip, by using bond wires (Figure 6). To address this problem, an engineer may create a single model using EM analysis to extract the S-parameters for the combined structure representing the I/O port of the board, the transition itself, and the I/O port associated with the QFN package. The board and package ports (wire-bond pads) would be based on their respective substrate stack-up (layers, materials, and more). The S-parameter response could then be inserted into the schematic for subsequent circuit simulations.

A superior design flow manages multiple, heterogeneous technologies within a single hierarchical project. At the circuit simulation and layout level, each module component can be defined by a schematic containing an arrangement of elements from a process design kit (PDK) that includes the electrical characteristics of the element for a range of operating conditions such as frequency and input power, and details of the substrate stackup. Figure 6 shows such a design flow.

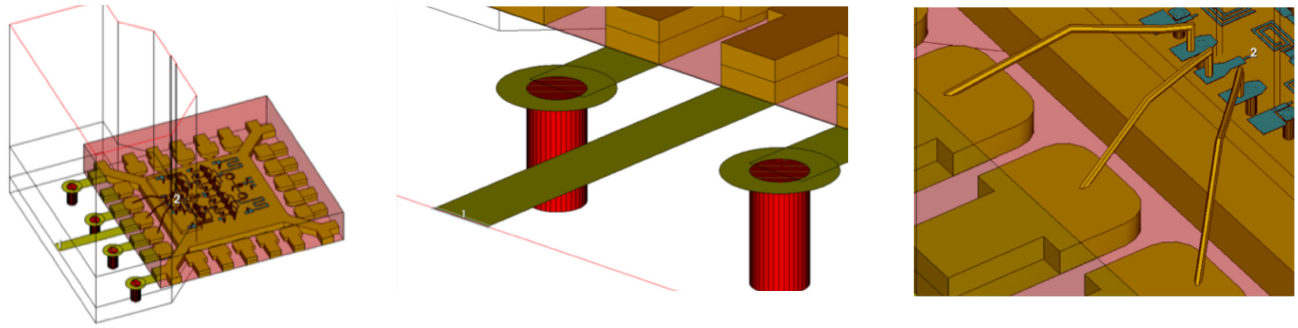


Figure 6: A monolithic microwave IC (MMIC) in a QFN package on a Duroid board. The launch has been drawn at Port 1, which goes onto the flat package and then to the MMIC via bond wires at Port 2, grounding vias from the board PDK and a closeup of the bond wires

The stack-up data provides information for the processing masks used later in manufacturing and dictates the model behavior of distributed components such as transmission lines and discontinuities such as microstrip-width steps, tee-sections, and bends. By using multiple libraries/PDKs for different manufacturing technologies, designers can easily integrate board, module, and chip technologies within the same EM project. This is accomplished in AWR software with the concept of hierarchy in the layout and automation developed in the EM interface.

For instance, the top schematic may represent the board with the various models, design rules, and layout settings, all specific for that board. Layout cells come from the board PDK. Another schematic could be developed for the chip design, using a PDK with the corresponding models and layout cells. With hierarchy, the schematic describing the chip can be used as a subcircuit to the board schematic in the module design. In this way, the designer can simulate both the board and chip together as a single network. For the wire-bonded chip-to-board example, the structure represents an interconnect that requires 3DEM simulation, since the wire bond is a 3D object and the bonding pad of the IC is adjacent to the edge of the die (planar EM solvers assume infinite dielectric layers in their formulations). Three-dimensional shapes are handled by extrusion of the polygons or by using 3D cells. Extrusion is a straightforward method in which a 2D polygon is drawn and a vertical distance is specified, either upward or downward.

In this chip-package-board design flow, the EM Socket architecture within AWR software streamlines the sharing of model layout information between AWR tools and EM simulators. The layout is automatically "flattened" before being sent to the EM simulator, meaning the hierarchy of the layout is removed and the layout consists of the various dielectric layers and shapes of all the subcells merged into one layout. The design can therefore solve multi-technology layouts in place using the Analyst simulator or through the EM Socket technology to 3D simulators such as AWR Analyst 3D FEM or Cadence Clarity™ 3D FEM/FDTD Solver, without worrying about hierarchy and how layout cells are handled.

From the described module design flow, AWR Microwave Office software enables users to quickly take advantage of features such as:

- Multiple PDKs and libraries for different physical technologies
- The ability to drive multiple simulators from one set of layout rules, layer stackup definitions, and shape simplification rules
- The use of 3D cells in a 2D layout to support both layouts in one environment
- Control of EM simulation results from different simulators using data sets

RFIC Integration

A module can be designed with off-the-shelf or custom RFICs/MMICs. Off-the-shelf components are often designed to a characteristic impedance of 50Ω and come with electrical operating and die attach instructions in the form of a datasheet or application note. For this scenario, the amount of RF design required to integrate the IC with the module may be minimal, perhaps nothing more than addressing the impact of the interconnecting wire-bond inductances. For custom RFICs or other components such as bulk acoustic wave (BAW) and surface acoustic wave (SAW) filters, off-chip elements may be required, and the RFIC component design and integration efforts may be shared by the RFIC and module laminate designers, as shown in Figure 7.

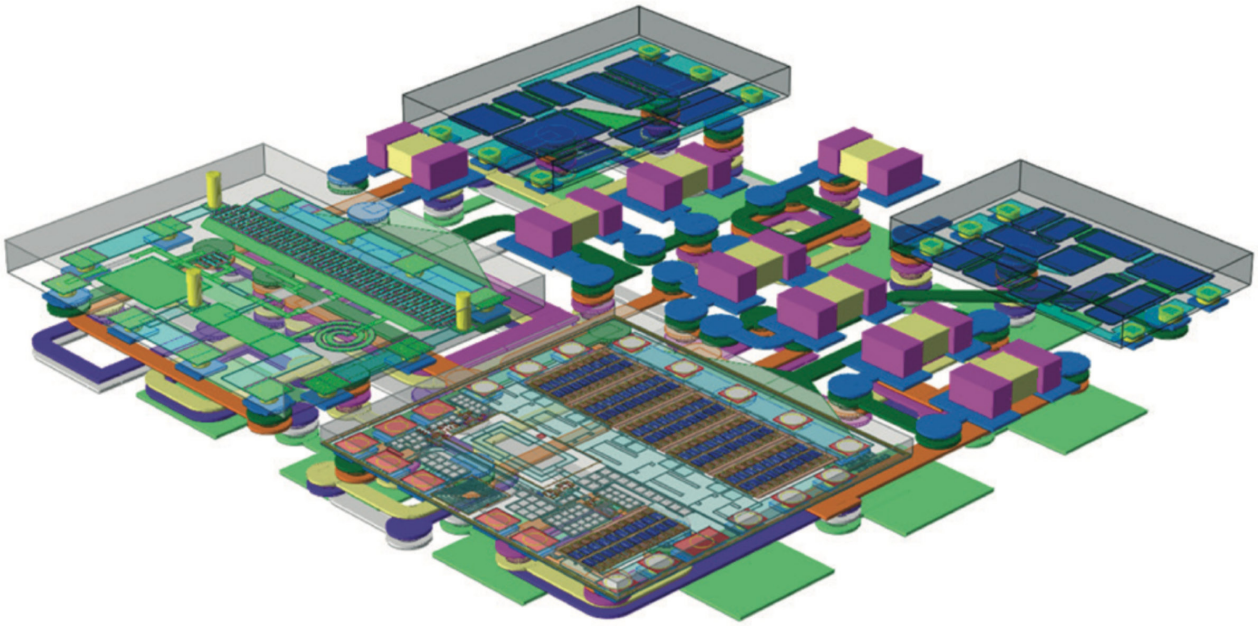


Figure 7: RF module design flows support laminate (PCB) design and integration of MMICs, RFICs, BAW/SAW filters, and other surface-mount technology (SMT) components

A large percentage of RFIC intellectual property (IP) has been and continues to be developed in the Cadence Virtuoso® environment. Consequently, a comprehensive module design flow must provide RFIC designers with laminate (electrical design) details and laminate (PCB) designers with the electrical details (S-parameters, simulation-ready netlist or behavioral models) of the RFIC. Therefore, the design tool should accommodate the designers' need depending on the focus of the individual design task or particular integration challenge of the module project. Interoperability between tools is necessary to the extent that design information needs to be shared between designers.

Recently, Cadence launched the Virtuoso RF Solution, supporting the design of RF modules and RFICs with passive-device modeling made possible through the integration of AWR software, specifically AXIEM 3D planar EM simulator, within the Virtuoso System Design Platform.

Note - Cadence provides multiple specialized EM solvers, including the Cadence EMX® Planar 3D Solver for Silicon IC component/layout modeling and the Clarity 3D FEM/FDTD Solver for large-scale system analysis/verification.

This approach provides seamless integration between the IC and package substrate design teams supporting the design of modules featuring off-chip devices and multiple ICs based on differing PDKs. Module complexity drives the need to integrate more powerful layout/circuit management, simulation tools for ultra-large networks, and EM simulation with the ability to incorporate the impact of physical design on electrical performance into a highly automated design flow that reduces potential design failures.

Module designs have many moving parts and the RF sections require support from specialized automated simulation technologies such as load-pull analysis, harmonic-balance simulation, and circuit envelope for nonlinear devices, as well as design aids that accelerate the initial stages of circuit development and physical realization.

Synthesis and Embedded Antennas

Modules targeting 5G and IoT devices may need to offer embedded antenna solutions optimized for performance, cost, and size. EM tools from Cadence let designers develop custom embedded antennas and antenna arrays while ensuring that they are properly integrated with minimal interference to other parts of the system and are adequately matched to the transceiver impedance.

With the network synthesis wizard option available in the AWR Microwave Office software, engineers can easily implement a suitable matching network for the desired single-, multi-, or broad-band operations. This ensures maximum power delivered to the antenna for devices that require low power consumption without sacrificing range (coverage).

Engineers from Fractus Antennas, a leading manufacturer of tunable surface mount antennas, designed a multi-band active antenna tuner for a battery-operated prototyping platform for cellular IoT (cIoT) from Nordic Semiconductor. The cIoT module and prototyping board offer six bands of operation including GPS, supported by the antenna and the band-specific impedance matching networks developed by Fractus Antenna. The RF section of the board includes the IoT module from Nordic Semiconductor, two single-pole-eight-throw switches from Qorvo that allow the signal to pass through different matching circuits dependent on the desired operating band, and the Fractus Antenna (Figure 8).

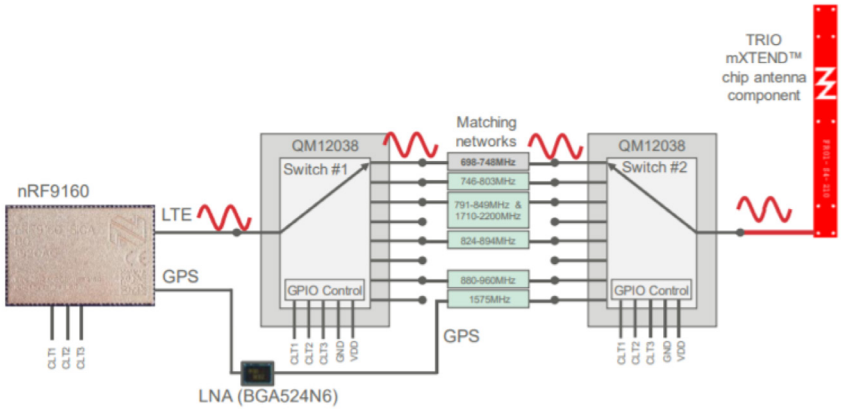


Figure 8: Block diagram of cIoT module and active antenna tuner for six-band operations

The goal-driven network synthesis tool creates matching networks according to simulation measurements and user-specified performance goals such as small-signal return loss or nonlinear amplifier behavior (Pout, PAE, etc.) from load-pull performance contours. The synthesis engine uses a proprietary, genetic optimization algorithm and heuristics to identify candidate matching networks, addressing challenging impedance matching problems across multiple performance goals and frequency bands.

The RF designer specifies which component types, such as an inductor, capacitor, and transmission line, can appear in a given series or shunt configuration, thereby managing the topology as well as allowing the user to constrain component parameter values to reflect manufacturing tolerances. This capability accelerates impedance matching, providing RF engineers with a greater number of viable network candidates through rapid design space exploration (Figure 9).

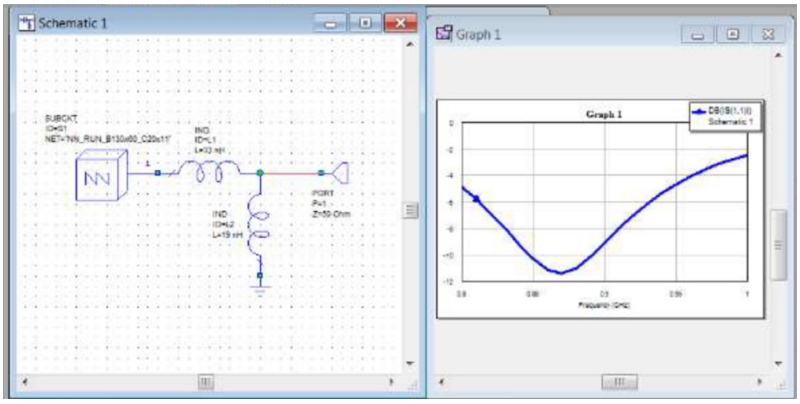


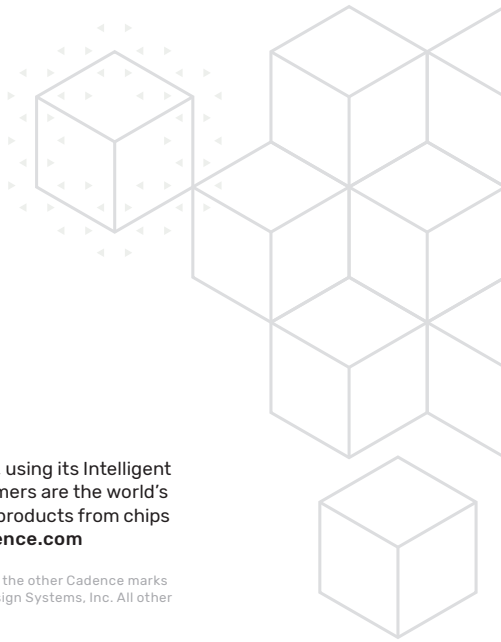
Figure 9: Simple two-element (ideal inductors) matching circuit and resulting return loss of matched antenna component

Synthesized networks can be based on models from the AWR Microwave Office ideal parts library, vendor component libraries or foundry PDKs, and microstrip transmission lines using substrate definitions in the given project. The user can then specify which candidate networks to import directly into the AWR Microwave Office project. Engineers at Fractus Antenna use network synthesis to achieve the desired in-band return loss for their surface mount antenna model, which is available as a component model (S-parameters) in the standard AWR Microwave Office vendor library. The designer places this antenna component into a schematic subcircuit and develops an impedance matching network to optimize the sub-circuits return loss, thereby maximizing antenna efficiency, the ratio of power radiated to power supplied to the antenna.

Conclusion

The rapid evolution of wireless connectivity has driven continual consumer thirst for more data throughput and reduced time to market. The smaller form factor and integrated functionality offered by RF modules make them an attractive choice for designers looking for wireless connectivity from a drop-in component. For device manufacturers, modules represent an opportunity to become more competitive with devices that offer more capabilities, differentiation from competitors, and potentially larger cost margins.

To reap these benefits, companies will require multi-disciplinary engineering teams working together using a well-organized design flow that supports advanced design management, model libraries, integrated circuit, system, and EM co-simulation, and interoperability with CAD layout and multi-physics point tools. Fortunately, the design software and supporting test and measurement solutions needed to support advanced module development are available and continue to evolve in step with the products they help bring to life.



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