SUCCESS **STORY**

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Qorvo and Cadence

1-8GHz GaN Distributed PA MMIC with Novel Trifilar Transformer Utilizing AWR Software

Key Challenges

Many modern microwave electronic systems specify amplifiers with high output power, wide bandwidth, and high efficiency. Until recently, most wideband high-power amplifier (PA) solutions have relied on vacuum electronics-based technologies. Recent work, however, shows steady progress in realizing high-power, high-frequency, wideband amplifiers utilizing gallium nitride (GaN) monolithic microwave integrated circuit (MMIC) technology that operates from near DC up to 7GHz. Qorvo designers were challenged to meet the requirements for an amplifier with high output power, wide bandwidth, and high efficiency by designing a 1-8GHz PA MMIC fabricated with a 0.15µm GaN process technology. The process featured a 100µm-thick silicon carbide (SiC) substrate and compact transistor layouts with individual source grounding vias (ISVs). The design utilized a nonuniform distributed PA (NDPA) topology with a novel trifilar connected output transformer (Figure 1).

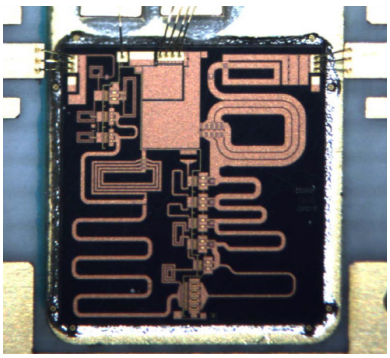

Figure 1: Photograph of the manufactured MMIC mounted to a test fixture, die dimensions are 3.25 x 3.50mm²

Application

- MMIC Power Amplifier

Software

- Cadence® AWR Design Environment® Software Portfolio, including:
  - Cadence AWR® Microwave Office® software
  - Cadence AWR AXIEM® 3D planar analysis

Benefits

- Speed of simulations
- Co-simulation ability
- Complete solution

Design goals for the PA MMIC were: 1-8GHz bandwidth, >25dB small signal gain, 10W saturated output power, and power-added efficiency (PAE) exceeding 30%. A small-signal gain goal in excess of 25dB required at least two amplification stages. To meet the bandwidth requirement, the NDPA topology was adopted [4,5]. The output power realized with the NDPA approach was proportional to V_d^2/R_L where V_d is the power supply voltage and R_L is the load impedance that the amplifier was driving.

Output power could be increased by designing the amplifier to operate with a higher power supply voltage and/or a lower load impedance. Increasing the supply voltage could be problematic, as the transistor technology might not be able to operate reliably at higher voltage and the drain transmission line impedances could become unrealizably high. Therefore, to increase output power, a novel monolithic trifilar coupled-line transformer design (patent pending) was used to reduce the 50Ω load impedance to about 25Ω. An idealized schematic for the transformer connected in the "bootstrap" configuration is shown in Figure 2.

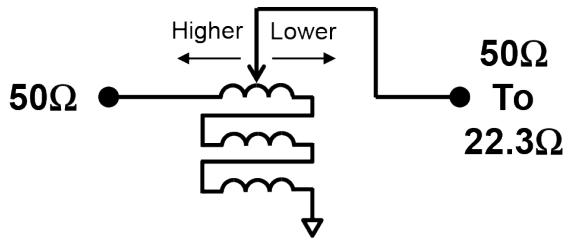

Figure 2: Triflar transformer for up to a 2.25:1 transformation ratio

Solution

The Qorvo design team chose AWR Microwave Office circuit design software for this complex task. The two-stage amplifier demonstrated 9.3-13.1W of output power over a 1-8GHz bandwidth with greater than 29% associated PAE. Theoretically, transformation ratios up to 2.25:1 are possible depending on the location of the output tap. Due to physical limitations regarding the location of the low impedance side tap, the microstrip implementation produced a ratio closer to 2:1.

EM simulations performed on the transformer using the AWR AXIEM 3D planar EM simulator suggested that an 8:1 bandwidth could be supported with this approach. For the NDPA application, the ground connection was replaced by a bypass capacitor providing a drain bias injection port. This mitigated the need for a wideband high-current drain bias choke, which could negatively impact the performance and bandwidth of the amplifier. The layout and EM simulation results are shown in Figure 3. The predicted loss varies between 0.28dB and 1.26dB over the 1-8GHz operating band.

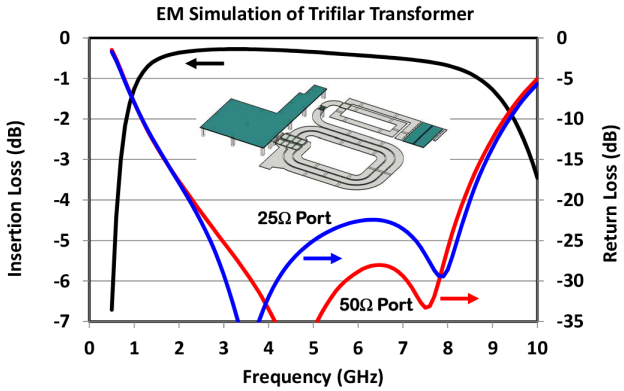

Figure 3: AWR AXIEM EM simulation results for the trifilar transformer

Taking into consideration the frequency range, available transistor cells, transmission-line current handling, and realizable characteristic impedances, a six-cell NDPA driving a 25Ω load was selected for the output stage of the amplifier. The output stage also utilized nonuniform transistor cell sizes such that the optimum transmission line impedances were realizable on a 100µm-thick SiC substrate. The driver stage topology was a three-cell NDPA driving a 50Ω load. Both stages operated at equal V_g and current density such that the first- and second-stage gate, as well as first- and second-stage drain bias taps, could be connected together. Hence, the circuit had single-gate and drain-bond pads.

The performance of the PA was compared to recently published GaN MMIC PA benchmarks. The measured performance of the amplifier MMIC compared favorably with results for bandwidth, gain, die size, and efficiency.

Summary

The Qorvo design team chose Cadence's AWR Design Environment software for the design of this 1-8GHz GaN distributed PA MMIC utilizing a novel trifilar transformer because of the powerful circuit design capabilities combined with integrated AWR AXIEM EM simulation.