

Isolating and Characterizing Critical Traces Using EM Analysis

The Cadence® AWR® AXIEM® electromagnetic (EM) simulator is integrated with the Cadence Virtuoso® RF Solution, providing designers with an integrated circuit (IC) and package/module design flow that improves productivity by eliminating the design failures caused by the manual translation of data. A single golden schematic is used for simulation, layout versus schematic (LVS), and EM analysis and verification, without the need for unique schematics for EM and LVS.

Design Overview

This application note examines how the combined Virtuoso RF Solution/AWR AXIEM EM simulator enables designers to perform EM analysis to isolate and characterize critical traces within the complex multi-layer configurations of today's modern applications.



Why EM Simulation for Analog Silicon Design?

In the traditional III-V flow for gallium arsenide (GaAs) and gallium nitride (GaN) chips, the nets are included as distributed line models, and EM simulation is used to check the models and the coupling between elements. In the traditional analog flow for silicon chips, the nets are treated as parasitics and modeled as lumped elements. EM simulation is useful in silicon for distributed structures such as inductors and for coupling between elements such as multiple inductors, pads, and bond wires. Other common cases where EM simulation is needed include modeling ground meshes, ground issues, or frequency dependent loss in interconnects.

Parasitic effects not included in models become more important in silicon as the frequency of operation gets higher. The electrical length is longer, coupling is more likely, imperfect ground is more of an issue, and the loss changes with the skin depth in the metal. Modules and board transitions, as well as bond wires and ball-grid arrays become more of an important issue.

An important difference between EM simulators and the more traditional parasitic net extraction tools used in RFICs is that, in EM simulators, ground is an important issue because they need a ground definition for S-parameters. In addition, ports need a port ground definition in terms of from where the current comes and what the port voltage reference is. Thus, the designer must have a good awareness of the ground location for an EM simulation.



Figure 1: Processed wafer with integrated passive elements

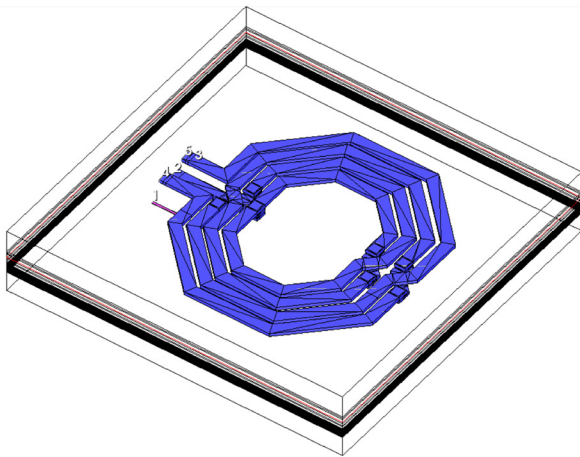
Using the AWR AXIEM Simulator with Virtuoso RF Solution

The AWR AXIEM EM simulator within the AWR Microwave Office® circuit design software is a best-in-class planar, open-boundary 3D planar engine that solves for currents on horizontal metal traces and vertical vias. The metal is drawn on planar dielectric layers, as is commonly used in silicon chips, boards, and packages. The AWR AXIEM simulator generates S-parameter and offers flexible port options, thick or thin metal mesh, shape simplification rules, and a high-capacity, fast-computational engine.

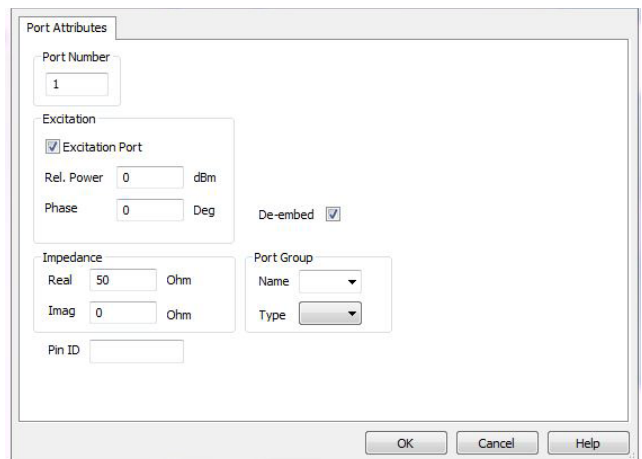
Prior to the Virtuoso RF Solution integration of the AWR AXIEM EM solver, users of both tools relied upon manual integration, namely exporting and importing the layout between environments. Additional manual steps were necessary, including setting up ports, simulation settings, generating S-parameters, and then exporting the results into a circuit simulator, either by exporting back to Virtuoso RF Solution or importing the Spectre® Simulation Platform netlist and running the AWR APLAC® circuit simulator within the AWR Microwave Office software. This manual flow is illustrated in simplistic fashion in Figure 1. Step 1 shows a spiral inductor being imported from the Virtuoso RF Solution into the AWR AXIEM simulator. Step 2 shows ports and simulation settings being added. Step 3 shows the S-parameters being generated. Step 4 shows the final resulting S-parameters that are used in a circuit simulator

This flow involved a great deal of manual manipulation of layouts, EM simulator setup, and manual export of data to circuit simulators that is both time-consuming and error prone. This manual flow becomes more difficult when one considers the designer is normally interested in several elements and nets, for example coupling between inductors.

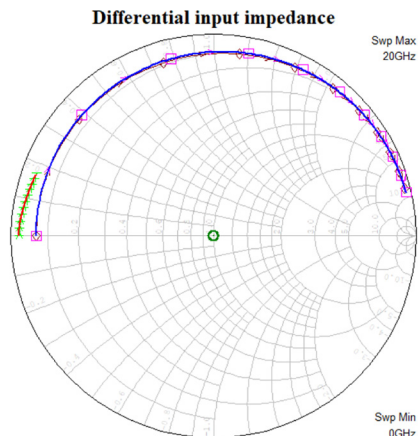
Step 1. Import layout from Virtuoso RF Solution into the AWR Design Environment



Step 2. Set up ports and simulation settings for the AWR AXIEM simulator



Step 3. Generate S-parameters



Step 4. Run circuit simulator

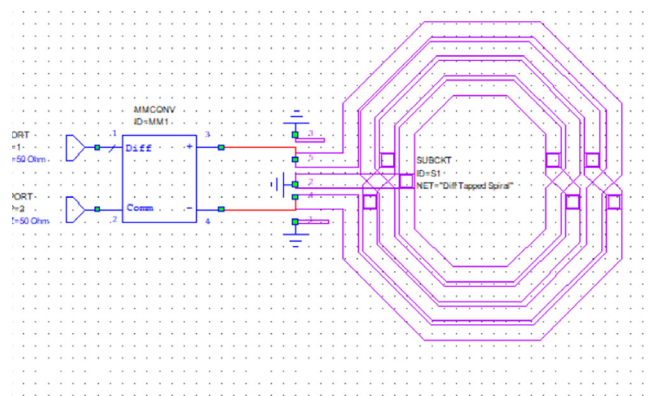


Figure 2: The traditional AWR AXIEM flow in AWR Microwave Office software for use with Virtuoso RF Solution

Integrated AWR AXIEM Solver/Virtuoso RF Flow

The integrated AWR AXIEM EM solver within the Cadence IC/system-in-package (SiP) flow for layout of silicon ICs provides design optimization and layout verification within a single schematic. Figure 2 shows the golden schematic flow for an example design of a voltage-controlled oscillator (VCO).

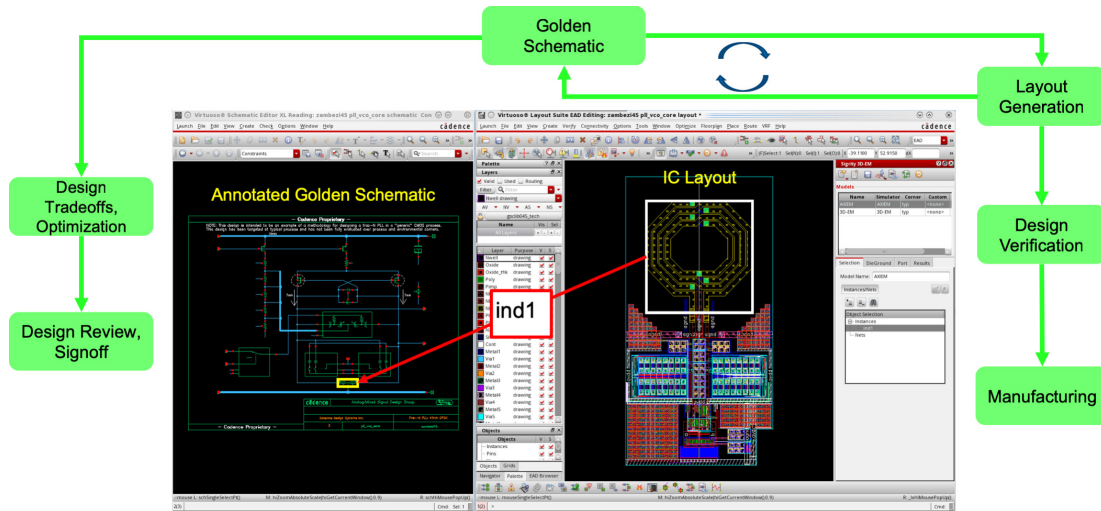


Figure 3: Golden schematic flow

The left side of Figure 2 shows the schematic of the VCO and the right side shows the layout. Traditionally, layout and schematic are loosely coupled in the Virtuoso environment. The golden schematic couples much more tightly with the layout, reducing error and saving time. The spiral in the layout has a corresponding model in the schematic, as is shown by the arrow. Later it will show how the model can be replaced by S-parameter results from the AWR AXIEM software, enabling the layout and schematic to stay connected.

Figure 3 shows the golden schematic on the left and the AWR AXIEM spiral layout in Virtuoso RF Solution. The model assistant is docked on the right side of the layout window.

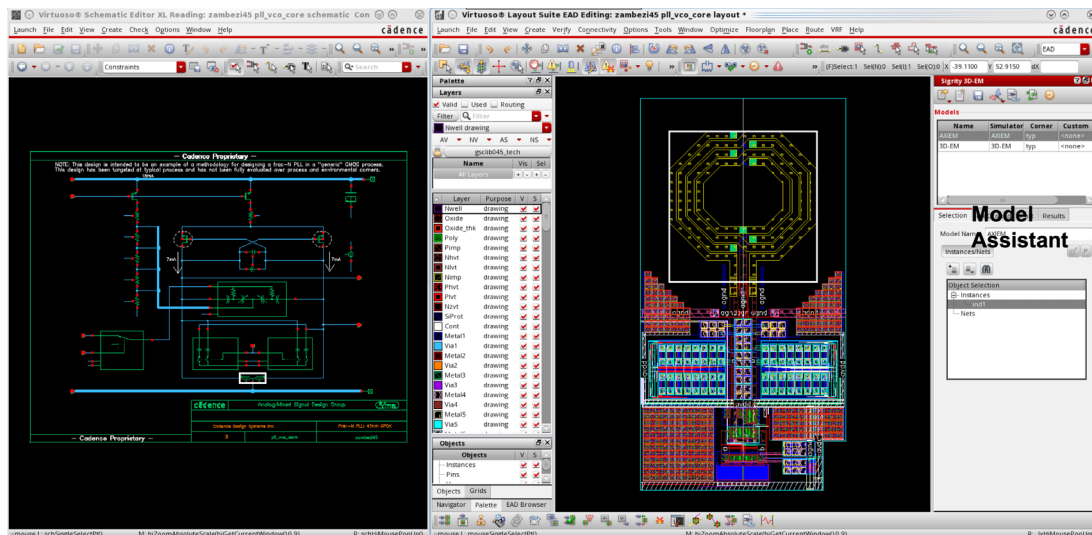


Figure 4: AWR AXIEM model in Virtuoso RF Solution

The white box drawn around the spiral is the limit of the layout that is extracted to AWR AXIEM software, in this case the spiral and feed lines. Ports are automatically attached to the feed lines once the layout is placed in the AWR AXIEM simulator. There is no need for the designer to add ports, they are added wherever the feed lines hit the simulation boundary in the Virtuoso layout. The box on the far right is the model assistant. It enables the designer to set the AWR AXIEM simulator nets and various control options.

The Process Setup in Virtuoso RF Solution

For it to work properly, the AWR AXIEM software requires that the STACKUP properties, material properties, and various simulation settings be configured. These settings reside in the Virtuoso modeling assistant. Figure 4 shows the process design kit (PDK) setup in the modeling assistant with several representative menus, for example, dielectric and via properties are shown in the middle picture, where the silicon material properties and layer thicknesses are listed. If desired, process variations and corner cases can be included.

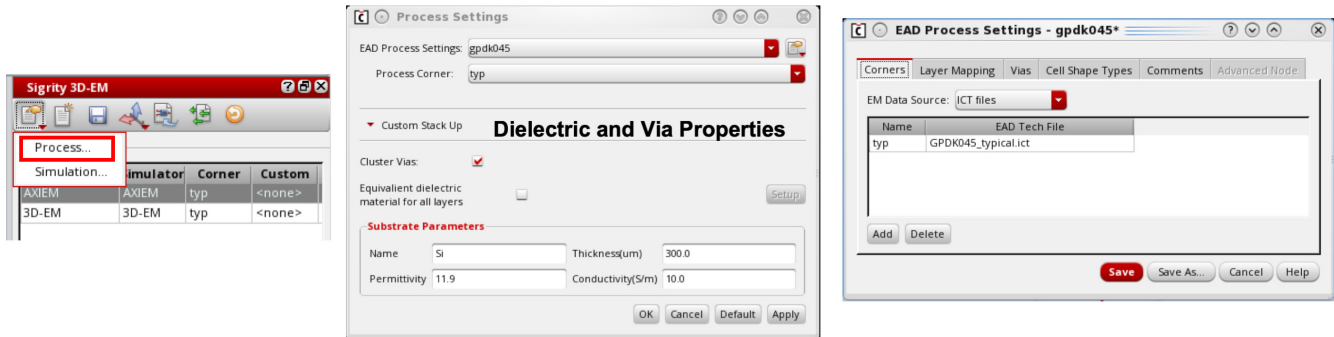


Figure 5: PDK setup in the Virtuoso modeling assistant

There are some preview and diagnostic capabilities built into the AWR AXIEM integration. Figure 5 illustrates how the mesh can quickly be previewed in the AWR AXIEM model to understand the density that will be used and the accuracy level. Note that, in this example, the mesh density is relatively sparse. There is a nice 3D view of the mesh on the surface of the inductor. Thick metal with side walls is used to capture the coupling. The meshing density can be adjusted in the AWR AXIEM setup menus if desired. For example, a Q calculation of a spiral inductor might require a higher mesh density than simple S-parameter calculations.

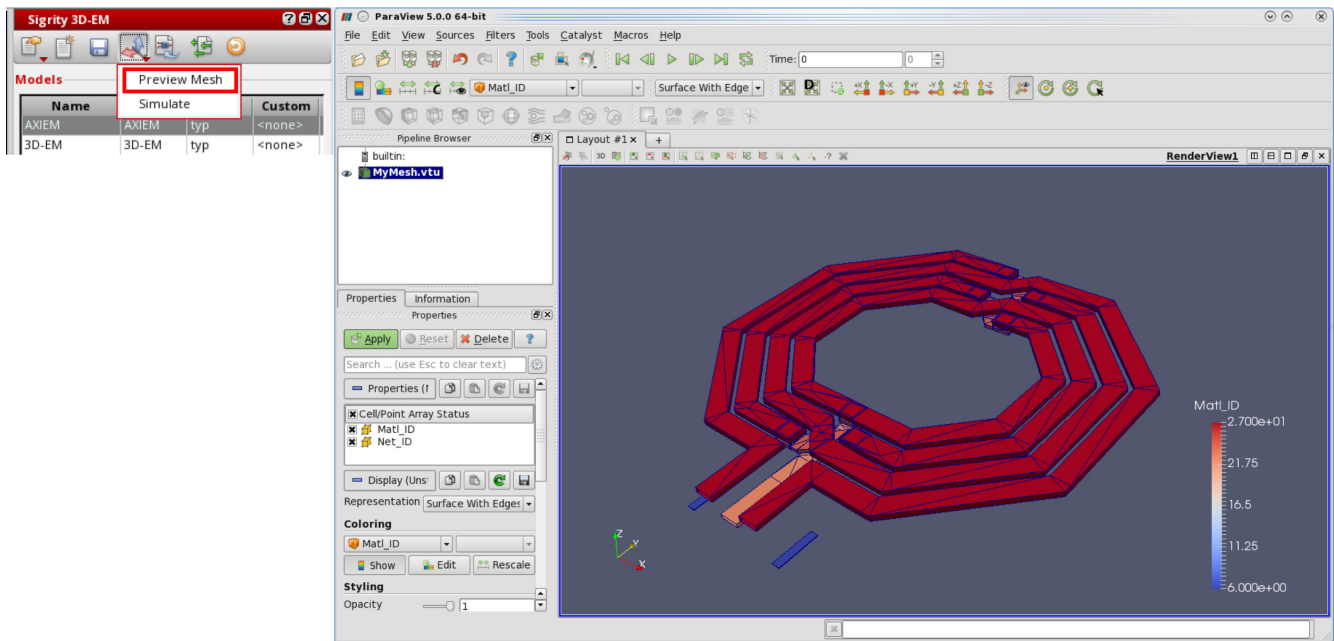


Figure 6: Mesh preview in the AWR AXIEM simulator

The log file is available to view once the project is completed, shown in Figure 6. The log file enables the designer to obtain useful information about the simulation such as the mesh size, the number of frequency points required, simulation time, and more.

```

-----
# of Unknowns = 1869
# of Nets = 3
# of Ports = 5
- Calculating DC solution
----- Candidate Solver Type : Direct (low frequency)
----- Calculating Greens Functions -----
----- Matrix Setup -----
- Elapsed time ( 00:00:14.27 )
----- Matrix Solve -----
- Elapsed time ( 00:00:0.01 )
----- Simulating DeEmbedding Standards -----
- Port 1, 2, 3, 4, 5: not de-embedded
- Elapsed time ( 00:00:0.00 )
- Solution @ DC - Elapsed time ( 00:00:14.29 )
- Calculating Solution @ 10 GHz
----- Candidate Solver Type : Direct (high frequency)
----- Calculating Greens Functions -----
----- Matrix Setup -----
- Elapsed time ( 00:00:11.28 )
----- Matrix Solve -----
- Elapsed time ( 00:00:0.01 )
----- Simulating DeEmbedding Standards -----
    
```

Figure 7: The AWR AXIEM log file is available to view

The goal of the Virtuoso RF Solution/AWR AXIEM EM solver flow is to enable the designer to stay within Virtuoso RF Solution environment and yet gain access to S-parameters with full-wave accuracy. After the S-parameters are generated, the model in the golden schematic is replaced with the S-parameter results. The extracted view is then created, and the model in the schematic is replaced with the S-parameters. Figure 7 illustrates the control menus for creating the extracted view.

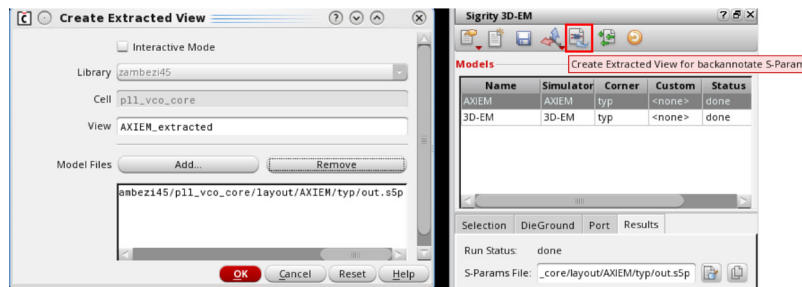


Figure 8: The extracted view is created, replacing the model with the S-parameters

This flow enables the designer to maintain the original layout and golden schematic. Notice in Figure 8 that the pin count and net names are correct after extraction to the schematic. This is important for checking the circuit, especially when running LVS, which is required for all silicon designs before the chip can be manufactured in order to ensure the layout and the schematic represent the same design. Otherwise, the layout could contain errors, such as critical nets that could be shorted, that might not be noticed by the layout team, resulting in disastrous consequences. The flow keeps the schematic and the layout synchronized together, thereby not breaking the LVS flow.

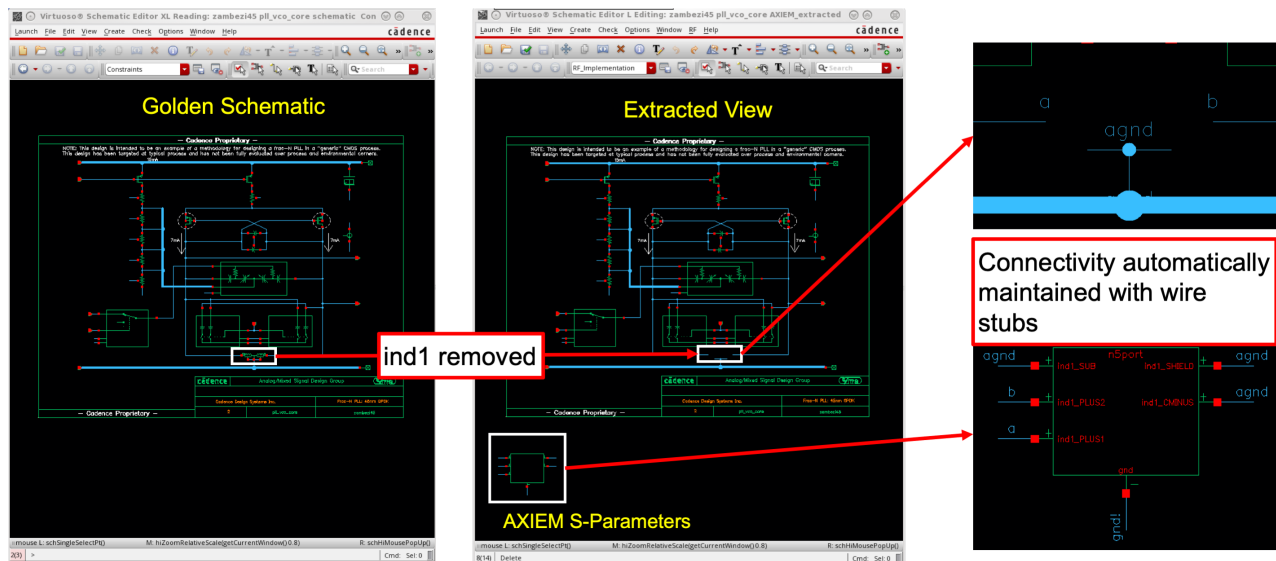


Figure 9: Extracted view and golden schematic with AWR AXIEM S-parameters

Figure 9 illustrates the simulation results for the VCO. The curves illustrate the oscillation frequency in GHz (vertical axis) versus voltage (horizontal axis). The red curve shows the case where only models in the Spectre circuit simulator are used. The blue curve shows the results when parasitics are added for the nets using a parasitic extractor. The green curve shows the AWR AXIEM EM simulation results used for the spiral inductor instead of a model, demonstrating that the more accurate EM representation of the spiral's performance is required, as opposed to using the built-in model.

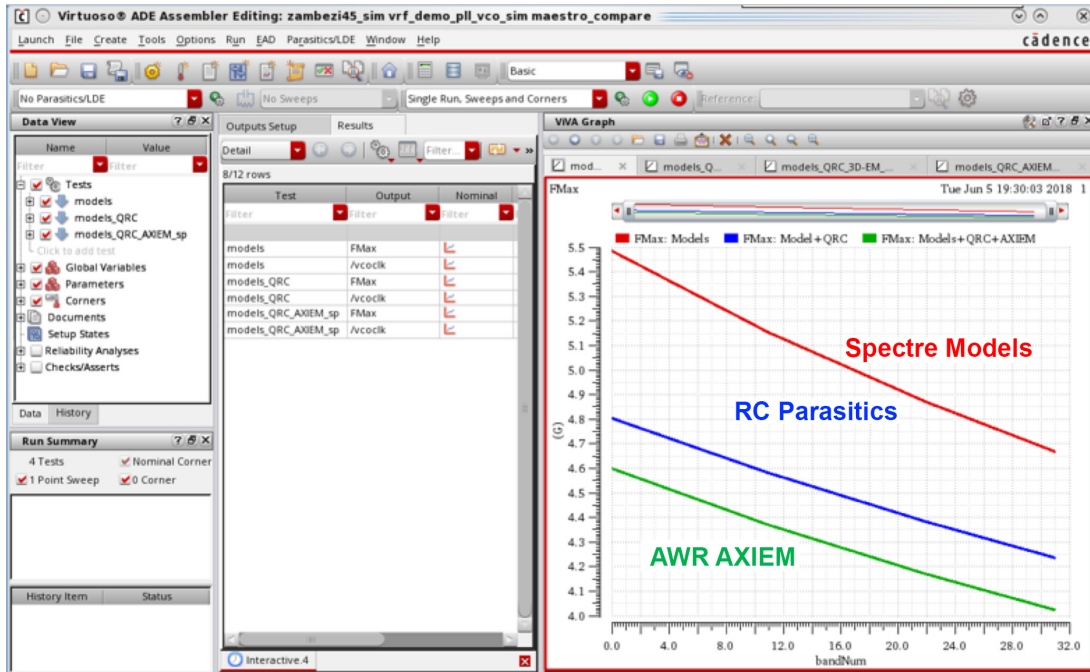


Figure 10: Simulation results for VCO

Conclusion

As frequencies of operation push upward, EM simulators are becoming more and more critical for RFIC designers. Distributed effects, such as inductors, become important, as do frequency-dependent effects such as resistance. Grounding issues become critical and must be accounted for in simulations. Structures such as meshed ground planes and rings need to be EM simulated to ensure they are modeled correctly. Coupling effects between various components, which are not included in models, become an issue and must be EM simulated.

The AWR AXIEM EM solver/Virtuoso RF Solution design flow seamlessly integrates the process of accounting for EM effects within a circuit design project by enabling a single environment for simulation, LVS, and EM analysis and verification, without the need for unique schematics for EM and LVS. This flow reduces the chance of error and cuts down on design time and verification cycles.



Cadence is a pivotal leader in electronic design and computational expertise, using its Intelligent System Design strategy to turn design concepts into reality. Cadence customers are the world's most creative and innovative companies, delivering extraordinary electronic products from chips to boards to systems for the most dynamic market applications. www.cadence.com

© 2020 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. All other trademarks are the property of their respective owners. 14720 07/20 SA/RA/AN-X-CDNC-RFIC/PDF