WHITE **PAPER**

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# The Importance of EM Analysis for RF/ Microwave Design

## Featuring Cadence AWR Software

This design flow conundrum is one that Cadence works hard to mitigate. The problem of electromagnetic (EM) concurrency and co-design within an overall circuit flow was voiced by customers, and, in response, the R&D team created the Cadence® AWR Design Environment® platform's EXTRACT flow for schematic-driven EM analysis. With an EXTRACT element on the schematic, the design is ready to automatically create EM documents from the schematic's layout and then seamlessly reintegrate the results back into the schematic as part of any circuit simulation, optimization, and/or tuning step. The process is easy to use and incorporates some very complex, innovative technology to solve a host of design issues related to the inclusion of EM analysis into the overall design flow.

The EXTRACT flow makes the designer's job easier by enabling the creation and control of EM documents from the electrical schematic so that they become an integral part of any simulation, tuning, or optimization process. This obsoletes the manual process of either updating EM structures or, more painfully, reintegrating multi-port S-parameter files back into the schematic from the EM analysis. The EXTRACT flow is useful for monolithic microwave integrated circuit (MMIC), RFIC, RF module, and RF PCB design and can be used with any solver or circuit extractor through the AWR® EM Socket open standard interface. This white paper overviews the EXTRACT flow and the EXTRACT element, or block, that goes on the schematic when speaking of the overall flow that the element enables.

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## Overview

Modern RF/microwave design flows make extensive use of EM analysis in many ways, and its co-existence and concurrency with circuit design and analysis cannot be undervalued. Prior to the circuit design and especially in larger designs, EM tools are used to create model library parts such as inductors, transitions, and antennas. While these parts are fairly self-contained, they must ultimately be integrated into the overall design, where, at the very least, they must be connected to the rest of the circuit or, in a more complex design, be coupled to it. During both the early and later stages of a design, engineers will switch from circuit-based models to EM analysis of critical interconnects to better understand couplings and achieve greater accuracy. EM analysis is used again before the design goes to manufacturing, so that the metal in the design can be analyzed one more time to verify circuit performance alongside design rule check (DRC), layout versus schematic (LVS), and even design for manufacturability (DFM).

An overriding issue common to all these applications is that at some level the EM solver must interact with other software tools. The raw materials that are input to the solver are geometries or structures but are no more than a layout with electrical material properties for all the layers. At the other end of the process, the EM solver produces S-parameters or some other linear model representation. Some solvers can output SPICE netlists directly, which must be integrated with the rest of the design in a circuit simulator. Achieving all of this successfully has historically been a less-than-seamless chore of duplicating geometries or exporting and importing structures from the design or layout tool to the solver. The results must then be imported into the circuit simulator. While much effort has gone into automation of moving GDSII or DXF files from layout tools to the solver, most of these tools lack real-time integration and have a "batch mode" feel, as though things were "auto-magically" going on behind the scenes. There has also been little help in integrating the results back into the schematic, especially when using the solver in a verification mode. Dozens if not hundreds of ports are involved in final verification, and it is often left to the designer to put together a schematic that properly reattaches each port in the solver's results to the proper pins of the remaining components. This must be performed without error, and quickly, in order to get the design to market quickly.

## How the EXTRACT Flow Works

The EXTRACT flow starts and ends with the schematic (Figure 1). When a simulation is requested by any means, even through tuning and optimization, the EXTRACT flow finds the elements in the schematic and on the layout that has been assigned to a particular EXTRACT block, and then copies the layout representation of those elements to the EM document specified on the EXTRACT block. The EM document is set up according to the data on the EXTRACT block: type of ports, frequencies for the enclosure, dimensions and gridding, which solver to use, and any other options required of the EM solver. After the EM solver runs, the circuit simulator is notified and automatically uses the solver results in place of the models associated with the schematic elements tied to the EXTRACT block. If the simulation was initiated from within an optimization loop or by sliding a tuner control, the entire EXTRACT flow will be re-executed while any changes to the elements associated with the EXTRACT flow are also under the control of the optimization or tuning process. If the elements associated with the EXTRACT block are not changed by tuning or optimization, then no changes to the EM document will be made and the EM solver will not be rerun.

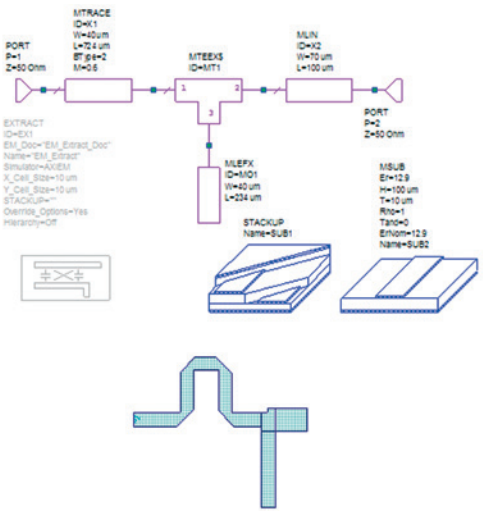


*Figure 1: Matching network schematic and layout with the EXTRACT flow disabled*

Two elements are needed to start the EXTRACT flow: an EXTRACT block and a STACKUP element. The latter normally comes as part of a process design kit (PDK) and is pre-qualified by the foundry. Custom STACKUPs can be created either by editing the foundry STACKUP or by starting from scratch by adding materials and associating them with the layers in the layout layer process file (LPF) and then building a custom arrangement of these layers using a graphical user interface (GUI) in the STACKUP's parameters dialog box.

The EXTRACT block itself has several options that determine how it behaves relative to the schematic on which it is placed, the EM structure it creates, and the STACKUP it references. The block defines how the EXTRACT flow should work in hierarchy, and if it is disabled, it reverts any elements associated with it back to their circuit model. For AWR Intelligent Nets (iNets), this would be a short circuit. Parameters control EM document updating and initialization, enclosure dimensions and oversizing, and which solver to use. A dynamic tab within the EXTRACT dialog (Figure 2) displays the solver options, which are reconfigured whenever the EXTRACT flow's solver parameters are changed.

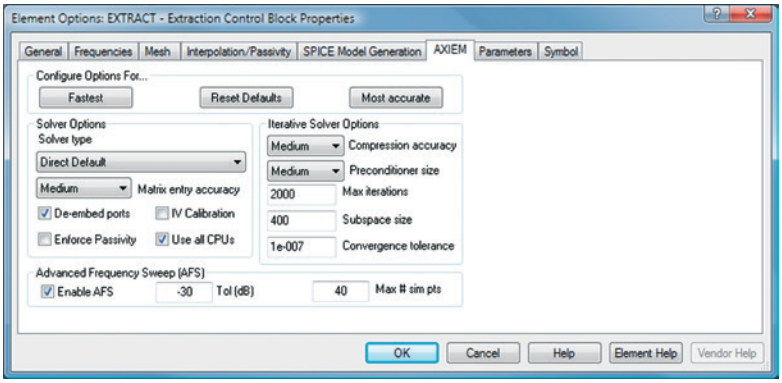


*Figure 2: The EXTRACT block's solver-specific dialog tab, shown here for AWR AXIEM analysis, allows the user to directly specify details of the analysis and control them from the schematic*

Designers can switch from the AWR's automatic circuit extraction (ACE) tool to Sonnet, to Cadence's AWR AXIEM® 3D planar EM analysis, to any combination thereof, and see all the respective options from within the EXTRACT element's parameter dialog. Finally, the STACKUP is specified from the EXTRACT flow to be used for interpreting the layout layer's material parameters and how the layers themselves map to the EM analysis. Different STACKUPs are sometimes desirable in order to go from a very simple analysis in which perfect grounds may be assumed for microstrip and stripline modeling, to those where ground may not be apparent at all.

Once the EXTRACT block is on the schematic, elements and iNets can be associated with it. To associate an element or a group of elements, or an iNet, or group of iNets with the EXTRACT block, the user simultaneously selects one or more of these items, and then proceeds to the Model Options tab in the parameter dialog (Figure 3). The EXTRACT flow is enabled with a check box and the specific EXTRACT block to use is identified with a text box.

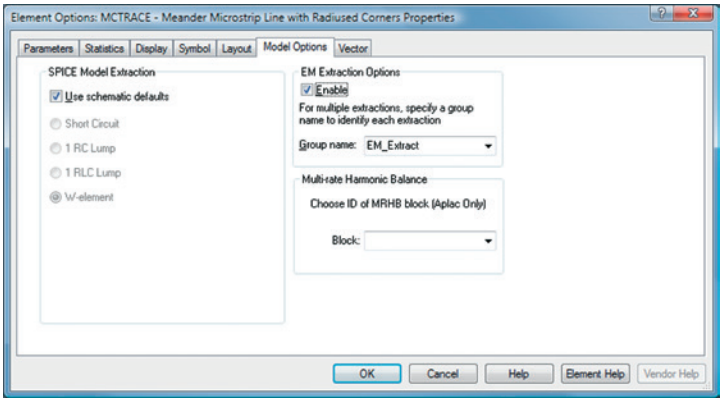


*Figure 3: The Model Options tab within the parameter dialog box for schematic elements specifies the elements' inclusion into an extraction by the name of the EXTRACT block*

As an illustration of this process, refer back to the simple open-stub matching network shown in Figure 1. The MTRACE element at Port 1 is allowed to meander the line, and although MTRACE captures the alternating line segments and bends as MLINs and MBENDs respectively, it does not couple the parallel segments to each other, nor to the MTEE. In Figure 4, the EXTRACT block is enabled, and by using the STACKUP to define the material properties and physical dimensions of all the dielectrics and metals, the layout is automatically transferred to the EM document EM_Extract (Figure 4). It is then run/analyzed using the AWR AXIEM analysis and the results are used in place of the elements between the two ports. This is all performed automatically, and immediately, whether the designer simulates, optimizes, tunes, or performs yield analysis. Figure 5 shows the difference for S21 for this matching network with and without the EXTRACT flow.

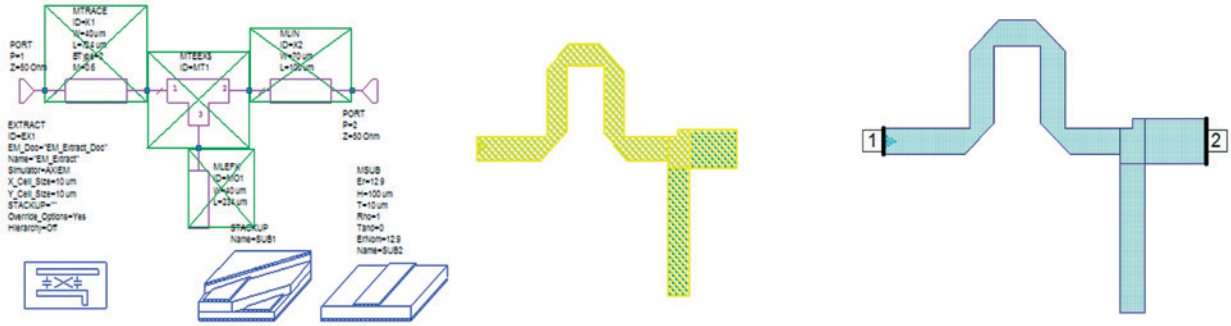


*Figure 4: A matching network schematic with the EXTRACT flow enabled showing associated elements (left), and the STACKUP element controls the mapping of the physical layers in the layout to the electrical properties for the analysis and EM document automatically created under simulation control of the schematic using EXTRACT and STACKUP blocks (right)*

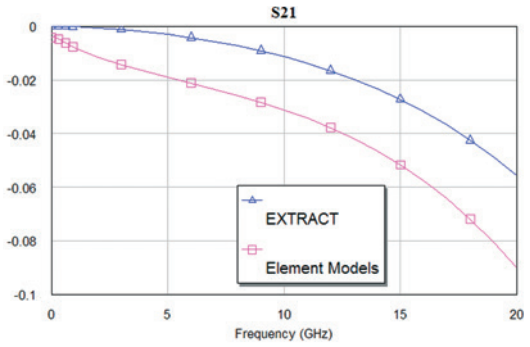


*Figure 5: Results of matching network EXTRACT flows compared to circuit models for the same element*

To create an EXTRACT EM document without simulating, the user simply right-clicks on either the EXTRACT block in the schematic or the schematic on the project pallet and selects *Add Extraction*. This makes it possible to make sure that the proper material-to-layer mappings are in the STACKUP, that the sizing of deembedding planes (if necessary) is correct, and, most importantly, that the designer has chosen a meshing grid that provides the desired simulation speed and accuracy of results metric.

Note: It is also possible to include layout-only components in the EXTRACT flow, such as an element that only appears in the layout, which might occur if there are floods for power or ground, via fences for isolation, or mechanical structures that have no direct electrical representation in the schematic. To do so, select the element in the layout, right-click *Shape Properties*, enable the EXTRACT checkbox, and specify the name of the EXTRACT block (Figure 6).

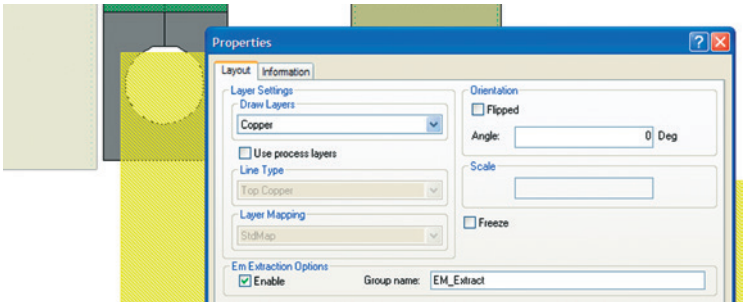


*Figure 6: Arbitrary shapes in layout, not associated with an element or iNet in the schematic, can be added to EXTRACT groups, such as here, a ground fill is added to the EXTRACT flow in a 7GHz PCB power amplifier*

The EXTRACT block itself controls how hierarchy is handled. This is especially important if the designer has separate EXTRACT blocks at lower levels of the design, which might be used to develop a self-contained model for a particularly complex subcircuit, such as a filter or coupler. Early in the design flow, it may not be desirable to consider the filter or coupler in an EXTRACT block of the metal connecting the filter to other parts of the circuit. However, in later stages of the design, it may be essential to do just that. By using the hierarchy parameter on a lower level block, the EXTRACT flow can be instructed to include the block in higher-level EXTRACT EM documents or to generate its own EM document.

There is no problem with having more than one EXTRACT block on the schematic for distinct EM solvers that do not couple. If input and output matching networks are electromagnetically isolated, they can be partitioned into two EXTRACT blocks. The circuit elements and layout structures in the input matching network would be enabled to go to one EXTRACT block and the output matching network circuit elements and layout structures would go to another EXTRACT block.

It is also possible to freeze an EM document created by an EXTRACT flow and continue to use the result, which is a powerful feature that allows EM structures to be "frozen" and worked on separately from the design as a whole. The EM solver can be optimized accordingly to the need for greater speed or accuracy from the simulation, or different EM solvers can be explored, all as a separate problem from the overall circuit and then reintegrate without having to re-enter data, move DXF or GDSII files, or cut-and-paste. This freeze option associated with a EXTRACT block is also useful for performing a separate study of the EM structure created by the EXTRACT flow— like creating a reusable, standalone part.

## Real-World MMIC Example

Perhaps the best way to understand and appreciate the elegance of the EXTRACT flow is through a real-world design. Designing a MMIC distributed amplifier requires a delicate balance between the cascaded input and output transmission lines for each section of the amplifier. Isolated, it is a simple task to obtain the correct input and output for each stage. When laid out within the confines of a space-constrained, cost-driven MMIC, any assumptions of the stages being electromagnetically independent must be revisited. The EXTRACT flow within an optimization loop is an ideal way to get closure on this critical aspect of the distributed amplifier design. This EXTRACT flow is one of the standard AWR Microwave Office® examples and takes advantage of several key features in the software.

Figure 7 shows the initial distributed amplifier design. The extracted EM document is seen in the upper left pane and the ACE analysis engine was chosen in lieu of traditional EM solvers so that the couplings considered in the analysis can be easily controlled to optimize the design. The arms of the input and output stages are modeled by separate instances of the same hierarchical, parameterized subcircuit. The subcircuits along with additional feed lines comprised of MLINs, routable MTRACEs, and iNets, can be combined together in a single EXTRACT flow to gather all of the interconnect couplings critical to this distributed amplifier's performance.

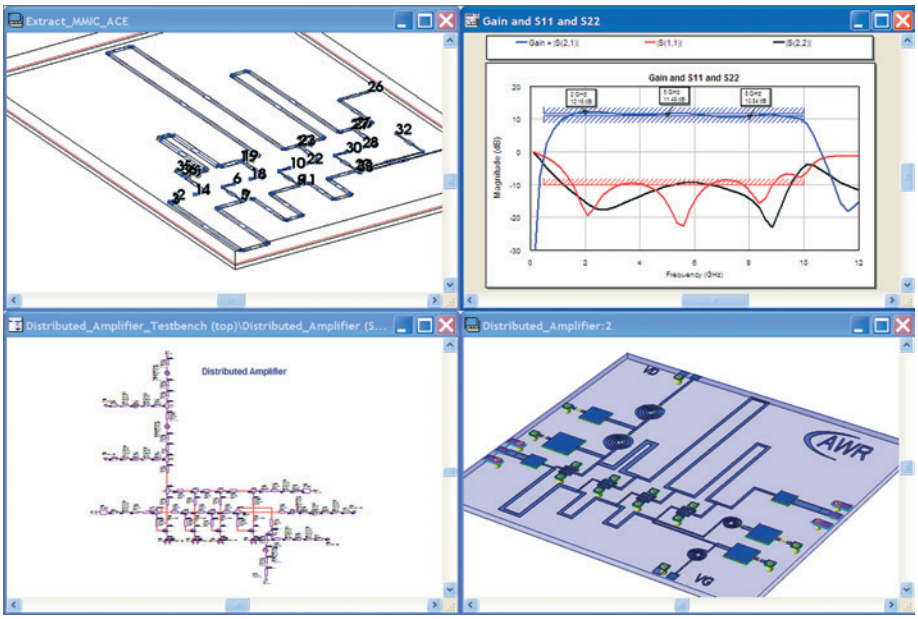


*Figure 7: The EXTRACT flow creates an EM document for ACE analysis*

## EXTRACT Flow with ACE Tool

By turning on full coupling within the ACE options tab on the EXTRACT block's parameter dialog box, it can be seen in Figure 8 that quite a bit of bandwidth is lost. Going back to the ACE options tab, the coupling radius can be changed to isolate the critical couplings (Figure 9). This takes only seconds as the EXTRACT flow continually updates the options for the EM document.

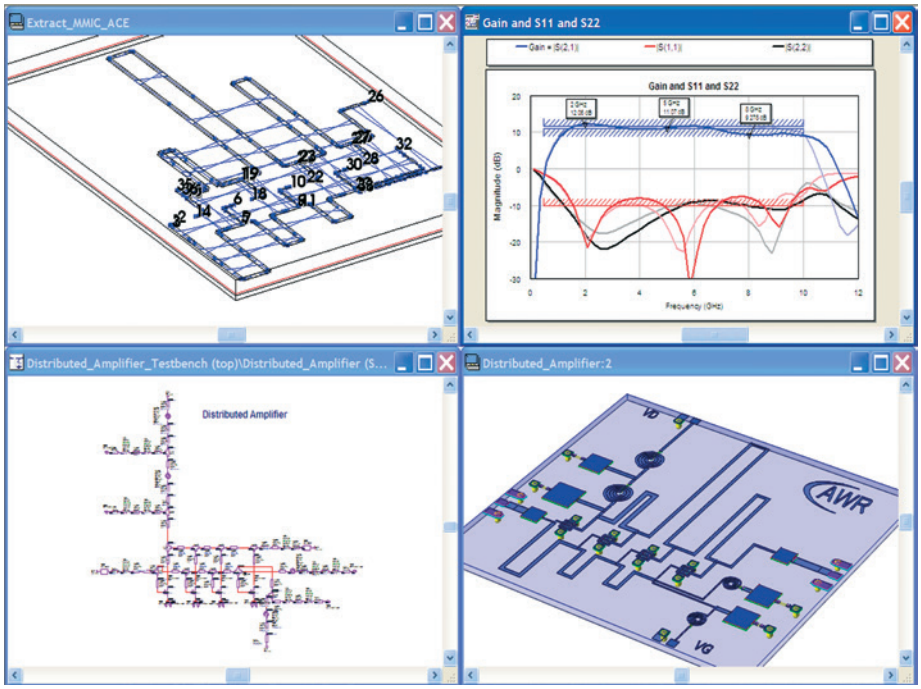


*Figure 8: The EXTRACT flow with the ACE tool shows all couplings for the distributed amplifier and the associated effect on bandwidth*

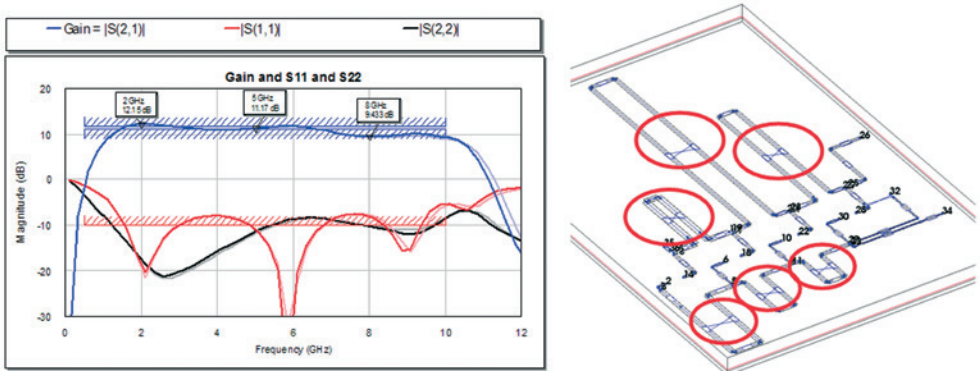


*Figure 9: The EXTRACT flow creates ACE analysis showing critical couplings, which alone give desired performance*

Since the critical couplings are defined parametrically, the optimizer can be started and used with the EXTRACT flow and all the couplings turned on, as shown in Figure 9. The EXTRACT flow creates ACE analysis within the optimizing loop, thereby allowing a new and appropriate set of parameters to be selected for each of the trombone sections defining the distributed amplifier's three stages. Once the optimization loop is finished running with the ACE tool, even greater accuracy can be obtained using the AWR AXIEM analysis.

## EXTRACT Flow with AWR AXIEM Analysis

To use the EXTRACT flow with the AWR AXIEM analysis as the EM desired solver, simply toggle a radio button and change the solver selection of the EXTRACT block to send an automatically created EM document to the AWR AXIEM analysis instead of or in addition to the ACE technology. Figure 10 shows a comparison between the two EXTRACT blocks using the same extraction group name. All elements in the extraction are identical to both analyses. Separate EM documents are created only to illustrate a results comparison, but a single EM document could be used.

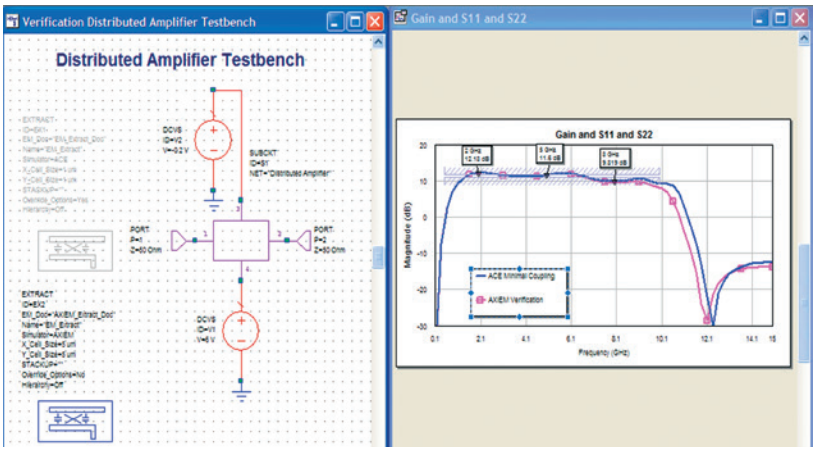


*Figure 10: The EXTRACT flow showing dual use of the ACE tool and AWR AXIEM analysis within a single EXTRACT group*

The simulators differ in that one has the simulator parameter specified to use AWR AXIEM analysis and the other to use the ACE tool. The difference in the S21 performance of the two options results from the use of EM quasi-static models for the coupled lines in the ACE tool rather than the 3D planar full-wave solution to Maxwell's equations with the AWR AXIEM analysis.

While the ACE tool lacks the AWR AXIEM analysis's ability to capture all the physics over the entire band, the overall accuracy is better than that provided by circuit element models alone. The ACE tool's benefit to the flow is in this middle ground, between the speed and ease of circuit element models which leave out critical couplings and the accuracy of AWR AXIEM analysis and other EM solvers, which may take more than the ACE tool's subsecond of extraction time. Together, circuit models, the ACE tool, and the AWR AXIEM analysis form a progressive triumvirate that moves with the designer sequentially through the design flow from concept and circuit models, to the preliminary design with the ACE tool and, finally, to the final simulations with AWR AXIEM analysis.

## Conclusion

EM solvers and circuit extractors are quickly becoming more and more critical to modern RF and microwave design flows. Frequency requirements, circuit complexity, and size constraints continue to drive design flows to more and more intimate concurrency between circuit simulation and layout analysis. These flows have traditionally been hampered by the need to have simulation-driven by schematic on one hand and EM represented by layout on the other. The AWR Design Software platform's EXTRACT flow eliminates this roadblock and improves user productivity by effortlessly enabling EM analysis and circuit extraction directly into a top-down flow.

The key benefit of the EXTRACT flow is that the EM setup is totally driven by and derived from the very same schematic, and associated schematic-driven layout that is used for the circuit simulation. Equally important in terms of time savings and elimination of errors, the resulting S-parameter matrix need not be manually retrofitted into a separate or modified schematic. The benefits of EXTRACTflow-enabled, schematic-driven EM simulation go far beyond the obvious automation aspects and associated time savings and related iteration and error reductions. The EXTRACT flow immerses EM analysis into circuit simulation, directly impacting design performance and flow efficiency and opening up significant possibilities for modeling and design for present and future EM extraction needs within the RF/microwave design community.

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