cadence®

CADENCE AWR DESIGN **MAGAZINE**

This special IMS edition of Cadence® AWR® Design Magazine showcases the latest release of the Cadence AWR Design Environment® platform, V15, and highlights recent application notes, customer success stories, and on-demand content for a broad range of RF/microwave applications.

Volume 20.IMS

Highlights

AWR Is Now Cadence

Virtual IMS Presentations

V15 Release of AWR Software

TABLE OF **CONTENTS**

COVER **STORY**

AWR Is Now Cadence

Glen Clark, Cadence VP of R&D for custom ICs and printed circuit boards (PCBs), spoke about the AWR acquisition in an exclusive Q&A with Microwave Journal in March 2020. Select highlights of the discussion follow:

What motivated Cadence to acquire AWR?

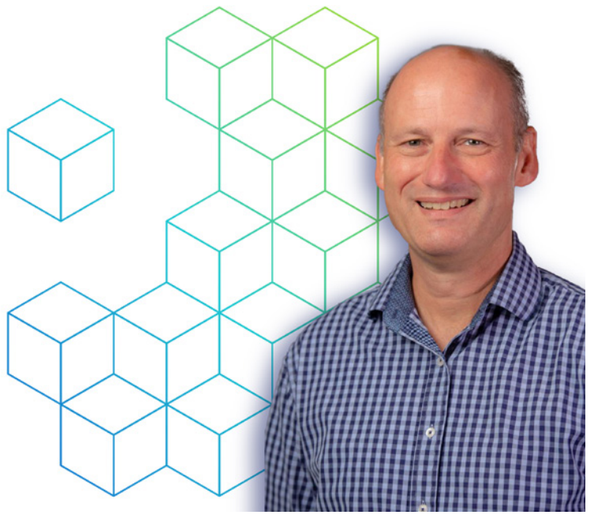
Historically, we've been incredibly strong in RF design on silicon (Si) but had more limited offerings for RF design in III-V technologies or microwave/mmWave design. As we worked with the AWR team to tightly integrate AWR AXIEM® 3D planar EM analysis into the Cadence Virtuoso® environment, we saw that a similar integration of other AWR simulation technologies into the Cadence tool suite provided a great opportunity for us and for our customers. Thus, the acquisition made complete sense, and we're happy to be working as one team now.

How are you integrating AWR products and people into Cadence? Will AWR remain a focused product area?

We are fully committed to the AWR product suite, and it will remain a focused product area for us. In fact, when we were doing our due diligence on the acquisition evaluation, we heard a consistent message that not only does AWR have great design tools, but they also do a superior job of supporting customers. We want to ensure that customers continue to get this excellent level of service. Additionally, we plan to leverage the AWR technology throughout the Cadence product lines, and we see a number of opportunities where we can support our customers optimally with a tight integration between AWR and existing Cadence products.

To read the full interview, visit www.awr.com/articles/executive-interview-glen-clark-cadence.

> *We plan to leverage the AWR technology throughout the Cadence product lines, and we see a number of opportunities where we can support our customers optimally with a tight integration between AWR and existing Cadence products.*
>
> Glen Clark, Cadence



Virtual IMS2020

Throughout the many challenges of this year, global communication systems have provided a vital lifeline, enabling people to work in safe isolation while remaining connected and productive. As 2020 marks the first worldwide deployments of 5G networks, connectivity has never been more important. Although circumstances prevent gathering in person at this year's International Microwave Symposium (IMS), Cadence is excited to participate in the technical sessions, MicroApps/workshops, and exhibition that will take place as a virtual event, made possible through the same communication systems that our customers help develop using our software.

At IMS2020, Cadence will be featuring demos and workshops developed especially for this virtual event that highlight new automated capabilities available in the recent V15 release of AWR software. The IMS2020 Virtual Conference provides designers with an opportunity to see how engineering productivity can be improved with new analyses, faster and higher-capacity simulation technologies, time-saving design automation, and 5G New Radio (NR) compliant testbenches that support power amplifier (PA) and antenna/array design, EM modeling, and RF/microwave integration across multi-technologies.

Learn more at www.cadence.com/go/awr/ims2020.

Virtual IMS Activities

IMS2020 has gone digital this year and the IMS planning committee has developed a virtual exhibition to facilitate the benefits of a face-to-face exhibition experience optimized for online interaction.

Join Cadence at the following IMS virtual event sessions and learn how to address your RF/microwave and multi-fabric design challenges, including electromagnetic (EM) analysis, verification, and cross-fabric implementation.

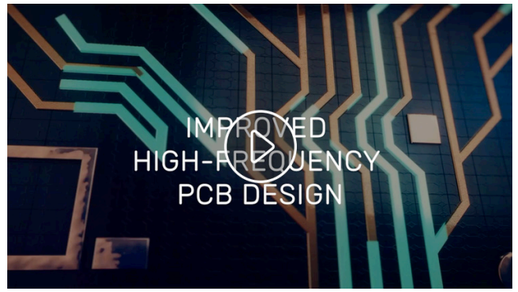
On-Demand Presentations

- PA Measurements Using Spectre Option and Virtuoso ADE Explorer and Assembler
  Sruba Seshadri
- Design Tutorial for a High-Efficiency GaN Doherty PA
  David Vye
- Module-Level RF/Microwave Design Flow Integrating Circuit/EM and Thermal
  David Choe and Michael Thompson
- Network Synthesis to Streamline PA Design Flow
  David Vye and Chris Bean
- Intuitive Microwave Filter Design Using EM Simulation
  Daniel Swanson, DGS Associates, LLC
- AWR AXIEM EM Simulation for Complex ICs and PCBs
  Dr. John Dunn
- Best Practices for Efficient EM Simulation
  Dr. John Dunn
- Understanding 5G System-Level Evaluation
  Gent Paparisto and Takao Inoue
- Automating Simulation of S-Parameters in Spectre Software
  Tawna Wilsey
- Parallel and Remote Schematic Simulation and Optimization
  Dustin Hoekstra

Live Demonstrations

Meet with Cadence experts during exhibit hours on August 4 – 6 to explore:

- Integrating multiple ICs onto an advanced RF module with the Virtuoso solution
- EM simulation for IC design based on the fast multipole method (FMM)
- The latest V15 release of AWR Design Environment software
- And more ...



To learn more, watch the IMS2020 highlight video at www.youtube.com/watch?v=z5hP0nwUdk0

Introducing AWR Design Environment V15

Engineering teams addressing performance, integration, and cost/space goals face time-to-market pressures while striving to meet increasingly complex product requirements. Version 15 (V15) of the Cadence AWR Design Environment platform offers new and enhanced technologies that provide greater design efficiency and first-pass success to engineering teams developing or integrating III-V ICs, multi-technology modules, and PCB assemblies for 5G, automotive, and aerospace/defense applications.

Engineering productivity is improved with new analyses, faster and higher-capacity simulation technologies, time-saving design automation, and 5G NR compliant testbenches that support PA and antenna/array design, EM modeling, and RF/ microwave integration across heterogenous technologies.

AWR Design Environment V15 Highlights				
Environment/ Automation	**Circuit Simulation**	**EM Simulation**	**System Simulation**	**Physical Design/ Layout**
Load-pull contours on rectangular plots	Fast, rigorous stability analysis	Faster, more robust adaptive meshing	Preconfigured 5G NR testbenches libraries	Real-time DRC compliant iNets routing guides
Template-based measurements	Low-frequency load-pull for two-tone excitations	Fast, accurate DC solver	Phased array MIMO bus support	Mixed physical units/ grid support
Add/edit optimization goals directly on graphs	Integrated TX-Line calculator/synthesis	Peak antenna measurements	PA linearization with digital predistortion (DPD)	Two-click data entry mode
Edit axes directly on plots	Network synthesis with PDK/vendor components			Resize layout objects with property page editing
Color-coded markers				
Equation grouping				Gerber file import for EM analysis

The V15 Advantage

AWR Design Environment V15 software offers key new and improved technologies that provide greater design efficiency and first-pass success to engineering teams developing and integrating III-V and Si ICs, multi-technology modules, and PCB assemblies. Engineering productivity is improved with new analyses, faster and higher capacity simulation technologies, time-saving design automation, and 5G NR-compliant testbenches that support PA and antenna/array design, EM modeling, and RF/ microwave integration across heterogenous technologies.

To learn more continue reading or download the complete technical brief at www.awr.com/serve/tb-v15.

Design Environment and Automation

New design environment and automation features help individual engineers and engineering teams be more efficient in their design entry, data display, and project management. Designers can adjust optimization goals directly from response plots, route design rule-compliant intelligent nets (iNets) in real-time, import Gerber-based layout designs into AWR Design Environment software for EM analysis, and provide more user capabilities for the design task at hand.

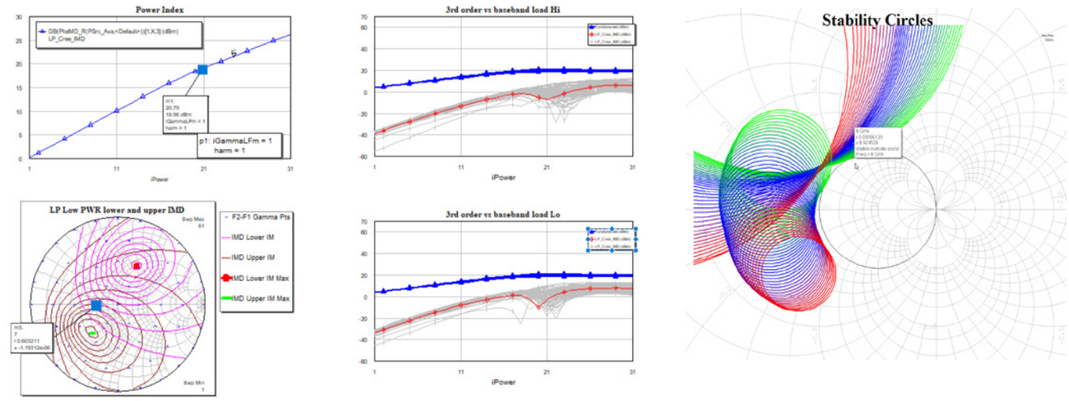
Synthesis Accelerates RF Designs

The characteristic impedance and electrical length (delay) of transmission lines represent two important design parameters used to control the frequency-dependent circuit response of passive RF/microwave circuits. Using AWR V15 software, designers can now directly synthesize the physical attributes (width, length) of microstrip, stripline, or coplanar waveguide structures for a given substrate based on the desired electrical characteristics.

Likewise, the electrical characteristics can be calculated directly from the physical properties of the single or edge-coupled transmission line placed in the schematic. Synthesis of circuit model parameters provides vital data for generating accurate layout of these transmission lines without having to invoke the transmission line calculator and manually transfer the results into the transmission line property dialog box.

PA Simulation and Design Support

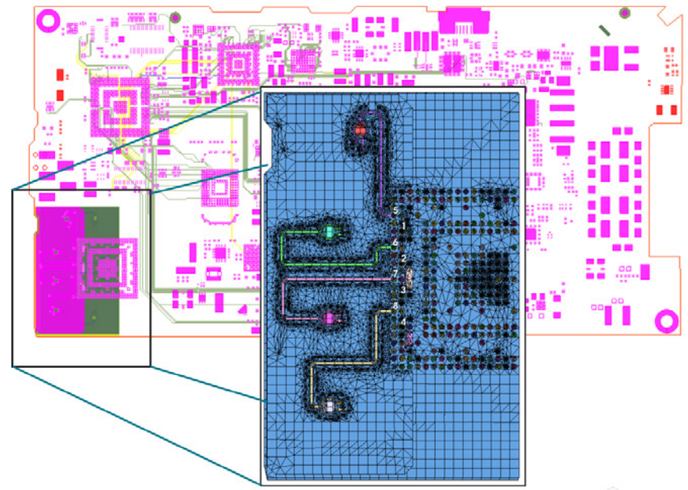
V15 of AWR software allows designers to optimize PA linearity performance through video band load-pull analysis of power amplifiers (PAs) operating under two-tone excitations. Designers can plot intermodulation (IMD) and third-order intercept point (IP3) results as a function of (F2-F1) impedance, directly investigating IMD products over swept input power. Load-pull analysis also supports impedance tuning at the 4th and 5th harmonics as well as the ability to generate contours on rectangular plots for enhanced visualization of performance versus load impedance.



Video-band load pull supports low-frequency impedance optimization to reduce IMD product (left) and loop gain envelope provides fast and rigorous nonlinear stability analysis and optimization (right)

EM Simulation and Antennas

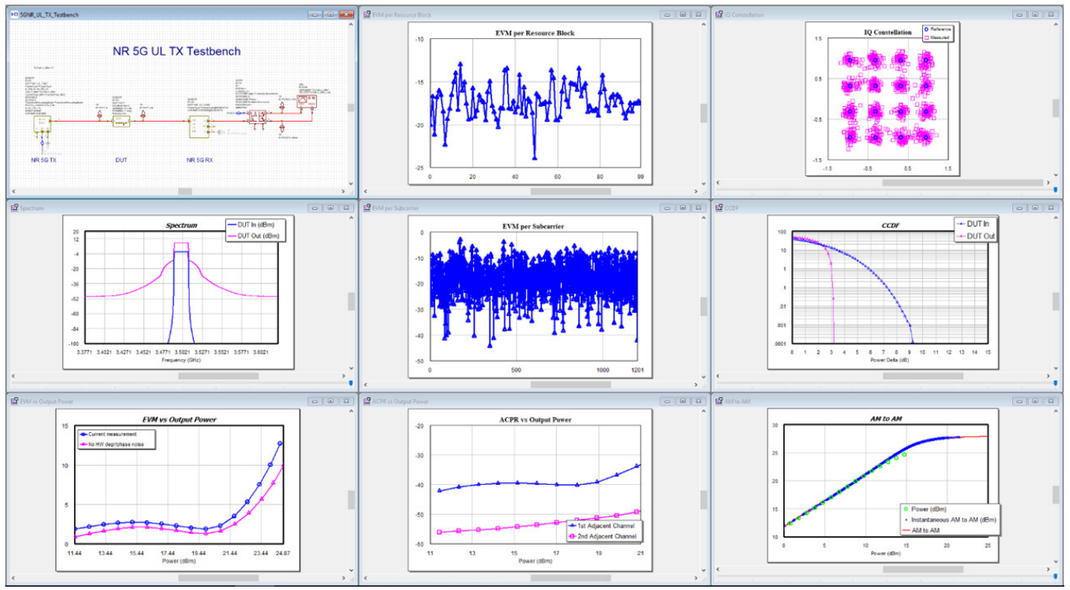
To enhance the speed and capacity of EM analysis for IC, package, and board structures, AWR AXIEM meshing and solver technologies have undergone several key improvements, resulting in improved mesh quality for faster simulation run times and the ability to solve larger problems with a reduced mesh. AWR Design Environment V15 software can now detect and remove problematic mesh facets automatically with robust healing of high aspect ratio facets (HARF).



Improved meshing and EM solver tackles large structures, faster

5G NR Library and DPD Models

The 5G NR library offers easy-to-configure signal sources and receivers that can be used to evaluate RF components and/or RF links using system-level measurements. New testbenches accelerate the component design and evaluation process with preconfigured 5G NR transmit (TX) and receive (RX) blocks and measurements supporting TX/RX functionality for both downlink and uplink.



5G NR libraries and test models for TX/RX device and RF link validation

Conclusion

AWR Design Environment V15 software brings new and enhanced RF/microwave design and simulation to the Cadence portfolio of EDA solutions. Advanced design automation optimizes engineering throughput and productivity by reducing manual design tasks and supporting tool interoperability.

New circuit simulation capabilities address fast and rigorous nonlinear stability analysis for multi-stage and balanced amplifiers, and video-band load pull to optimize low-frequency impedance terminations for reduced intermodulation distortion. Network synthesis supports impedance network development using vendor components and process design kits (PDKs), and a new integrated transmission-line calculator and synthesis capabilities launched directly from schematic.

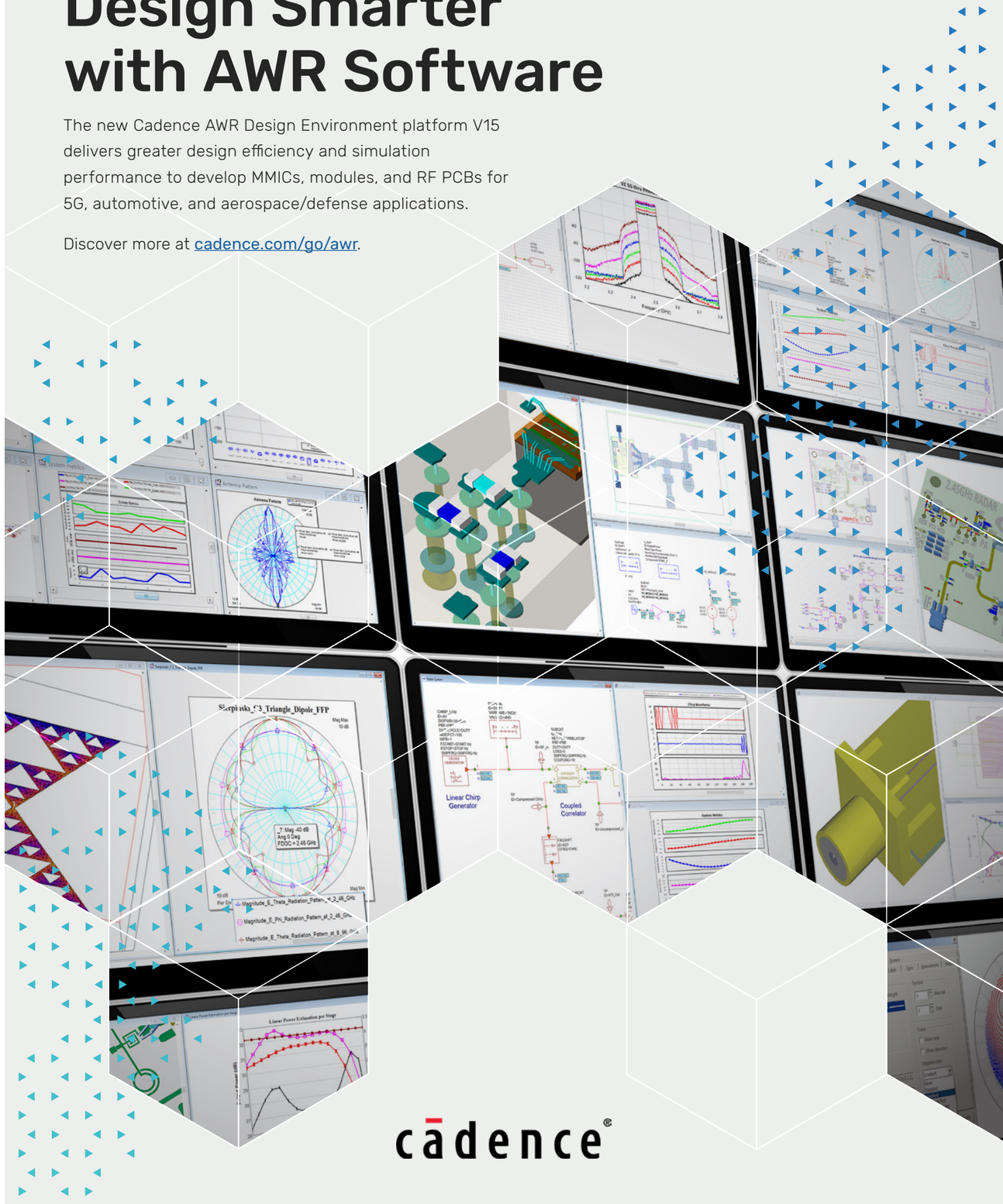
Robust simulation engines solve large structures more quickly using EM analysis with enhanced meshing and smart geometry handling for chip, package, and board characterization. Preconfigured, 5G NR-compliant testbenches provide signal sources and measurements for PA and RF link validation.

Learn more about AWR Design Environment V15 at www.awr.com/whatsnew.

Design Smarter with AWR Software

The new Cadence AWR Design Environment platform V15 delivers greater design efficiency and simulation performance to develop MMICs, modules, and RF PCBs for 5G, automotive, and aerospace/defense applications.

Discover more at cadence.com/go/awr.



RFIC/SiP Design: AWR AXIEM EM with Virtuoso RF

The AWR AXIEM EM simulator is now integrated with the Cadence Virtuoso RF solution, providing designers with an integrated circuit (IC), package/module design flow that improves productivity by eliminating the design failures caused by the manual translation of data. A single golden schematic is used for simulation, layout versus schematic (LVS), and EM analysis and verification, without the need for unique schematics for EM and LVS.

Using the AWR AXIEM Simulator with Virtuoso RF

The AWR AXIEM EM simulator within AWR Microwave Office® circuit design software is a best-in-class planar, open boundary 3D planar engine that solves for currents on horizontal metal traces and vertical vias. Prior to the Virtuoso integration of the AWR AXIEM EM solver, users of both tools relied upon manual integration, namely exporting and importing the layout between the Virtuoso environment and the AWR AXIEM simulator within the AWR Microwave Office environment.

Integrated AWR AXIEM Solver/Virtuoso RF Flow

The integrated AWR AXIEM EM solver within the Cadence IC/ system-in-package (SiP) flow for layout of silicon ICs provides design optimization and layout verification within a single schematic.

Traditionally, layout and schematic are loosely coupled in Cadence software. The golden schematic couples much more tightly with the layout, reducing error and saving time. Figure 1 shows the golden schematic on the left and the AWR AXIEM spiral layout in Virtuoso RF. The model assistant is docked on the right side of the layout window.

The white box drawn around the spiral is the limit of the layout that is extracted to AWR AXIEM software, in this case the spiral and feed lines. Ports are automatically attached to the feed lines once the layout is placed in the AWR AXIEM simulator. There is no need for the designer to add ports; they are added wherever the feed lines hit the simulation boundary in the Virtuoso layout. The box on the far right is the model assistant. It enables the designer to set the simulator nets and various control options.

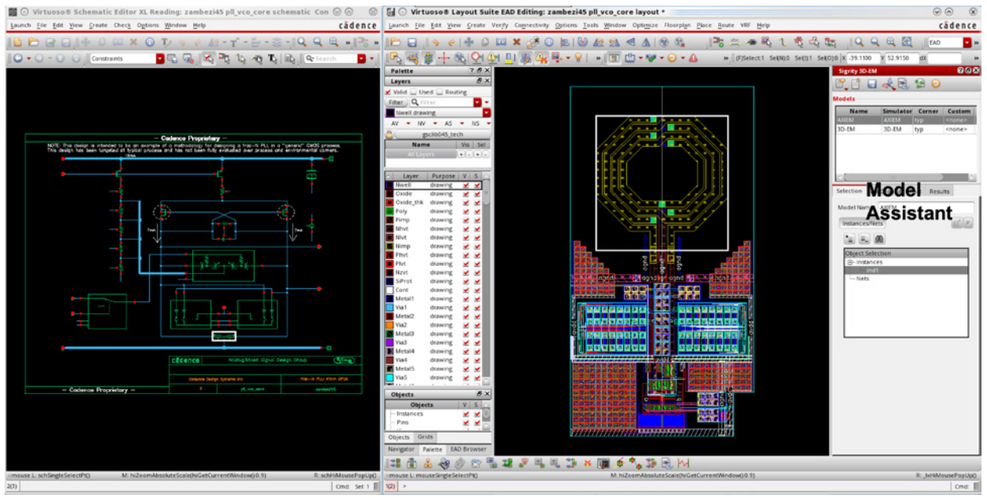


Figure 1: AXIEM model in Virtuoso

The Process Setup in the Virtuoso Environment

For it to work properly, AWR AXIEM software requires that the STACKUP properties, material properties, and various simulation settings be configured. These settings reside in the Virtuoso modeling assistant. Figure 2 shows the PDK setup in the model assistant with several representative menus, for example, dielectric and via properties are shown in the middle picture, where the silicon material properties and layer thicknesses are listed.

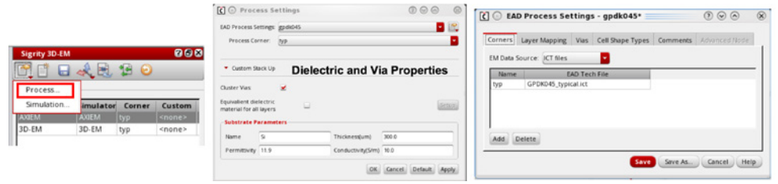


Figure 2: PDK setup in the Virtuoso model assistant

There are some preview and diagnostic capabilities built into the AWR AXIEM integration. Figure 3 illustrates how the mesh can quickly be previewed in the AWR AXIEM model to understand the density that will be used and the accuracy level.1 Note that in this example the mesh density is relatively sparse. There is a nice 3D view of the mesh on the surface of the inductor. Thick metal with side walls is being used to capture the coupling. The meshing density can be adjusted in the AWR AXIEM setup menus if desired.

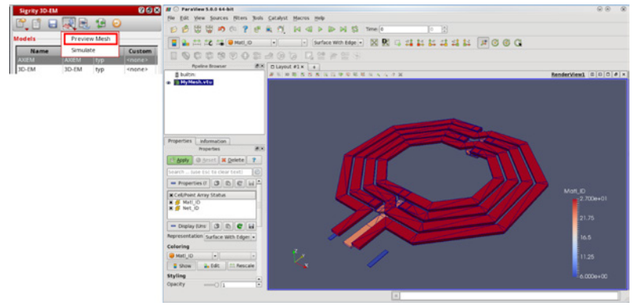


Figure 3: Mesh preview in the AXIEM simulator

The goal of the Virtuoso and AWR AXIEM EM solver flow is to enable the designer to stay within Virtuoso environment and yet gain access to S-parameters with full-wave accuracy. After the S-parameters are generated, the model in the golden schematic is replaced with the S-parameter results. The extracted view is then created, and the model in the schematic is replaced with the S-parameters.

Conclusion

As frequencies of operation push upward, EM simulators are becoming more and more critical for RFIC designers. Distributed effects, such as inductors, become important, as do frequency-dependent effects such as resistance. Grounding issues become critical and must be accounted for in simulations. Structures such as meshed ground planes and rings need to be EM simulated to ensure they are modeled correctly. Coupling effects between various components, which are not included in models, become an issue and must be EM simulated.

The AWR AXIEM EM solver and Virtuoso design flow seamlessly integrates the process of accounting for EM effects within a circuit design project by enabling a single environment for simulation, LVS, and EM analysis and verification, without the need for unique schematics for EM and LVS. This new flow reduces the chance of error and cuts design time and verification cycles.

RF PCB Design: AWR with Allegro

Designers face multiple challenges when incorporating RF/microwave, analog, and digital design elements together on the same PCB. These multi-layer PCBs, which are commonly used in next-generation commercial and military applications, are densely populated with high-speed data lines and RF circuitry and are prone to coupling/crosstalk and other parasitic behavior that can impair system performance.

To successfully integrate RF/microwave content and mixed-signal designs, PCB layout tools and RF circuit design software must exchange design data efficiently. AWR software offers an RF/microwave intellectual property (IP) creation platform with import and export functionality to provide a pathway to and from Cadence Allegro or OrCAD® PCB design tools (Figure 1).

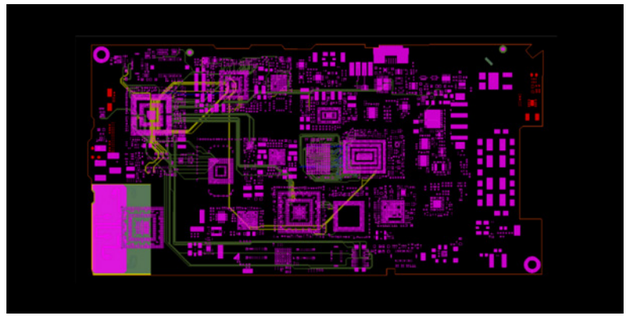


Figure 1: Cadence originated PCB imported into AWR software through an IPC-2581 file format

RF/Microwave IP Integration

RF/microwave designers use schematic capture to place active and passive components within a network. Unlike analog and digital designs, which use parasitic extraction after layout, these designs typically include closed-form transmission line models (such as microstrip and stripline) explicitly in the schematic to account for RF behavior much earlier in the design process. EM analysis is also used to characterize structures and validate the overall design. In this way, the electrical and physical designs are concurrently implemented. The AWR Design Environment provides the platform for RF/microwave design entry, circuit/system/EM analysis, and optimization.

The result is an electrical design with the layout and PCB stackup information necessary to ensure accurate prediction of the manufactured device's performance. Transferring this layout and stackup information into the Cadence PCB layout and routing platform eliminates the need for manual design reentry, thus saving time, costs, and the potential for errors.

Features

- Linear/nonlinear frequency-domain simulation for RF/microwave circuit design
- Schematic-driven RF-aware design with integrated EM extraction technology
- Parametric studies with optimization, tuning, and yield analysis

Benefits

- Reduce design time with a comprehensive workflow that supports data exchange between RF/microwave and PCB design tools
- Maximize engineering productivity with design automation and a user-friendly interface for engineers of all skill levels
- Eliminate costly design respins through accurate design verification

RF/Microwave PCB Verification

RF/microwave PCB verification is enabled by importing an IPC-2581 file into AWR software through the AWR Microwave Office software PCB import wizard (Figure 2). Powerful editing features prepare the structure for fast, accurate, and efficient EM analysis using the AWR AXIEM planar EM simulator, which enables designers to select traces, layers, and board regions and specify exactly which layers, nets, and board areas to analyze. Designers can easily omit manufacturing details that won't impact electrical behavior but will unnecessarily slow down the simulation.

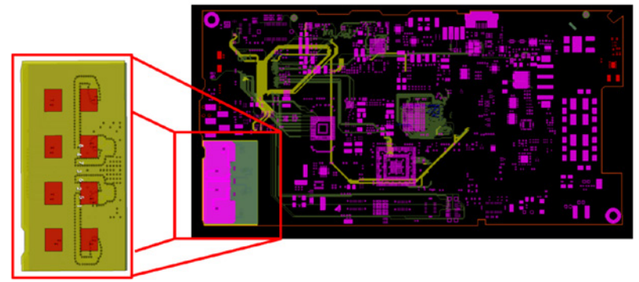


Figure 2: Integrated mmWave IP area on a mixed-signal PCB with antenna array in the red popout

The AWR AXIEM simulator uses the method-of-moments (MoM) technique to analyze distributed PCB components, transmission lines, and layer-to-layer PCB interconnects like vias. Designers extract S-parameters directly and visualize fields/currents to identify parasitic coupling, resonances, and other concerns that could lead to design failure.

Features

- Full-wave planar MoM technology with advanced hybrid adaptive meshing
- Time-saving PCB import wizard technology
- Layout editor with shape modifiers/defeaturing for fast EM simulation
- Field visualization and post-processing

Benefits

- Reduce design time with a comprehensive workflow that supports data exchange between RF/microwave and PCB design tools
- Maximize engineering productivity with design automation and a user-friendly interface for engineers of all experience levels
- Eliminate costly design respins through accurate design verification

Conclusion

At higher operating frequencies, the physical details of circuit components and signal traces will impact electrical performance and must be considered as part of the design process. Electronics can appear to behave in unpredictable ways at radio and microwave frequencies, often seeming to violate basic electrical principles such as Ohm's law. EM analysis based on layout and stackup information is commonly used by RF/microwave designers to understand how physical design impacts electrical behavior.

With RF-aware simulation tools, engineers eliminate wasted cycles trying to design and troubleshoot front-end components and related integration challenges. In addition, EM analysis plays a critical role in design verification of all high-speed mixed-signal traces. The state-of-the-art RF/microwave capabilities within the AWR software product portfolio help engineers ensure successful wireless design and integration.

To learn more, watch the webinar recording "Developing PCBs for Wireless Applications with EM Verification and an RF Design Flow" at awr.com/developing-pcbs-wireless-verification-flow.

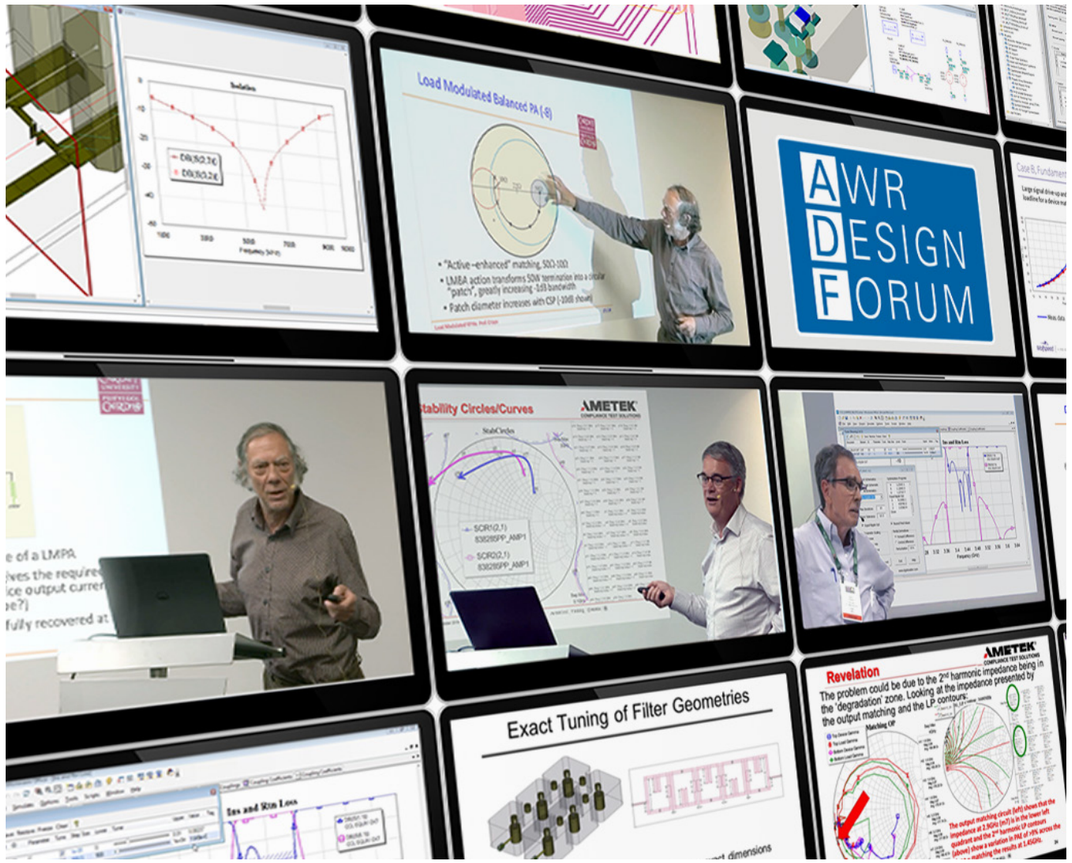
Best of ADF Now Available On-Demand

For those who missed the live AWR Design Forum (ADF) 2019 tour and/or want to learn more about Cadence AWR Design Environment software, a video collection of the best presentations from customers, partners, and academia is now available for on-demand viewing.

The keynote, given by noted power amplifier expert Dr. Steve Cripps, a distinguished research professor at Cardiff University in Wales, discusses some of the potential benefits and possible hazards of a new approach to PA design.

The Best of ADF 2019 collection is organized into five tracks addressing various aspects of RF/microwave design and highlights presentations from Dr. Steve Cripps, Cardiff University, key industry experts Dr. Zoya Popovic, University of Colorado, Dr. Dominic FitzPatrick, Ametek-CTS, and Dan Swanson, DGS Associates, as well as prominent companies such as Wolfspeed, Arralis, United Monolithic Semiconductors (UMS), AMCAD, OMMIC, and Focus Microwaves.

Start watching at www.awr.com/adf.



Track 1: Keynote and Industry Insights

- Active and Passive Matching in RF PAs
  Dr. Steve C. Cripps, Cardiff University
- Instability in Wide Bandwidth High PAs
  Dr. Dominic FitzPatrick, Ametek-CTS
- Enhanced Design Flow for Cavity Combline Filters
  Dan Swanson, DGS Associates
- RF/Microwave Design in Teaching
  Dr. Zoya Popovic, University of Colorado

Track 2: Semiconductor Technology and Modeling

- Wolfspeed RF Device Modeling
  Dr. Yueying Liu, Wolfspeed, A Cree Company
- Gallium Nitride-on-Silicon Carbide at High Frequencies
  Eric Leclerc, UMS
- 5G High-Power and Low-Noise Applications
  Julien Poulain, OMMIC
- Coupled Effect Between Antenna Arrays and Front Ends
  Wissam Saabe, AMCAD Engineering

Track 3: PA and Front-End Design

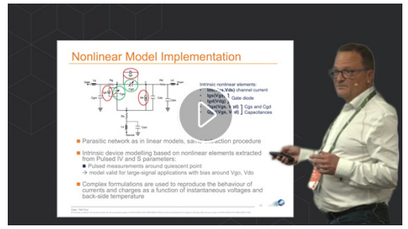
- HPA Design for Satellite Communications
  Thomas Young, Arralis and David Vye
- MMIC PA Design
  David Vye
- Input and Output Controlled High-Efficiency PAs
  Vince Mallette, Focus Microwaves
- Doherty PA Design from Load-Pull Derived Enhanced Polyharmonic Distortion (EPHD) Models
  David Vye

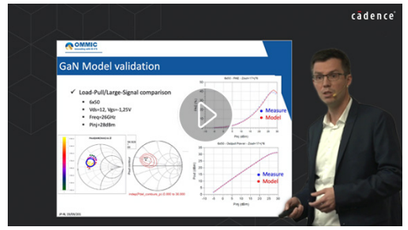
Track 4: EM Analysis and Design Optimization

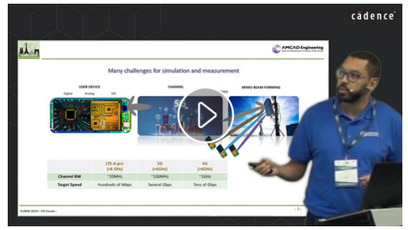
- Best Practices for EM Simulation
  Dr. John Dunn
- Tips and Tricks for Silicon RFIC Designs
  Dr. John Dunn
- Designing a Narrowband 28GHz Bandpass Filter for 5G
  David Vye

Track 5: Communication/Radar System Simulation

- Phased-Array Antenna Simulation for 5G
  Steve Tucker, Cadence
- RF Link Budget Analysis Using VSS
  Joel Kirshman
- Phase Noise Modeling Using VSS
  Joel Kirshman







On-Demand Webinars

AWR Software V15 Spotlight Webinars

- Power Amplifier Design in AWR Design Environment V15
  Dr. John Dunn
- Filter Design in AWR Design Environment V15
  Dr. John Dunn
- Phased-Array Antenna Design in AWR Design Environment V15
  Joel Kirshman
- Advanced PA Design Capabilities
  Chris Bean
- Developing PCBs for Wireless Applications
  Dr. John Dunn and David Vye
- 5G Technology Creation from a Customer Perspective
  Dr. John Dunn

Customer Spotlight Webinars

- RF Amplifier Simulation Using ADI Models
  Ivan Soc, Analog Devices
- mmWave MIMO Radar System Design
  Dr. Tero Kiuru, VTT

To view more videos and webinars, visit www.awr.tv and www.awr.com/resource-library.

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RF/MICROWAVE DESIGN SOFTWARE

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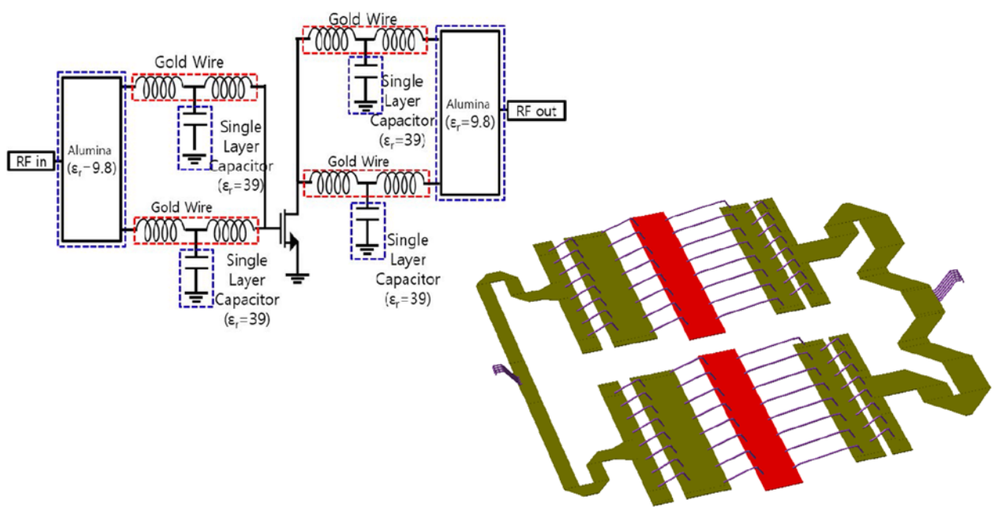
Get started today at ww.awr.com/try

Wavice Research Engineer Designs S-Band IMFET

Long-range radar systems with solid-state PAs often require high-power output, and as there is limited installation space, the device must also be very small in size. MMICs are considered the best solution for reducing the size of PAs.

> *AWR software is intuitive, which reduced my design time while delivering high accuracy," said Oh. "In particular, the tuning and optimization features are advantageous for assigning variables to view performance trends.*
>
> Kwanjin Oh, Wavice Inc.

However, the development cost of MMICs can be extremely high when used in low- to medium-volume applications such as defense. Wavice Inc designer Kwanjin Oh used the AWR Microwave Office circuit simulator within the AWR Design Environment platform to design an internally matching field-effect transistor (IMFET) that enabled a reduction in the size of the PA by more than 10 times. Matching the source and drain impedances was straightforward and the load-pull analysis, tuning, and optimization features in the software significantly reduced design time as well.



Block diagram and 3D layout of IMFET

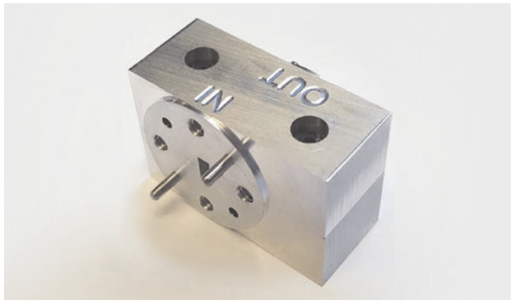
To read the full story, visit www.awr.com/customer-stories/wavice-inc.

Anritsu Designs G-Band Frequency Tripler for Broadband Instrumentation

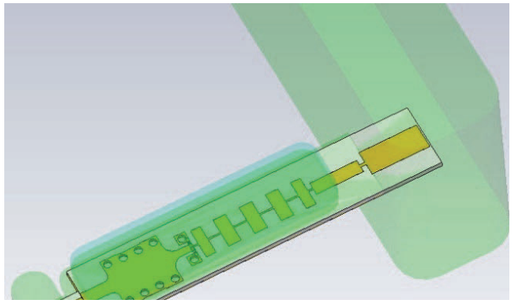
Broadband frequency sources are required to extend the frequency range of broadband microwave and millimeter-wave (mmWave) test equipment for applications such as 5G NR communications, automotive radar, and security (detection) applications. In some broadband systems, nonlinear transmission line (NLTL)-based multipliers and receivers have been used to extend the frequency ranges. NLTL-based multipliers can be used to extend broadband system frequency ranges.

> *The time it takes to figure out how to do something with AWR Microwave Office software is far less than other circuit simulators on the market. It is the only circuit simulator Anritsu owns and uses.*
>
> Jon Martens, Anritsu

However, the difficulty in meeting the input drive level and unwanted harmonic suppression requirements for NLTL devices motivated Anritsu designers to develop an extended planar frequency tripler covering the entire G-band (140-220GHz). AWR software enabled them to 3D simulate the structure and extract an accurate representation of the six-port model that was critical to the success of the design.



WR15-WR5 G-band tripler assembly



Complete 3D EM model of the G-band tripler.

To read the full story, visit www.awr.com/customer-stories/anritsu-corporation.

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