SUCCESS **STORY**

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# Arralis and Cadence

## K-Band Satcom MMIC PA Using AWR Software

### Key Challenges

K/Ka-band satcom systems can provide constant, uninterrupted access to information, driving companies to invest heavily in this spectrum for global broadband services. These systems are enabled through high-power amplifiers (HPAs), which form the final link in the RF power chain of next-generation, satellite-based, RF front-end components. Arralis has developed the Leonis chipset, originally as part of the European Space Agency (ESA) Advanced Research in Telecommunications Systems (ARTES) program, to address the growing demand for lower cost K/Ka-band satellite equipment.

The chipset includes IQ and subharmonic mixers, upconverter and downconverter core chips, switches, phase shifters, low-noise amplifiers (LNAs), and PAs. Within this chipset is the company's LE-Ka1330308, a high-power monolithic microwave integrated circuit (MMIC) amplifier that was fabricated on space-qualified 0.25µm gallium nitride on silicon carbide (GaN on SiC). The three-stage MMIC amplifier was fabricated on the United Monolithic Semiconductors (UMS) GH25-10 process. Arralis has successfully demonstrated transceiver architectures for both uplink and downlink communications.

#### Application

- MMIC PA
- Passives
- PCB
- Packaging

#### Software

- Cadence® AWR Design Environment® platform, including:
  - Cadence AWR® Microwave Office® software
  - Cadence AWR AXIEM® 3D planar analysis
  - Cadence AWR Analyst™ 3D Finite-Element Method (FEM) analysis

#### Benefits

- Co-simulation ability
- Complete solution
- Design efficiency

Figure 1 illustrates the low-band transmitter architecture and performance with the integrated HPA.

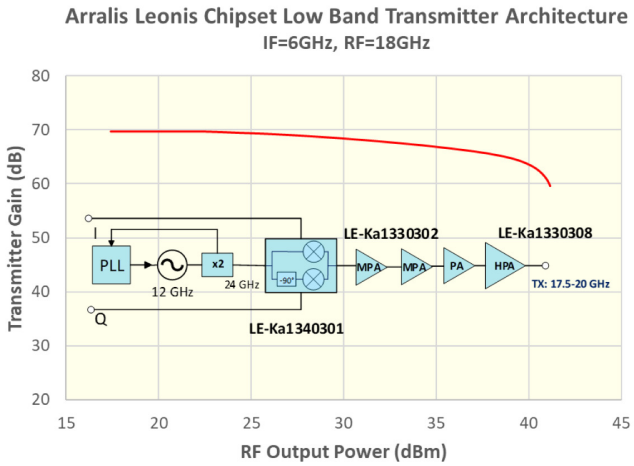


*Figure 1: Chipset architecture for K/Ka-band satcom applications*

## Solution

During the design phase, extensive circuit design and simulation was performed using the AWR Design Environment platform, specifically AWR Microwave Office software, the AWR AXIEM EM simulator for 3D planar structures (MMIC manifold feed network, on-chip passives, and evaluation board), and the AWR Analyst EM simulator for 3D EM analysis of the package. Arralis designers used the simulation software to work with the active and passive MMIC component models developed by the foundry and organized into process design kits (PDKs) developed through collaboration between the AWR and UMS modeling teams.

> *Cadence's AWR Microwave Office circuit design software combined with the powerful AWR AXIEM and Analyst EM simulators enabled us to work with the active and passive MMIC component models developed by the foundry to design and optimize the Arralis HPA.*
>
> Thomas Young, Arralis Ltd.

The MMIC die was represented in simulation using foundry-verified, schematic-based models and EM analysis, allowing the designers to reliably predict and optimize key performance metrics.

Figure 2 shows the correlation between measured and modeled S-parameters. The graph also shows the simulated gain variation due to process tolerances. Measured gain performance falls on the high side of the variation; however, it is within the predicted limits of the simulation.

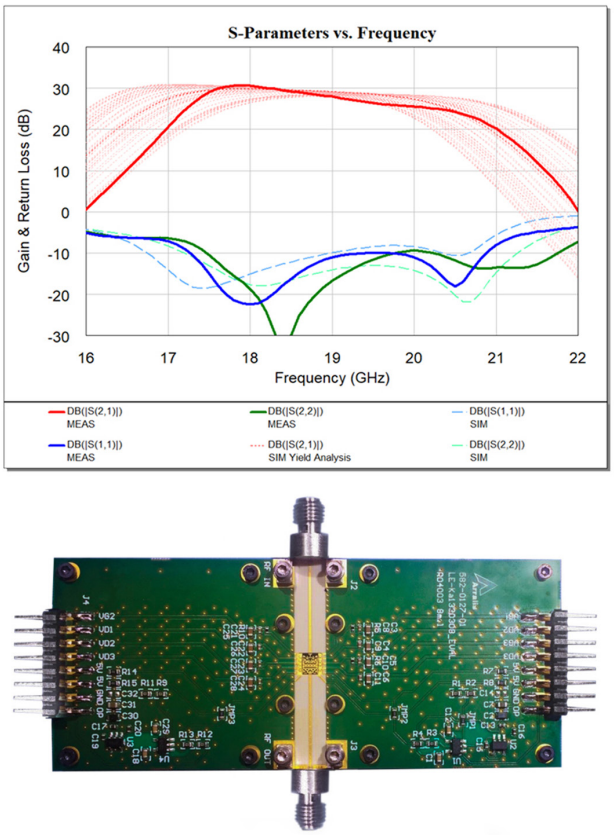


*Figure 2: Simulated data including yield analysis vs. modeled small-signal frequency response for the LE-Ka1330308 reference board*

Significant EM analysis and design optimization was carried out at the component and subcircuit level to ensure that parasitics and inadvertent EM coupling between structures was incorporated into the simulation. Towards the end of the design phase, the AWR AXIEM simulator was used for larger and more integrated EM analysis for final verification and to ensure that all interactions were captured in simulation.

The success of the bare die MMIC has fueled the subsequent development of a packaged part that will facilitate a more convenient solution for system integration. The Kyocera SGMR-B1193, a commercially available 7 x 7mm ceramic quad-flat no-leads (QFN) package, was selected for investigation, as shown in Figure 3.

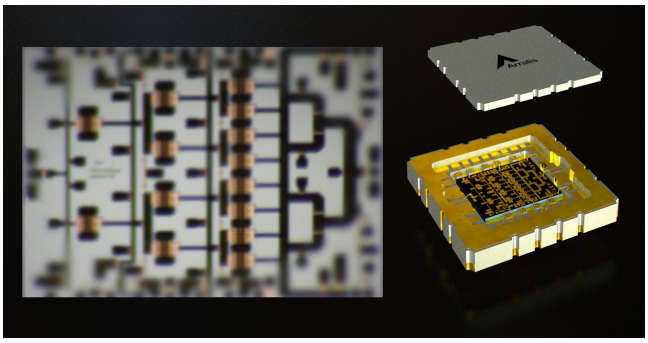

*Figure 3: Proposed packaging (Kyocera SGMR-B1193) for K-band HPA. Image courtesy of Kyocera Corporation*

This package will provide a hermetically sealed solution with enough space to accommodate the die and decoupling capacitors, while also minimizing the RF I/O bond-wire length. A coefficient of thermal expansion (CTE)-matched molybdenum copper (MoCu) heat sink will provide a reliable thermal path through the base. The ceramic QFN package is a compact size of 7 x 7mm.

This RF transition was simulated using the AWR Analyst EM simulator (Figure 4) to minimize return loss due to impedance mismatches between the MMIC, the package, and the evaluation board. The simulation results show a well-matched transition with insertion loss of 0.25dB. This will translate to an overall gain reduction of 0.5dB and power reduction of 0.25dB for the packaged part compared to bare die option.

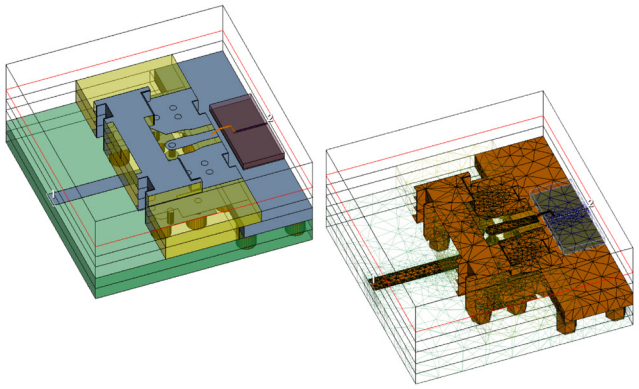

*Figure 4: Details of package model I/O port simulation setup (left) and resulting mesh in AWR Analyst software (right)*

## Conclusion

Arralis engineers successfully designed a K/Ka-band chipset, inclusive of a 10W saturated output power HPA, for satellite communications applications. The three-stage MMIC amplifier, fabricated with space-qualified, 0.25µm GaN on SiC, was developed using state-of-the-art semiconductor technology, foundry-qualified device models, and AWR software circuit/EM simulation technology. Transceiver architectures for both uplink and downlink communications were demonstrated with this chipset and the integrated HPA. Additional development efforts are focused on integrating the bare die into a suitable package with initial samples of the packaged HPA.

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