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SYSTEM ELECTROTHERMAL TRANSIENT ANALYSIS OF A HIGH CURRENT (40A) SYNCHRONOUS STEP DOWN CONVERTER

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ABSTRACT

In this paper, we detailed the system electrothermal transient co-design modeling and silicon validation effort that led to the industry's first highly efficient, highest power density (40A) synchronous step-down converter. The device was designed in an innovative multichip module (MCM) low-profile LQFN packaging technology. By integrating the control and drive circuitry with two discrete N-channel power MOSFETs, significant reduction in system on-resistance, RDS(ON), was achieved. The validity of the co-design electrothermal modeling methodology was assessed by comparing directly to silicon thermal measurements made on an evaluation module (EVM) which comprises the inductor, capacitor, and other essential components. Correlation between simulation and laboratory measurements on the integrated solution will be discussed.

Keywords: DCDC converter, High Current, 3D Packaging, Electrothermal Simulation and Correlation.

NOMENCLATURE

BEOL	Back-end of line
DC-DC	Direct current-Direct Current
FEA	Finite Element Analysis
LQFN	Low-profile Quad Flat No-Leads
MCM	Multichip module
PCB	Printed Circuit Board
$R_{DS(ON)}$	Drain-to-source On Resistance

1. INTRODUCTION

All DC-DC converters dissipate power in the form of heat. This heat has to be managed properly to making sure the converter maintains operation within the recommended temperature limits [1]. Managing heat dissipation has always been a critical concern for any power supply designer, and this concern has grown to utmost importance as output current levels have increased while IC packages size are reduced in an attempt to achieve optimal power densities. To promote efficient heat removal, a number of innovative power packages technologies have recently emerged. One such innovation is TI PowerStack™, a multi-chip module (MCM) in low-profile quad-flat no-lead (LQFN) package [2]. The PowerStack™ allows for three-dimensional (3D) stacking of power MOSFETs in a "source-down" configuration that improves electrical and thermal performance (see Figure 1). Stacking naturally eliminates several electrical parasitics by placing the common terminals in immediate physical contact via copper clip bonding connectivity. The thick copper bridge substantially reduces $RDS_{(ON)}$, i.e. conduction losses, compared to wire bonding and provides excellent thermal performance. The electrical benefit of the innovative PowerStack™ package is thoroughly covered in [3]. Thermally, the stack configuration is inherently superior as the exposed ground pad effectively transfers heat to the printed circuit board. The 3D stacking configuration allows for thermal optimization by leveraging the best thermal-spreading layer(s) for effective heat dissipation as compared to the traditional side-to-side MOSFET lateral placement configuration [2]. By soldering the exposed pads on the device directly to the PCB, the heat generated can be drawn away from the device. Thermal vias located under the device can be used to channel the heat directly to internal ground planes or other heat sinking structures built into the PCB.

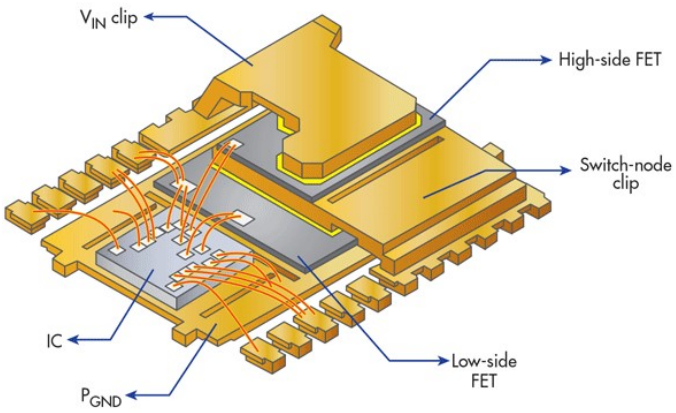


Figure 1. PowerStack™ 3D package showing copper clip connectivity.

In response to continued device scaling, the power-supply converter designs are moving toward lower voltage, higher current and quicker response to transient load variations. The exponential power density increase will in turn leads to increasing device junction temperature and localized "hot-spots". The higher temperature has significant adverse impacts on the device performance and reliability. In addition to the classical thermal analysis, it is shown that temperature-dependent electrothermal simulation is necessary for accurate estimates of multilevel back-end of line (BEOL) interconnect temperatures under aggressive current loadings thermal conditions [4]. Additionally, with continued package size reduction and PCB layer counts minimization, metal temperature is increasing significantly due to increasing current density. Thermoelectric effect is creeping up and if not assess early in the design process can lead to inaccurate thermal performance assessment.

In this work, the importance of augmenting traditional thermal analysis to additionally comprehend thermoelectric effect of the package and PCB high current density metallization is demonstrated. The impact is shown through system-level electrothermal modeling, simulation, and verified by comparison to silicon laboratory measurement on a high current (40A) synchronous step down converter. As device scaling continues, it is evident that electrothermally-aware temporospatial design considerations should be considered early in the design process to ensure optimal performance.

2. MATERIALS AND METHODS

This section is divided into five sub-sections. Sub-section 2.1 provides an overview of the high current (40A) synchronous step down converter device. The system-level electrothermal modeling and analysis methodology is covered in Section 2.2. Section 2.3 covers the classical static thermal analysis. The direct current (DC) and transient thermoelectric, self-heating, of the supply network interconnect to the thermal performance are covered in sub-section 2.4. Details of the system-level silicon characterization and measurements are outlined in sub-section 2.5. Results, findings, and observations are discussed in Section 3.

2.1 Device Description

The device is a high-efficiency, single channel, integrated FET, synchronous buck converter. It is suitable for point-of-load applications with 40A or lower output current in storage, telecom, and similar digital applications. The device features a proprietary D-CAP3™ mode control combined with an adaptive, constant on-time architecture. This combination is ideal for building modern high/low duty ratio, ultra-fast load step response DC-DC converters. The device includes a power stage consisting of a half-bridge (control FET and sync FET) and their respective drivers (located on the controller IC). The device is packaged in a 7mm×5mm, 40-pin, LQFN-CLIP (RVF) package. Figure 2 below shows a functional block diagram of the synchronous step-down converter device.

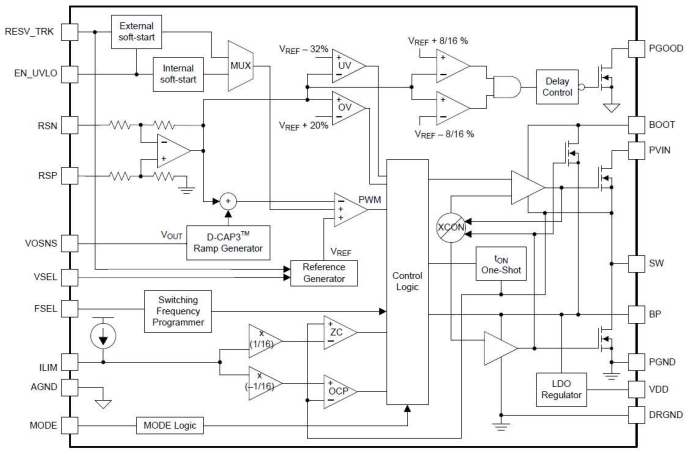


Figure 2. Functional block diagram of the synchronous step-down converter.

The device integrates two N-channel NexFET™ power MOSFETs rated at 40A. The converter input voltage range is from 1.5V up to 16V, and the VDD input voltage range is from 4.5V to 22V. The output voltage ranges from 0.6V to 5.5V. The drain-to-source breakdown voltage for these FETs is 25V DC. Its high-level of integration enables high power density. Additional details on the device can be found in reference [5].

2.2 ElectroThermal Modeling Methodology

The electrothermal modeling mathematical formulation is described in detail in [6-7]. A summary of the key fundamental steps are summarized below. The co-analysis methodology contains two functional modules: 1) physical field solvers and 2) equivalent circuit/network solver. The field solvers resolves the electrical and thermal field variables by the conventional 3D finite-element method, while the network solver can achieve accurate and efficient results by connecting the equivalent electrical, thermal and flow circuits that are extracted from the system through advanced numerical schemes including Finite-Element Analysis (FEA) and Computational Fluid Dynamics (CFD). The integrated equivalent network can then be solved by a generic circuit solver for steady-state and transient responses due to electrical and thermal interaction, and the heat dissipation to the surrounding fluid is also taken into account. Figure 3.0 below shows the electro-thermal co-analysis process flow.

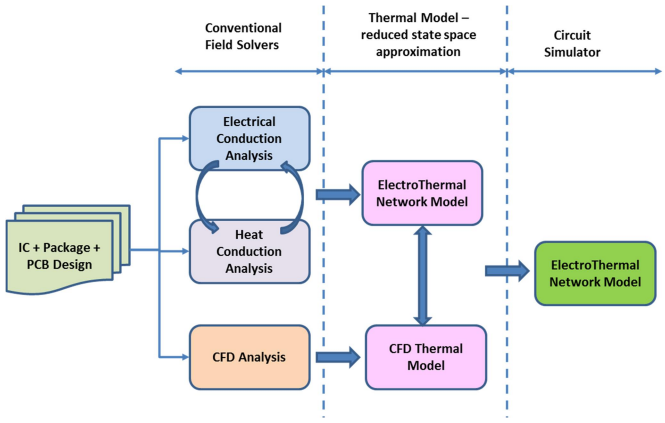


Figure 3. Electrothermal co-analysis methodology flow.

In the physical conventional field solvers the governing equations are solved iteratively based on the physics of electrical and thermal formulations respectively. For electrical and thermal solutions, the following equations are solved respectively:

$$\vec{J} = \overline{\overline{\sigma}} \cdot \vec{E} \tag{1}$$

$$\overline{\overline{\sigma}} = f(T) \tag{2}$$

$$\vec{J} \cdot \vec{E} = \frac{J^2}{\sigma} \tag{3}$$

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) + Q = \rho c \frac{\partial T}{\partial t} \tag{4}$$

Equation (1) is Ohm's law in point form, where J is a vector representing the current density, σ is a second order tensor with 9 components in general representing electrical conductivity, and E is a vector representing electrical field. The electrical conductivity tensor is a function of temperature as shown in equation (2). The Joule heating (power per unit volume) due to electrical current is expressed in equation (3). The thermal transport equation is given in equation (4), where T, k, ρ, c, Q indicate temperature, thermal conductivity, density, specific heat, and heat source respectively. To effectively solve the electrothermal-coupled equations, appropriate electrical and thermal boundary conditions are employed to achieve results that are coherent with physics and fit for realistic applications. Depending on the nature of problem of interest, different heat dissipation conditions may be applied at relevant surfaces or bodies where heat would transfer out of the system and to the environment. By coupling the FETs power dissipation (static/transient) switching profile to the rest of the system (i.e. package and PCB), the impact of temperature rise can be computed using the electro-thermal methodology develop here.

Once the electrothermal analysis is done, an equivalent thermal network model may be derived based on reduced state-space approximations as shown in Figure 3 above. Furthermore, to include the heat transfer to or from the environment surrounding the solid components, the third type of flow circuits was created using the Computational Fluid Dynamics (CFD) technique. Finally, by taking advantage of a generic circuit solver, both the static and transient responses of the system can be obtain in an efficient and accurate way, at any particular locations within the system. The electrothermal methodology described here has previously been employed successfully on other applications [8-10].

2.3 Static Thermal Analysis

One of the essential elements of numerical simulation is creating physical model that can accurately represent the objects or assemblies for simulation. In this study, the 3D geometrical models of package and PCB (EVM board) are generated based on the imported design files, respectively, without simplification by the simulation software. All the physical sizes and shapes of the components within the assembly reflect the true 3D dimensions. Material properties are also imported according to actual designs. Typical materials and their properties used are listed in Table 1.

Component	Electrical conductivity	Thermal conductivity	Density	Specific heat
	S/m	W/m-K	kg/m^3	J/kg-K
Lead frame	4.06E+07	284	8933	385
Wire	4.20E+07	315	19300	131
Solder	5.10E+06	23	8500	163
FET	Not specified	148	2330	712
Mold	Not specified	1	1200	1000
FR4	Not specified	0.3	1900	1200

Table 1. Material properties of components

There are mainly four heat sources with power consumption in the assembly: high-side FET, low-side FET, controller, and inductor. The power computation values at these four components can be obtained analytically or by measurements. After the 3D geometrical model, material properties, and heat input boundary conditions are adequately set up, the static thermal analysis will begin with CFD simulation based on specified flow conditions including thermal radiation. In the CFD simulation, the PCB is simplified as a single plate by averaging the material properties of the components within the PCB. Once the flow simulation is successfully performed, heat transfer coefficients at relevant heat-dissipating surfaces are extracted for further detailed analysis. Figure 4 and Figure 5 present CFD simulation results under natural convection and forced convection respectively.

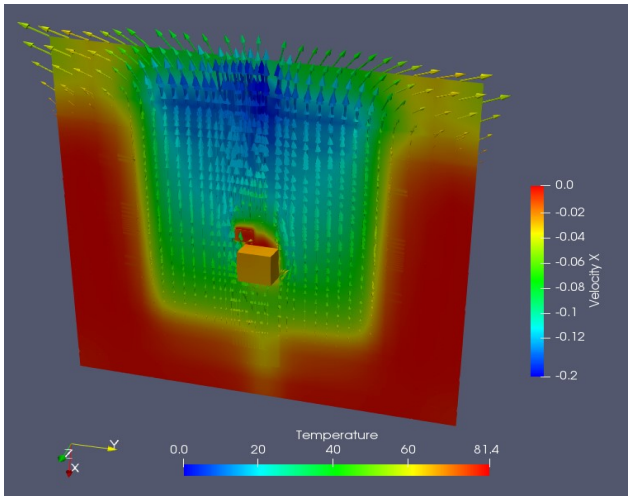


Figure 4. Natural convection: cross section of velocity field and component temperature distribution.

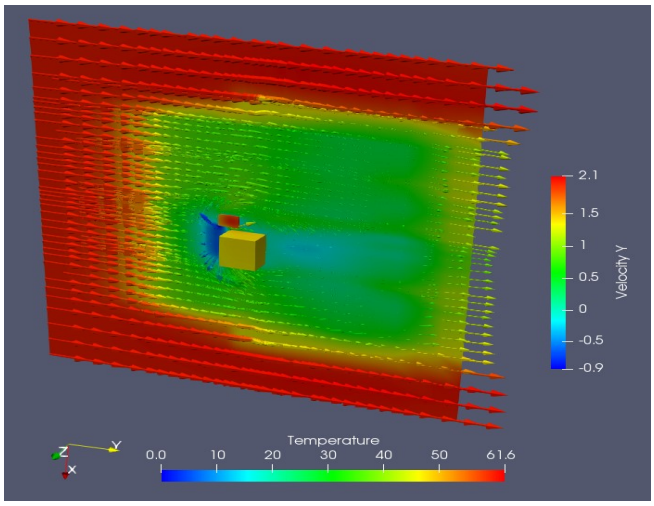


Figure 5. Forced convection (400 LFM airflow): cross section of velocity field and component temperature distribution.

Next, all the heat transfer coefficients obtained from CFD simulation are assigned to the 3D physical model for static thermal simulation using FEA, where all package and PCB details are retained. The thermal analysis based on 3D geometries and FEA can resolve temperature profiles of each component within the package and PCB, including FETs, wires, vias, and traces. The global locations of maximum temperature and local hot spots can also be identified. Figure 6 and Figure 7 give temperature distribution of thermal analysis results of the two flow convection cases described above. Note that the Joule heating due to electric currents are not modeled in this set of thermal-only simulation.

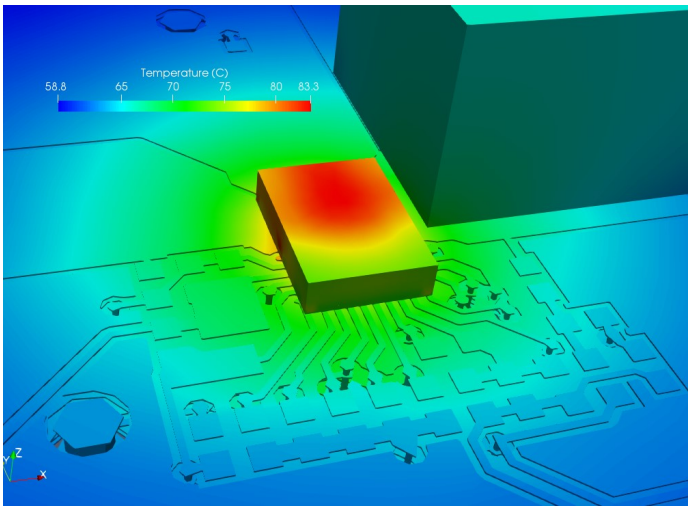


Figure 6. Natural convection: Temperature distribution of the assembly with PCB dielectric not shown.

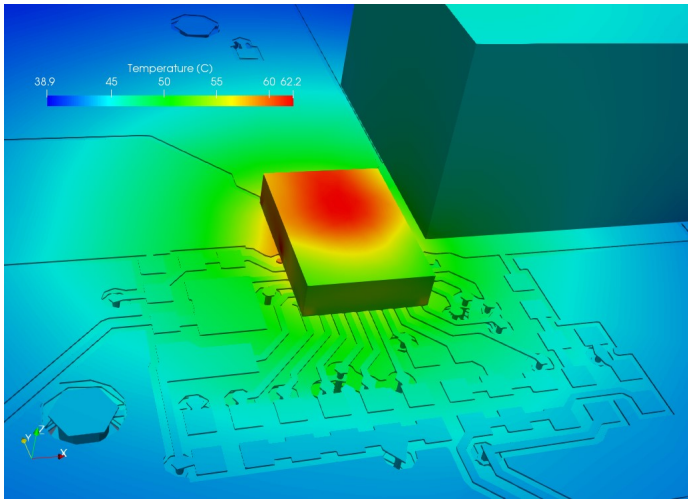


Figure 7. Forced convection (400 LFM airflow): Temperature distribution of the assembly with PCB dielectric not shown.

2.4 Static and Transient Electrothermal Analysis

The output current rating of the buck converter in this study is specified up to 40A. At high currents the power generation due to Joule heating within the PCB can be significant in real applications. Therefore, electrothermal co-simulation should be performed to evaluate the overall thermal response accommodating the power generation due to electrical current flowing through the PCB. In this section we present the results of static and transient electrothermal simulation using FEA based on the same 3D geometrical model, including 1) the voltage-in current flowing from the connector to the package and 2) the switch current from the package to voltage-out patch. The Joule heating due to these currents will modify the electrical resistance of the conductive paths and eventually reach thermal equilibrium. Figure 8 and Figure 9 illustrate the static electrothermal simulation results with the same setups as Figure 6 and Figure 7, except the Joule heating effect is modeled by applying appropriate currents to the traces on PCB. It is clear from the results when the Joule heating is included, the maximum temperature on the package top surface increases approximately 5~6°C under natural convection and 1~2°C under forced convection with airflow of 400 LFM. This is expected since the airflow of 400 LFM (~ 2 m/s) would be quite efficient in cooling the overall assembly with additional power generation by Joule heating on PCB.

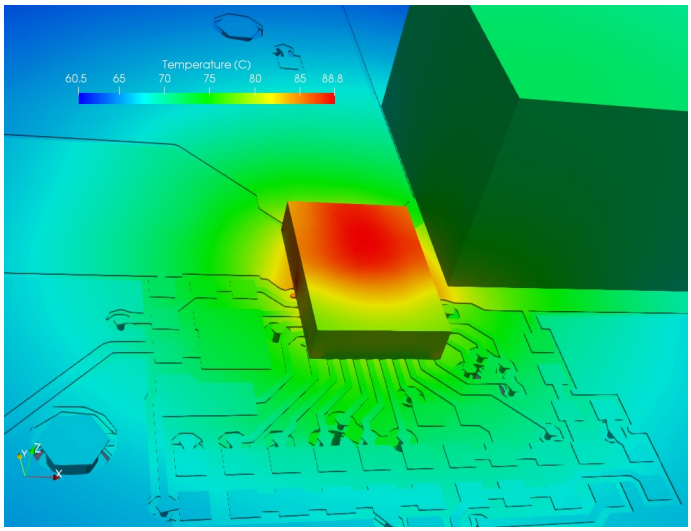


Figure 8. Natural convection: Temperature distribution of the assembly including Joule heating with PCB dielectric hidden.

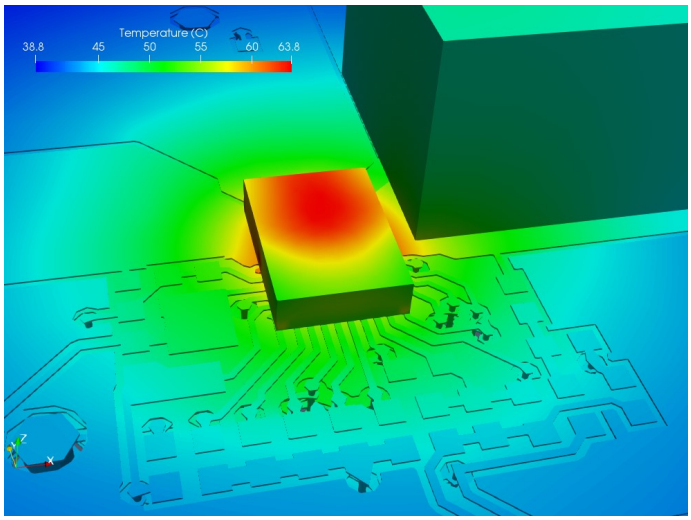
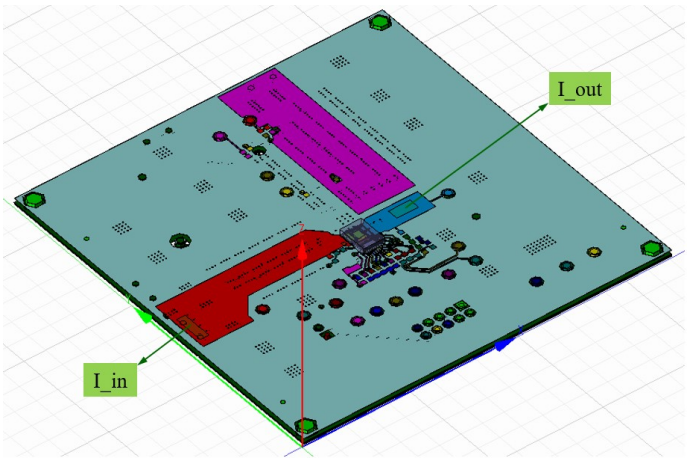


Figure 9. Forced convection: Temperature distribution of the assembly including Joule heating with PCB dielectric hidden.

Transient electrothermal simulation can also be conducted with given current waveforms applied to the relevant metals and traces in the PCB. In real applications, the input current flows into the package only during the time when the high-side FET is on, while the real-time output current can be treated as superimposing a ripple current on top of the average output current of interest. The duty cycle of the input current is essentially the voltage ratio of the output and input, namely V_out/V_in. Figure 10 gives an illustrative stimulus of the input current (I_in) and output current (I_out) that are used for the transient thermal simulation in this study. Note that for a typical switching frequency of 650 kHz, the period of one cycle shown in Figure 10 is about 1.5 us.



(The inductor is hidden for illustration)

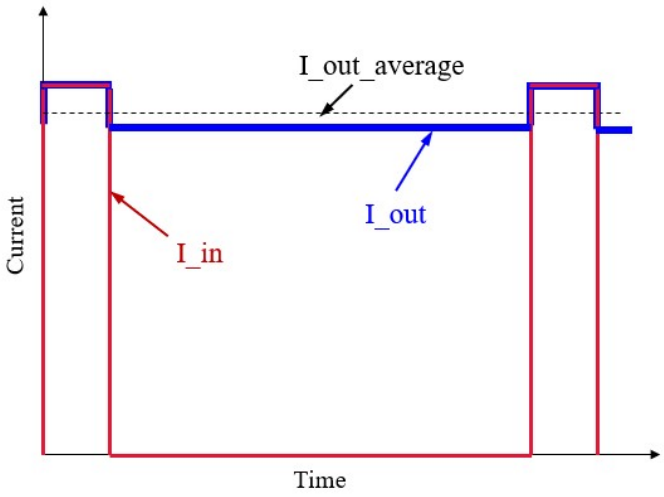


Figure 10. Application of current stimulus to PCB metals.

For the package-PCB assembly in this study, the total power input including the Joule heating is about 7 W, while the contribution of Joule heat in PCB is approximately 10% of the total power. When the stimulus currents are applied to the respective metals in PCB during the time on the order of micro-second, with the presence of other heat sources in the system, it is difficult to observe noticeable absolute temperature variations due to the stimulus currents. However, the relative temperature variations (versus ambient) after normalized by the maximum temperature increase during the time elapse of interest can be informative. Figure 11 shows the average temperatures at the package top surface during the first 100 cycles of the stimulus wave forms as given in Figure 10, with and without the Joule heating in PCB. It is clear the electrothermal simulation can capture the transient behaviors of temperature rising during the actual time scale. Also, starting from the onset stage the Joule heating is effective and contributes about 13% of the total temperature increase after the first 150 us of operation.

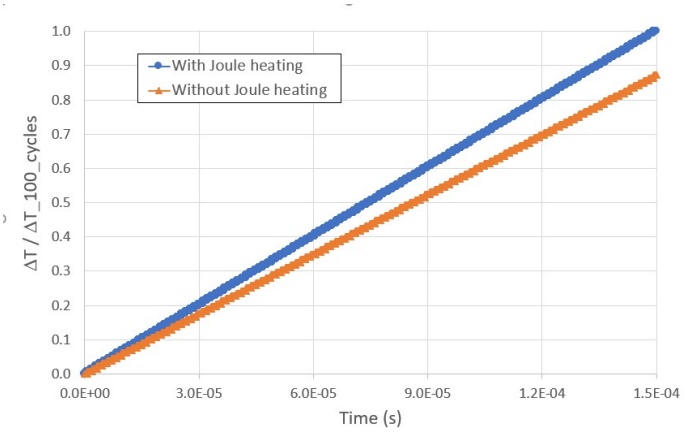


Figure 11. Transient electrothermal simulation with and without Joule heating during the first 100 cycles of stimulus currents.

2.5 Measurement Set-up

To validate the accuracy of the electrothermal analysis methodology, system-level measurements were performed on the evaluation module (EVM). A complete detailed description of the EVM is given in [11]. The EVM module was mounted inside a Venturi tunnel in order to provide a well-controlled environment for airflow and temperature measurements. Figure 12 shows the Venturi tunnel, anemometer (airflow meter), thermal camera placement, and EVM placement [12].

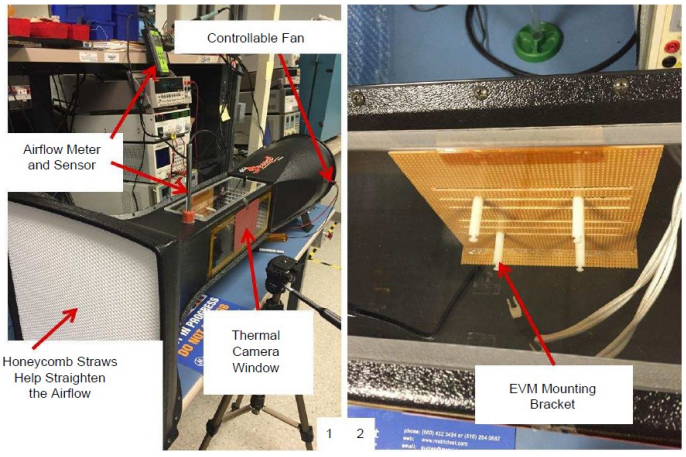


Figure 12. Measurement setup for thermal characterization.

The controllable fan is driven by an external motor from one side and the air exits at the other end. An anemometer's sensor is placed inside the tunnel to aid in calibrating the airflow in linear feet per minute (LFM), including 0 LFM. A cone was added to the thermal camera window to allow an unobstructed view between the thermal camera lens and the EVM, such that the thermal camera is placed about 1 foot from the EVM mounted inside the chamber.

3. RESULTS AND DISCUSSION

As discussed above, the higher temperature, due to increasing power density, has significant adverse impacts on the device performance and reliability. Electrothermal effects of the high current carrying interconnect on the device thermal performance needs to be considered early in the design phase. A predictive system-level thermal modeling serves to assess performance before hardware manufacturing. In this work, a system-level electrothermal modeling flow and methodology was developed and implemented on a real test case. As shown in Figure 12 and Figure 13, good correlation between simulation methodology and laboratory measurements was achieved respectively. The results of the two cases selected for thermal-only simulation and electrothermal simulation including Joule heating are summarized in Table 2.

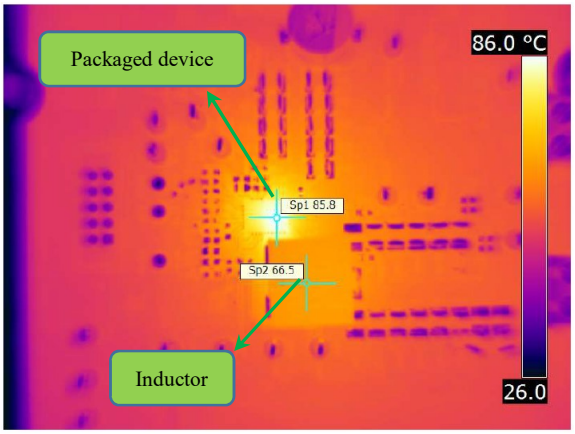


Figure 12. An example of a thermal IR plot taken at steady-state.

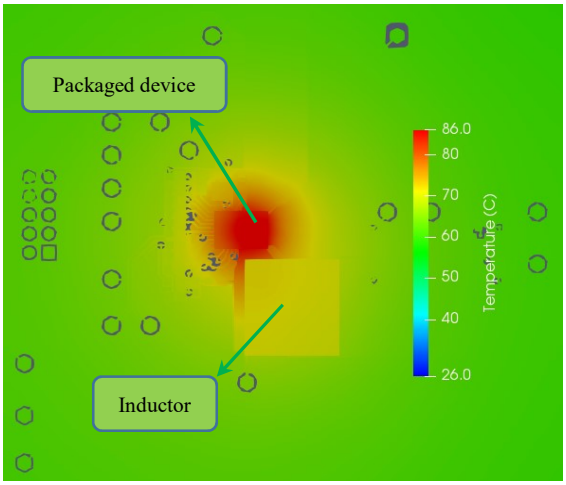


Figure 13. Electrothermal simulation results of the case in Figure 12.

Flow condition	T_ave on package (°C) without Joule heating	T_ave on package (°C) with Joule heating	T_reading (°C) IR Measured
Natural convection	79.3	84.6	85.8
Airflow (400 LFM)	58.0	59.2	59.8

Table 2. Summary of simulation and measurement results for ET analysis.

It is obvious that the Joule heating power on PCB has noticeable effect on the thermal profile. It shows that the average temperature on the package top surface increases 5.3 ºC and 1.2 ºC under natural and forced convections, respectively. These numbers correspond to approximately 9% and 4% of the total temperature increases in both conditions respectively. It is also interesting to note that the Joule heating on PCB plays a less important role affecting the thermal response in the forced convection, mainly because the 400 LFM airflow results in a sufficient cooling effect.

4. CONCLUSION

In this paper, we detailed the system electrothermal transient co-design modeling and silicon validation effort that led to the industry's first highly efficient, highest power density (40A) synchronous step-down converter. Good correlation was achieved, on the characterization evaluation module, between modeling/analysis methodology and silicon measurements for static thermal and electrothermal transient analyses. It is evident from the work carried out here that comprehending the system (viz. Die + Package + PCB) collectively is a must to ensure desired thermal performance. Additionally, it is critical to ensure that thermal analysis assessment is complemented by electrothermal analysis to properly capture the impact of the high current density on the system interconnect. The methodology developed here should be applied early in the design process/cycle of the device.

ACKNOWLEDGEMENTS

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