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Thermally Optimizing a High-Power PCB

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The growth of battery-powered applications is presenting new challenges for designers of electronic motor-driven solutions. Targeting higher performance and efficiency, the power stages of these products must manage high currents while meeting strict power dissipation and size requirements. This white paper illustrates a thermally aware workflow with the Cadence® Celsius™ Thermal Solver that was used to optimize the STMicroelectronics EVALSTDRIVE101 evaluation board deployed in battery-powered electronics. Detailed electrothermal co-simulations using the Celsius Thermal Solver during the routing phase enabled the designer to achieve maximum system performance in a short timeframe.

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Design Overview

The use of batteries for application power supplies requires lower operating voltage, usually in the range of a few tens of volts, because of the limited number of battery cells connected in a series. When applications require high power, above hundreds of watts, the management of currents flowing through the motor to drive the electronics becomes critical, to ensure overall system efficiency and reliability. Indeed, motor currents may exceed tens of amperes in such applications, which leads to increased power dissipation inside the inverter module, reducing its efficiency. More power to the electronic components of the inverter also results in higher temperatures, which could consequently degrade their performance over time and/or cause sudden breaks if going above maximum allowed ratings.

Several electronic components widely used in motor control systems are very sensitive to operating ambient temperature. For example, electrolytic capacitors typically used to stabilize the main supply voltage of the inverter are guaranteed by the manufacturer for a minimum number of hours without failures if their temperature remains below specific thresholds, but if operated above the threshold, a reduction in their average life should be expected.

Consequently, the optimization of thermal performance, in combination with a compact form factor, is a key aspect of the inverter design phase that can hide pitfalls if not properly addressed, resulting in underperforming products.

The current density in the PCB is also a critical factor when the current flows between different planes through via holes. Overstressing a single via connection due to poor placement could result in a sudden failure during operation, making analysis of this issue critical as well. A traditional approach to this problem would typically be the production of a first prototype once electrical signoff is completed and a direct check of its thermal performance by on-field validation. The design would then be successively refined, and new prototypes evaluated again in an iterative loop that should converge to the optimal result. The problem with this approach is that electrical and thermal evaluations are totally separated, and electrotheremal coupling effects are never addressed during the PCB design process, resulting in a long iteration time that directly impacts the time to market.

A more effective alternative method is to optimize the electrothermal performance of motor control systems by taking advantage of modern simulation technologies. STMicroelectronics, a leading manufacturer of industrial motor control integrated circuits (ICs), fine-tuned its EVALSTDRIVE101 evaluation board using the Celsius Thermal Solver, which provided—in a few minutes—a global and accurate assessment of design performance from both an electrical and thermal perspective. This tool dramatically simplified the inverter optimization process and enabled the designers to achieve a compact and reliable design in a short timeframe.

High-Power Demonstration Board

The EVALSTDRIVE101, in Figure 1, is a high-power demonstration board designed to drive three-phase brushless motors. It is based on the STDRIVE101 three-phase gate driver, and six STL110N10F7 power metal-oxide semiconductor field-effect transistors (MOSFETs), arranged into three half-bridges. Figure 2 shows the block diagram of the EVALSTDRIVE101.

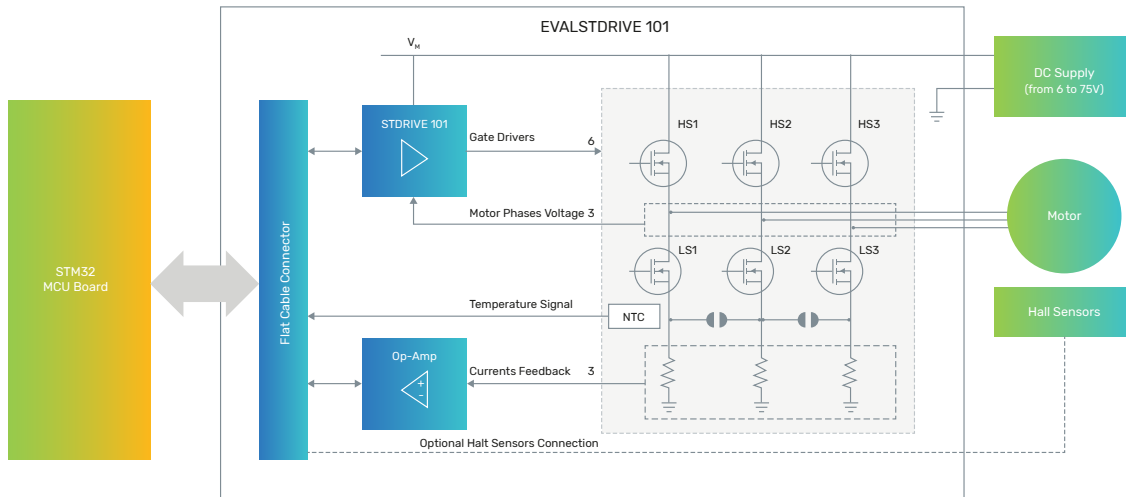*Figure 1: EVALSTDRIVE101 demonstration board*

Figure 2: EVALSTDRIVE101 basic block diagram

The EVALSTDRIVE101 is a four-layer board with 2oz copper, width of 11.4cm, and height of 9cm. Although the board has a custom aluminum heatsink for operations up to $20A_{rms}$, this document addresses operations without a heatsink. In this case, a maximum power of roughly 1kW can be delivered to the load with $15A_{rms}$ output current and supply voltage of 75V. The following maximum current rating was considered but the supply voltage was scaled down to 36V to better fit with battery-powered scenarios.

From a thermal perspective, the most critical part of the EVALSTDRIVE101 is the power stage area, which mainly includes power MOSFETs, shunt resistors, ceramic bypass capacitors, electrolytic bulk capacitors, and connectors. The layout of this part of the board, seen in Figures 3–6, covers roughly half of the overall PCB size, i.e., $50cm^2$. Special care was taken in the placement and routing of the MOSFETs, as these components are responsible for most of the power losses during inverter operations. The MOSFET drain terminal corresponds to the exposed pad of the package and provides the main link to the silicon substrate for heat dissipation. Consequently, the PCB copper area of all drain terminals was maximized on the top layer (as evident in Figure 3) focusing on the input net virtual machine (VM) bus and the three output nets (OUTU, OUTV, and OUTW). Copper areas of the VM and outputs available on the top layer were replicated and enlarged where possible for other layers to improve heat transmission toward the bottom board surface (Figures 4–6). In this way, both top and bottom surfaces of the board effectively contribute to heat dissipation by natural convection and radiation. The electrothermal connections between different layers are provided by vias of 0.5mm diameter that facilitate air flow and improve PCB cooling. The grid of vias was located right below the MOSFETs' exposed pads, but its diameter was reduced to 0.3mm to prevent solder paste reflows in the holes.
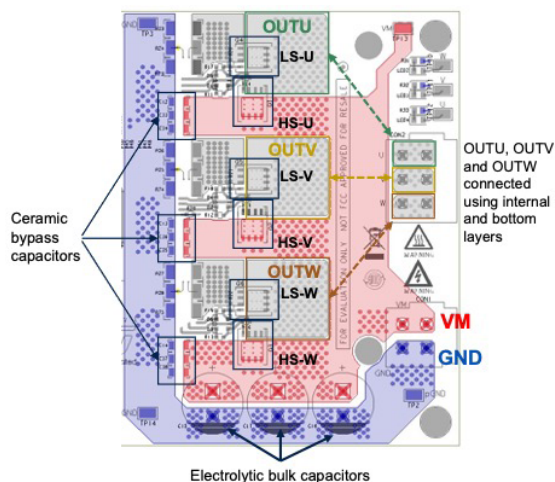

Figure 3: EVALSTDRIVE101 top-layer PCB

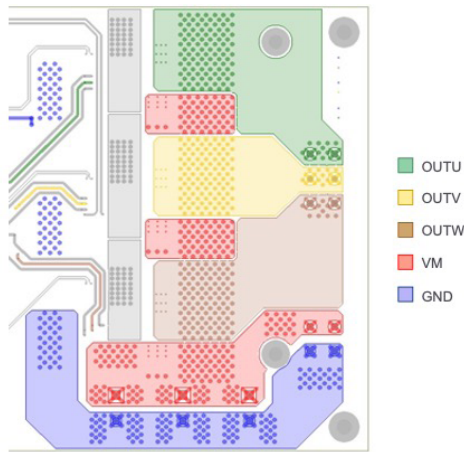*Figure 4: EVALSTDRIVE101 first inner-layer PCB*

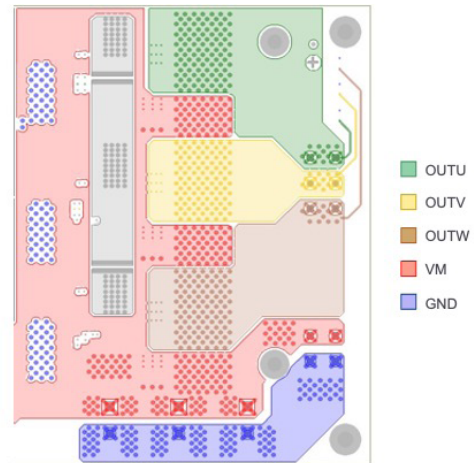Figure 5: EVALSTDRIVE101 second inner-layer PCB

Figure 6: EVALSTDRIVE101 bottom-layer PCB

In addition to the thermal perspective, the PCB routing also optimizes electrical performance. The lower panel of Figure 7 shows a placement detail of one half bridge; the MOSFETs, shunt resistors, and ceramic capacitors were placed close to each other to minimize current loops and were connected by large top traces to reduce inductive and resistive components positively affecting the radiated emission and noise level. The same reduction of parasitics was implemented for connections between STDRIVE101 gate driver and MOSFETs using incremented width of 0.7mm and two vias for each crossing of layers. This, together with a tuned polarization network of MOSFET gates made by a 33Ω resistor in parallel with a Schottky diode (shown in the upper panel of Figure 7), also allowed the designer to control the induced turn on effects and obtain the best motor control.
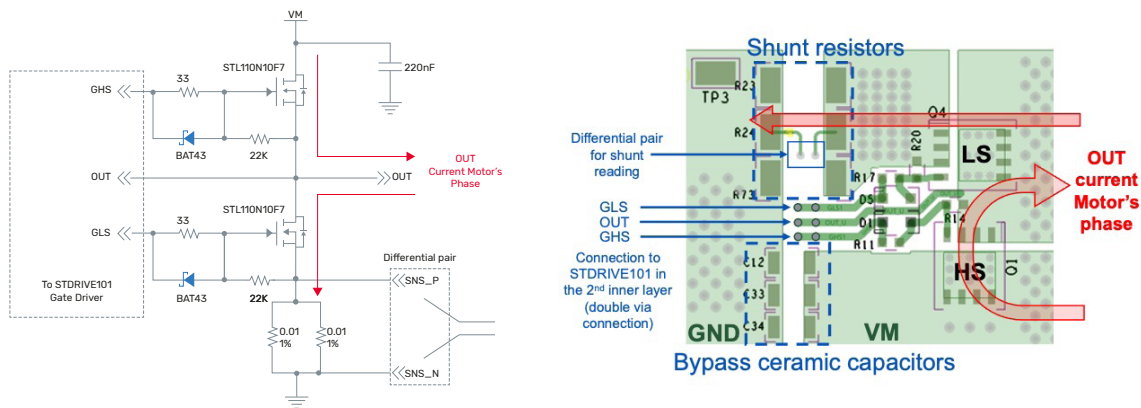

Figure 7: Schematic of one half-bridge in the EVALSTDRIVE101 and associated layout pattern

Celsius Thermal Solver Simulations

The Celsius Thermal Solver is the first complete electrothermal co-simulation solution for the full hierarchy of electronic systems from ICs to physical enclosures. Based on a production-proven, massively parallel architecture that delivers up to 10 times faster performance than legacy solutions without sacrificing accuracy, the Celsius Thermal Solver integrates with Cadence IC, package, and PCB implementation platforms. This enables new system analysis and design insights and empowers electrical design teams to detect and mitigate thermal issues early in the design process reducing electronic system development time.

By combining finite element analysis (FEA) for solid structures with computational fluid dynamics (CFD) for fluids, the Celsius Thermal Solver enables complete system analysis in a single tool. When using the Celsius Thermal Solver for PCB and IC

packaging, engineering teams can combine electrical and thermal analyses and simulate the flow of both current and heat for a more accurate system-level thermal simulation than legacy tools. In addition, the tool performs both static (steady-state) and dynamic (transient) electrothermal co-simulations based on the actual flow of electrical power in advanced 3D structures, providing visibility into real-world system behavior.

In addition to the heat generated locally around and underneath certain components at the PCB or IC package level due to component power consumption, the Celsius Thermal Solver can calculate the heat generated by the Joule effect due to the high currents flowing through the copper from the voltage regulator to the sinks. Local increase of the current density at the PCB package level will also introduce a local increase of the temperature (local hotspots). This makes it ideal for applications such as DC/DC converter PCB designs, switch mode power supply (SMPS) PCB designs, motor controlling applications, and any automotive and industrial types of applications dealing with high currents.

The Celsius Thermal Solver empowers electronics design teams to analyze thermal issues early and share ownership of thermal analysis, which reduces design respins, and enables new analysis and design insights not possible with legacy solutions. In addition, the tool accurately simulates large systems with detailed granularity for any object of interest and is the first solution capable of modeling structures as small as the IC and its power distribution, together with structures as large as the chassis.

The tool allows designers to directly import PCB and IC package layout files (.brd, .mcm, .sip, odb++ formats), even in draft versions. For example, a board such as the EVALSTDRIVE101, which consists of digital, analog, and power subdomains, can be optimized in the inverter section, even if the other parts are not yet defined. This feature allows obtaining immediate feedback when designing the PCB; therefore, it is possible to refine the layout step by step if critical issues are highlighted by simulations. This workflow was adopted to obtain the production-ready version of EVALSTDRIVE101 and involved iterative work mainly of changes in component placements, refinement of traces shapes, and inclusion/removal of vias.

Manufacturing Modifications

The Celsius Thermal Solver allows the designer to view and modify manufacturing parameters related to the PCB stackup and via characteristics such as plating, thickness, and filler. As Figure 8 shows, the EVALSTDRIVE101 has an overall PCB thickness of 1.58mm and consists of four copper layers that were optimized at 70μm (2oz/ft2). Copper thickness affects not only the electrical resistance of PCB traces, as explained in the previous section, but also their thermal resistance. A cross-section area of the traces can be increased with greater copper thickness to dissipate less power for the Joule effect, and to reduce thermal resistance and enable better heat spreading. However, copper thickness requires a tradeoff between performance versus PCB production cost and its minimization is deemed necessary.

The stackup settings allow to take into account production tolerances, usually 20% of nominal values, and simulate both in typical and worst-case condition to make the design even more robust. The physical properties of specified materials are automatically provided through the embedded library and their values are adapted according to operating conditions. Copper resistivity, for example, is increased with temperature to obtain better simulation results.

Layer #	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Fill-in Dielectric
1			Signal$TOP	0.07	copper		FR4
			Medium$41	0.25	FR4	0	
2			Signal$2INN	0.07	copper		FR4
			Medium$43	0.8	FR4	0	
3			Signal$3INN	0.07	copper		FR4
			Medium$45	0.25	FR4	0	
4			Signal$BOTTOM	0.07	copper		FR4

Figure 8: EVALSTDRIVE101 stackup

Electrical Analysis

Critical points in the current flow that could produce board overstress can be identified. The Celsius Thermal Solver allows designers to perform simulations that also include an electrical analysis of the system that provides current densities in traces and vias, as well as voltage drops. Such simulations require designers to define the PCB's current loops of interest using a circuit model for the system, made of current sinks, voltage sources, and resistances.

Current paths are not immediately defined for the inverter, as these depend on the operating condition of the three half-bridges. A full description of system behavior should include current exchange through the high-side or low-side MOSFET within one PWM cycle and account for realistic motor driving by amplitude modulation over time. However, it would be overde-tailed and of little use for a simulation that is intended to address longer time-scale phenomena. Figure 9 proposes a more convenient representation for each half-bridge. It consists simply of two constant current generators placed between the output and power supply connectors and three short circuits modeling the MOSFETs and shunt resistor. The two current loops provide good fitting with real case average currents throughout the supply rail and ground plain while the output path current is slightly oversized, a convenient operating condition for evaluating design robustness..
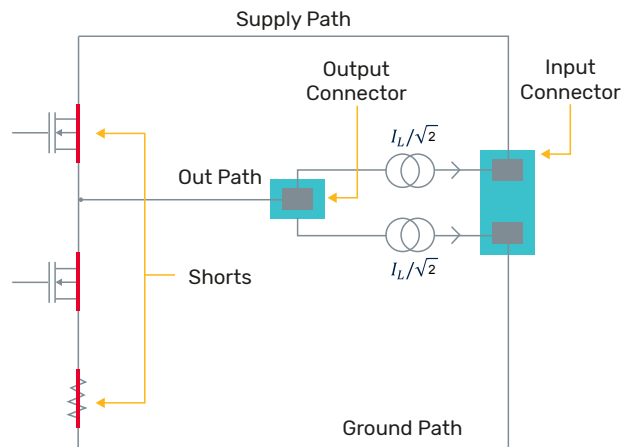

Figure 9: PCB current loop modeling

Figures 10 and 11 show the voltage drops and current density of the EVALSTDRIVE101 with I_L of 15A. Voltage drops simulated with the Celsius Thermal Solver with respect to ground reference highlight a particularly optimized layout with an absence of bottlenecks and well-balanced outputs at 28 mV, 25 mV, and 23 mV for U, V, and W. Output U shows the highest voltage drop while output W, the lowest of the three, which is an expected result, considering the relative path lengths from the power connector.
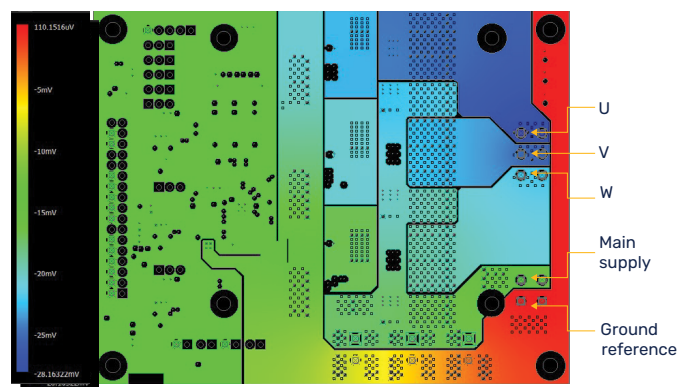

Figure 10: Voltage drops resulting from DC current loops

The Celsius Thermal Solver analysis of current distributions also confirmed the board's targeted performance (Figure 13). The currents are well distributed in the various paths and have an average density below 15A/mm^2, which is the recommended value for power traces sizing. Some red areas are highlighted in the proximity of the MOSFETs, the shunt resistors, and the connectors. These represent a higher current density, as the components' terminals are smaller than the underlying power traces. However, the maximum current density is far below the limit of 50A/mm^2, which could realistically lead to reliability issues [1].
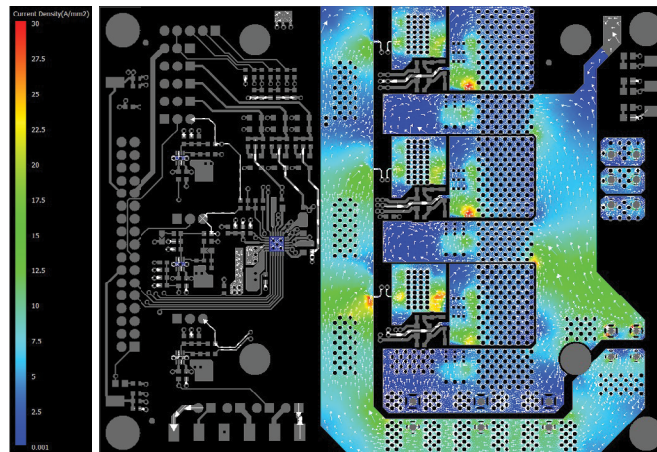
Figure 11: Current density resulting from DC current loops

Thermal Analysis

The Celsius Thermal Solver enables designers to set up and run steady-state or transient simulations. The former provides a single 2D temperature map for layers and components, while the latter provides maps for each simulated time instant and warmup curves at a cost of longer simulation time. Settings needed for steady-state simulation can be applied to a transient simulation; however, this additionally requires a definition of power dissipation functions for the components. Transient simulations are suitable when defining different operating states for the system with power sources not simultaneously active and also to assess the time needed to reach steady-state temperature. Simulations were done at an ambient temperature of 28°C with the heat transfer coefficient as boundary conditions and two-resistors thermal model for devices. These models were used instead of detailed thermal models such as Delphi, as they were directly available in the components' datasheets, although slightly sacrificing simulation accuracy [2]. The power loss of the inverter was estimated by simplified formulae considering the contribution of shunt resistors and power MOSFTEs due to conduction, switching, and the diode's drop.

Figure 12 provides the steady state results of the Celsius Thermal Solver for the EVALSTDRIVE101 and Figure 13 presents the transient simulation results. Step power functions are used in transient simulation to enable all the MOSEFTs and the shunt resistor at time zero.
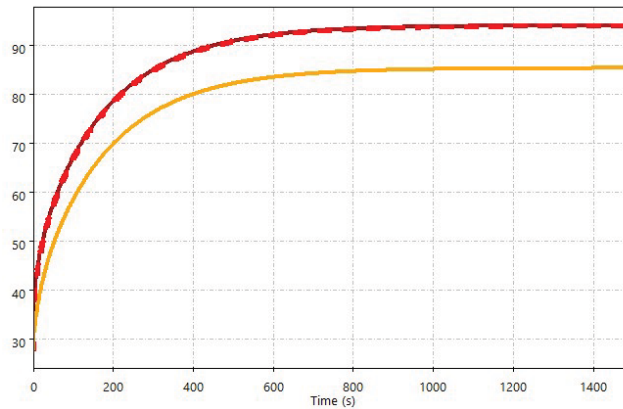

Figure 12: Result showing steady-state PCB simulated top layer temperature map
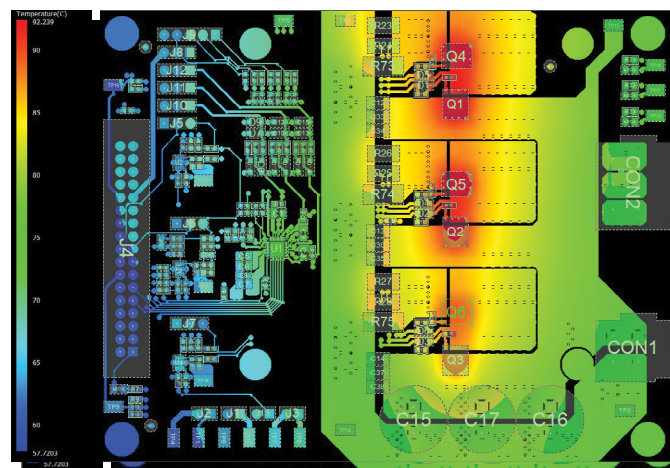
Figure 13: Result showing component warmup of the U half-bridge simulated thermal transient curve

From the Celsius Thermal Solver simulation results, the Q1 MOSFET was the hot spot on the board, at 94.06°C. Other components such as the Q4 MOSFET at R24 and R23 had a temperature of 93.99°C, 85.34°C, and 85.58°C, respectively.

Thermal Characterization: Simulation vs. Measured Data

For the thermal performance evaluation of the EVALSTDRIVE101 board, a setup was used consisting of three coils wired in a star configuration, namely, a three-phase load that emulates the motor. Each coil must have a saturation current compatible with the board rating, but the inductance or its parasitic resistance value need not be equivalent to that of the emulated motor. Indeed, it is more advantageous to have low parasitic resistance value for the coils, to considerably reduce the active power that would lead to unnecessary Joule effect heating inside the coils and obtain a lossless reactive power transfer between the board and the load, and vice versa.
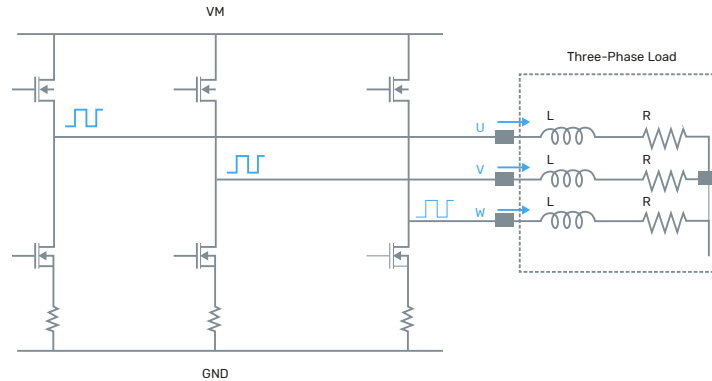

Figure 14. Three-phase load connected to the inverter

By applying three sinusoidal voltages that are out of phase by 120° to each other to the three terminals of the load, the three sinusoidal currents flow in the load. The three sinusoidal outputs are generated by modulating the PWM duty cycle around 50% mean value, as sinusoidal PWM modulation.

Equation 1 shows the peak amplitude of the current obtained.

Equation 1:

$I = V/\sqrt{(2\pi f L)^2 + R^2}$

▸ V is the peak amplitude of sinusoidal voltage applied to the load

▸ f is the frequency of sinusoidal voltage

▸ L is the inductance of one coil

▸ R is the resistance of one coil

With this method, the power stage works in an operating condition very close to the final motor driving application. Furthermore, the load current is stable and easy to configure by simply varying the frequency and applied voltage amplitude conversely to the motor driving, which needs appropriate closed-loop control algorithms.

Figure 15 shows the physical setup used for the thermal characterization of the EVALSTDRIVE101.
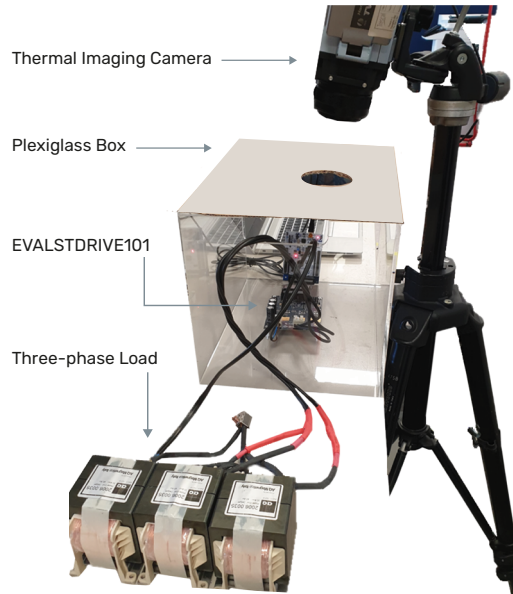

Figure 15: Setup for the thermal characterization of the board

The device was connected to a control board to generate the necessary driving signals and placed inside a plexiglass box to obtain system cooling by convection, without accidental air flow. Above the box is one thermal imaging camera, which frames the board through a hole in the cover of the box.

A three-phase load with inductance of 300µH and resistance of 25mΩ for each coil is connected to the board outputs, as previously described, and 36V is supplied to the system. Figure 16 shows the output current of $15A_{rms}$ obtained by applying three out-of-phase sinusoids with a frequency of 100Hz. The PWM applied by the half-bridges has a frequency of 20kHz and a dead time of 500ns.
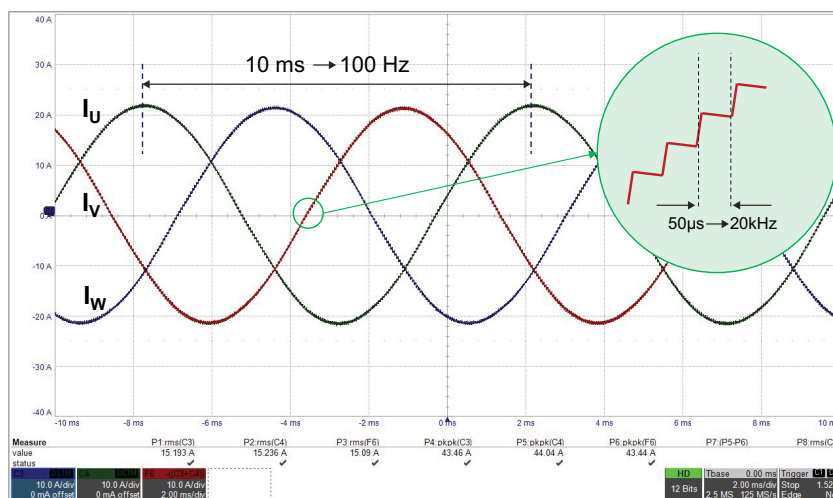

Figure 16: Output currents of the three phases using an SV-PWM modulation

Power Loss Measurement

One factor affecting the quality of the simulation results is certainly the data accuracy of the power dissipated by each device on the power stage. Measurement was made on the board, as described below, to evaluate the error in quantifying the dissipated power.

As the power dissipated by the board is the difference between the input power and the power delivered to the output load, it can be calculated as shown in Equation 2.

Equation 2:

$$P_{loss} = P_{in} - P_{out} = \overline{V_{in} \cdot I_{in}} - \sum_{i=1}^{3} \overline{(V_i - V_c) \cdot I_i}$$

- V_{in} is the input voltage of the board
- I_{in} is the input current
- V_i-V_c is the voltage drop on each coil, i.e. the difference between voltages of i-th output and center tap of the load
- I_i is the current flowing through the i-th coil

The measurement was made using an oscilloscope and applying the proper math functions to the waveforms: first the point-by-point product of the voltage and current was computed, then the power was averaged over an integer number of sinusoid cycles. Table 1 shows the measurement results at ambient temperature and at hot when the power stage reached the steady state condition. It also provides the overall value of power dissipated by the board estimated by formulae.

Table 1: Measured vs. Estimated Power Losses

Power	Measure @ Tamb	Measure @ Thot	Estimate
P_{in}	27.51	28.39	-
P_{out}^U	5.6	5.7	-
P_{out}^V	6.5	6.6	-
P_{out}^W	6.1	6.2	-
$P_{loss} = P_{in} - (P^U_{out} + P^V_{out} + P^W_{out})$	9.36	9.89	9.5

The results show very good matching between measurements and estimates, which is in line with introduced approximations. The formulae overestimates the measurement at room temperature by 1.5%, which provides roughly a 3.9% underestimate compared with hot condition data. This result is in line with the variability associated with the on-resistance of the MOSFETs and shunt resistors, as nominal values were used in the computations.

As expected, all power values were higher at hot than at room temperature, due to the increase in the resistances of the coils and MOSFETs with temperature. The data also shows a difference among the measured powers for the three outputs. This effect is due to the unbalancing of the three-phase load, because of slightly different values of L and R from coil to coil. This effect plays a marginal role, as the misalignment is lower than the one between the measurements and the estimate.

Temperature Results

The sinusoids generation and acquisition by the thermal imaging camera were simultaneously activated. The thermal imaging camera was previously configured to collect thermal images every 15 seconds and to include in every capture three temperature markers for components Q1, Q4, and R23, respectively, the high-side MOSFET, low-side MOSFET, and shunt resistor of the U half-bridge.

The system remained active until the steady-state condition was reached after about 25 minutes. The ambient temperature detected inside the box at the end of the test was about 28°C. Figure 17 shows the heating transient of the board that was derived from temperature markers and Figure 18 shows the final temperatures on the board.
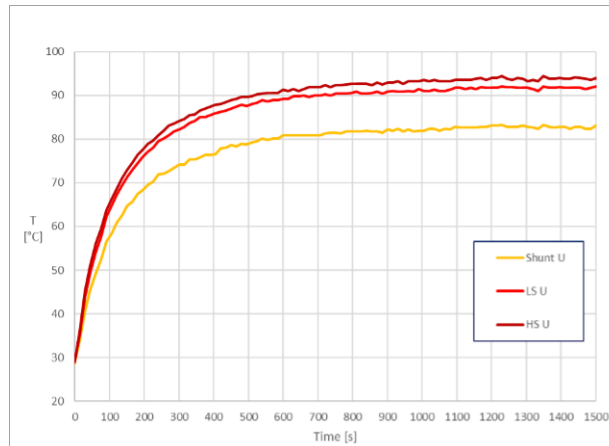
Figure 17: Measured thermal transient curve - EVALSTDRIVE101 warmup at 15A$_{rms}$
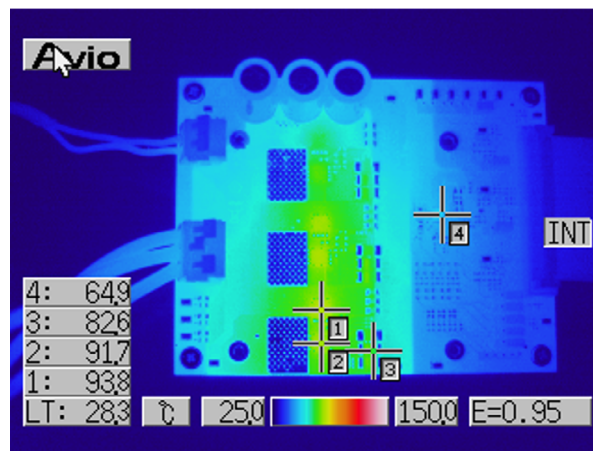

Figure 18: Thermal measurement - EVALSTDRIVE101 steady-state thermal image

The measurement showed that Q1 MOSFET was the hottest component of the entire board with a temperature of 93.8°C, while the Q4 MOSFET and R23 resistor reached 91.7°C and 82.6°C, respectively.

As discussed in the previous section, the Celsius Thermal Solver simulated the Q1 MOSFET temperature at 94.06°C, the Q4 MOSFET temperature at 93.99°C, and the R23 temperature at 85.58°C, giving very good matching with measurements.

Conclusion

STMicroelectronics recently released the EVALSTDRIVE101 evaluation board for use in high power and low voltage three-phase brushless motors for battery-powered applications. The board includes a compact power stage of only 50 cm^2, which can deliver over 1kW power and 15A$_{rms}$ current to the motor without heatsink or additional cooling.

Using different simulation features within Celsius Thermal Solver, it was possible not only to predict the temperature profile of the board and its hot spots on power stage components, but also to have a detailed description of voltage drops and current density along power traces, which could be problematic or not feasible at all to obtain by experimental measurements.

Celsius simulation outputs enabled fast optimization of the PCB layout, placement adjustments, and layout weakness corrections from early in the design to signoff. A thermal characterization with an infrared camera showed good agreement between simulated and measured steady state temperatures, as well as the transient temperature profile, validating outstanding performance of the board and effectiveness of the Celsius Thermal Solver in helping designers reduce design margin and achieve quick time to market.

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