USXGMII Ethernet PCS (PCSR_X) IP

Overview

With a comprehensive and rich feature set, multiple integration options, and flexible configurations, Cadence® IP are leading the way in mainstream Ethernet IP.

The Cadence USXGMII PCS (PCSR_X) IP provides the logic required to integrate a USXGMII, 5GBASE-R, or 10GBASE-R PCS into any system on chip (SoC).

Compliant with the Cisco Universal SXGMII Interface for a Single Multi-Gigabit Copper Network Port and IEEE 802.3 Clause 49 standards, the PCS IP has several optional features to customize the physical coding sublayer (PCS) for the specific needs of any application.

There are options to include support for BASE-R forward error correction (FEC), as per IEEE 802.3 Clause 74, and access to control and status registers through an APB interface.

The PCS IP is engineered to be quickly and easily integrated into any SoC, and to connect seamlessly to a Cadence or third-party MAC through a demultiplexed XGMII (64-bit data, 8-bit control, single clock-edge interface). Connection to the SerDes is through a configurable 16-, 20-, 32-, 40-, or 64-bit interface.

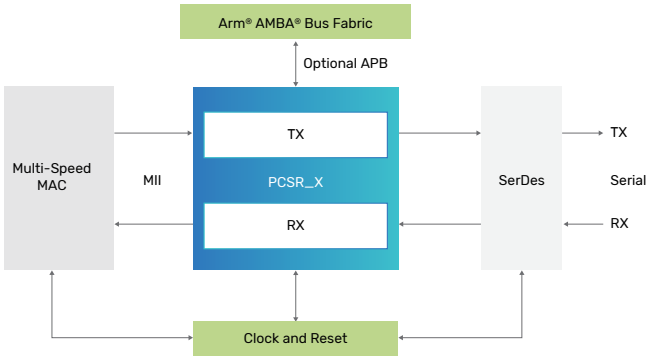

Figure 1: Example system-level block diagram

Benefits

- Ease of use—Customizable with easy integration
- Designed by an industry leader—Cadence is an active contributor to the IEEE 802.3 standards working groups

Key Features

- Multispeed single-port USXGMII interface
  - Supporting 100Mbps and 1/2.5/5/10Gbps Ethernet data rates
  - SerDes rates of 5.15625Gbps and 10.3125Gbps with data widths of 16, 20, 32, 40, and 64 bits
  - Clause 37-type auto-negotiation for link status notification
- Also configurable as a 5GBASE-R or 10GBASE-R PCS compliant with IEEE 802.3 Clauses 49 and 129
- ISO 26262 ASIL-B ready with automotive safety features (ASF)
- Optional BASE-R FEC (Clause 74)
- Programmable PRBS31 and PRBS9 (Clause 68) test pattern generators and error checkers
- Scrambled idle test pattern generator and checker
- Square wave test pattern generator
- 64b/66b encoding/decoding
- Optional clock tolerance compensation on receive (RX) path
- Connection to a 10 Gigabit Ethernet MAC using a demultiplexed XGMII interface
- Data scrambling on transmit (TX) path and descrambling on RX path
- Optional APB control status register interface

Product Details

The Cadence USXGMII PCS (PCSR_X) IP is designed as an on-chip PCS for connecting an Ethernet MAC to a 5.15625Gbps or 10.3125Gbps SerDes. It supplies all required PCS functionality as well as some physical medium attachment (PMA) features.

It includes all the functionality of a standard 10GBASE-R PCS along with functionality to replicate 66-bit encoded blocks to adapt slower Ethernet data rates to the fixed speed of the SerDes. It also includes functionality for a modified Clause 37 auto-negotiation state machine to pass status information from the PHY to the MAC as defined by the USXGMII standard. (The packet control header (PCH) non-standard preamble as described in the USXGMII standard is not supported.)

The 64b/66b encoder takes eight octets (64-bits) from the demultiplexed XGMII and codes them into a single 66-bit block. The 66b/64b decoder takes 66-bit blocks from the gearbox or, after FEC transcoding and error correction, from the optional FEC block, and decodes the block into eight octets.

The data scrambler uses the algorithm defined in IEEE 802.3 Clause 49.2.6 to scramble the data after line coding. The data descrambler reverses the scrambling algorithm applied by the data scrambler in accordance with IEEE 802.3 Clause 49.2.10.

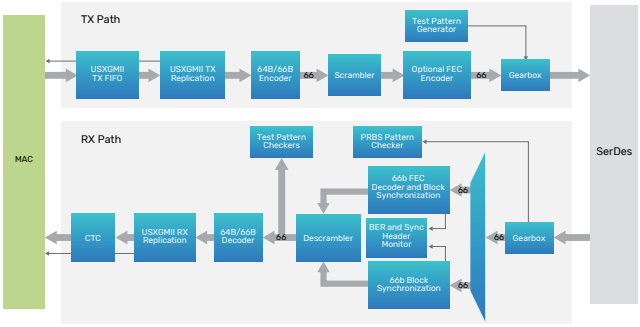

Figure 2: IP-level block diagram

The gearbox converts signals between the 66-bit width used by the PCS and the bit width used by the 10G SerDes. The SerDes interface is configurable to whatever width the SerDes requires. An optional APB interface is also available for controlling the PCS and returning status.

The IP has built-in PRBS31 and PRBS9 (Clause 68) test pattern generators and checkers for testing the integrity of the link. A separate square wave pattern generator is also included.

Related Products

- Verification IP for Ethernet

Deliverables

- Documentation—Integration guide, user guide, quick start guide, and release notes
- Functional Safety—safety manual including FMEDA report and description of automotive safety features
- Synthesizable Verilog HDL
- Synthesis scripts
- Sample Verilog testbench with confidence tests

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