

## Overview

Cadence is a leader in semiconductor IP addressing hyperscale computing, enterprise, data center, automotive, and artificial intelligence/machine learning (AI/ML) applications. Our IP are available in advanced-process nodes ranging from 28nm to 3nm—all silicon verified in leading-edge foundry processes. Our memory IP portfolio spans DDR, LPDDR, and GDDR. The Cadence® IP family for PCI Express® (PCIe®) includes support for PCIe 6.0/5.0/4.0/3.1/2.1/1.1 as well as Computer Express Link (CXL). Our high-speed PAM4 SerDes in 112G and 56G address the needs of hyperscaler designing products for 400G and 800G networks as well as 5G applications. Our UCIe and UltraLink die-to-die (D2D) connectivity products address chiplets, multi-chip, and multi-die implementation in 2D standard packages or 2.5D advanced packages, and are ideally suited for disaggregated CPUs, GPUs, and complex heterogenous SoCs that are pushing the limits of Moore's Law.

		Enterprise	Hyperscale	Comms	Aerospace/ Defense	Automotive	Mobile	Industrial	Consumer
	224G-LR (200G/400G/800G/1.6T)	•	•	•	•			•	
	112G-ELR (100G/200G/400G/800G)	•	•	•	•			•	
,D2D	56G-LR (100G/200G/400G)	•	•	•	•				
Ethernet/PCIe/CXL/CPRI/D2D	25G-KR (25G/100G)	•	•	•					
XL/	16G UCle™	•	•		•				
le/0	40G UltraLink™ D2D	•	•		•				
t/PC	10GBase-KR	•		•	•	•		•	•
rne	USXGMII/QSGMII/SGMII	•		•	•	•		•	•
Ethe	PCIe 6.0/CXL	•	•	•	•	•		•	•
	PCIe 5.0/CXL	•	•	•	•	•	•	•	•
	PCIe 4.0	•	•	•	•	•	•	•	•
	PCIe 3.1	•	•	•	•	•	•	•	•
	USB4	•	•	•	•	•	•	•	•
	USB3.0/3.1/3.2	•	•	•	•	•	•	•	•
/DP	USB2.0/eUSB	•	•	•	•	•	•	•	•
USB/MIPI/SATA/DP	MIPI®D-PHY <sup>sm</sup>					•	•	•	•
S/Ic	MIPI®C/D-PHYsm					•	•	•	•
₩	MIPI SoundWire®						•		•
USB	MIPI I3C®	•	•	•	•	•	•	•	•
	SATA	•						•	•
	DP					•	•	•	•
~	DDR5	•	•	•	•			•	•
300	DDR4	•	•	•	•		•	•	•
DR/(	DDR3						•	•	•
LPD	LPDDR5/5X	•	•	•	•	•	•	•	•
DDR/LPDDR/GDDR	LPDDR4/4X	•	•	•	•	•	•	•	•
	GDDR6	•	•			•			
je je	xSPI				•	•	•	•	•
Storage	SD/eMMC					•	•	•	•
St	ONFi/Toggle	•				•	•	•	•

Table 1: Apps versus IP titles

## **Advanced SerDes**

We offer various complete, configurable, and production-proven interface protocols, such as Ethernet, PCIe, CXL, D2D, USB, SATA, DP, and MIPI. All these solutions are designed with your SoC in mind, eliminating the need for you to design around our IP. Moreover, our IP can be delivered with a complement of Cadence Verification IP (VIP) and models. Pre-verified solutions save time and effort and allow you to focus on your innovative designs.

						тѕмс			Sam	sung			bal dries	имс		ѕміс				
	Protocol	Data	7.‡	FC					4 0		9	ω	7	υ Ω	,	7	5	87	шu	Ctrl
		Rate	22ULP/ 28HPC+	16/12 FFC	N7	9N	NS	N5A	N4P	N3E		LPP		LPE	<u>-</u>	LP+	HPC	HPC+	14/12 nm	
	224G-LR (200G/400G/ 800G/1.6T)	212.5 Gbps								0										0
	112G-ELR (100G/200G/ 400G/800G)	106.25 Gbps			•	•	•		•	0				0						•
	56G-LR (100G/200G/400G)	53.125 Gbps			•	•														•
rnet	25G-KR (25G/100G)	25.78125 Gbps			•	•	•		0	0										•
Ethernet	10GBase-KR	10.3125 Gbps	•	•	•	•					•	o								•
	USXGMII	10.3125 Gbps		•	•	•	•		0	0									•	•
	QSGMII	5Gbps	•	•	•	•	•		0	0									•	•
	SGMII	1.25Gbps	•	•	•	•	•		0	0									•	•
	Multi-Speed Ethernet Controller (soft IP)	10M/ 100M/1G																		•
	PCIe 6.0/CXL	64Gbps					0			0				0						•
×	PCIe 5.0/CXL	32Gbps			•	•	•	0	0	0									0	•
PCIe and CXL	PCIe 4.0	16Gbps		•	•	•					•				•	0			0	•
le ar	PCIe 3.1	8Gbps	•	•	•	•	•		0	0			•	0			•	•	•	•
PC	PCIe 2.1	5Gbps	•	•	•	•	•		0	0	•	0	•	•	•	0	•	•	•	•
	PCIe 1.1	2.5Gbps	•	•	•	•	•		0	0	•	0	•	•	•	0	•	•	•	•
CPRI/ eCPRI	CPRI Option10	24.33 Gbps			•	•													0	
	40G UltraLink D2D	40Gbps			•	•	•						•			•			0	•
D2D	UCIe	16Gbps			o		0			0										0

Table 2: IP for Ethernet, PCIe and CXL, and D2D connectivity

- Ready for design
- In progress

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		тѕмс								Samsung							
	Protocol	Data Rate	16	12						28	10	8	7	5	14	C	trl
		Nate	FF	С	N7	N6	N5	N5A	N4P	FD-SOI		LPP		LPE	nm		
	USB4	20Gbps	0	0	0	0	0		0								
	USB 3.0	5Gbps	•	•	•	•	•		0	•	•	0	•	•	•		xHCI Host
	USB 3.0	5Gbps	•	•	•	•	•		0	•	•	0	•	•	•	•	DRD
USB	USB 3.1	10Gbps	•	•	•	•	•	0	0		•	0	•	•	•	•	ä
Š	USB 2.0	480Mbps	•	•	•	•			0	•	•	0	•	0	•	•	g l
	USB 3.0	5Gbps	•	•	•	•	•		0		•	0	•	•	•	•	Device
	USB 3.1	10Gbps	•	•	•	•	•	0	0		•	0	•	•	•	•	
	USB 2.0	480Mbps	•	•	•	•	•		0	•	•	0	•	0	•	•	ОТС
	D-PHY v1.2	2.5Gbps	•	•	•											•	
	C/D PHY 1.0/1.2	3.5Gsps/2.5Gbps	0	0												•	CS12 DSI
MP	C/D PHY 1.1/2.1	6Gsps/4.5Gbps			0	0	0		0							•	
	SoundWire v1.2	12MHz				•										•	
	13C	Soft IP														•	CSI2 DSI
SATA	SATA 3.0 Host	6.0Gbps	•	•	•	•	•		0						•		
DP/ eDP	DP 1.4 TX	8.1Gbps	•	•	•	•	•		0						•		

Table 3: IP for USB, MIPI, SATA, and DP

Ready for designIn progress

## **Advanced Memory**

We offer the broadest and most configurable portfolio of the industry's widely used memory and storage protocols. The Cadence Denali® Memory IP gives you the added value of multi-standard DDR support by providing controller IP that supports DDR5, DDR4, DDR3, DDR3L, LPDDR5X/5, LPDDR4X/4, and LPDDR3 as a single IP solution, as well as GDDR6. We also offer advanced memory IP solutions created by the best experts in the field to provide you with the controller, PHY, and VIP you need for your design.

						TS	мс					5	Sam	sunç	9		Global Foundries		SMIC	
	Protocols	Perf.	22	28	16	12			4P	ш	41	10	œ	7	4	വ	,	7	E L	Ctrl
		(Mbps)	ULP	HPC+		F 5	N 7	9 N	N2/N	N5/N4P N3E						LPE	ط <del>أ</del>		14/12 nm	
		8,800+							0	0										0
	DDR5/4	6,400+							0	0										0
	DDR3/4	5,600							•							•				•
- AC		4,800			•	•	•	•	•					•				•	•	•
DDR/LPDDR	DDR5/4, LPDDR5/4X combo	5,600					0	0	•						0					•
JR/L	LPDDR5/4X	6,400					•	•	0											•
	LPDDR5X/5	8,533+							0	0										0
	LPDDR4/3/DDR4/3[L]	4,266	•	•	•	•	•	•											•	•
	LPDDR4/4X/3/DDR4	4,266			•		•	•											•	•
	DDR4/3[L]	3,200	•	•	•	•	•	•											•	•
DR	CDDD4 DHV	16G					•	•	0		•			•		•	0	0		•
GD	GDDR6 PHY	20G+							•											•

Table 4: IP for DDR, LPDDR, GDDR, and HBM

- Ready for design
- In progress

## Storage IP

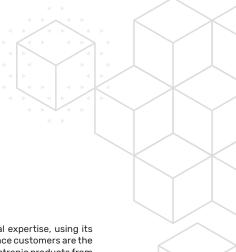
Cadence storage IP solutions consist of three popular technologies: NAND Flash, SD/eMMC, and xSPI. These memory technologies address the needs of a broad range of market requirements. The Cadence NAND Flash Controller IP supports all major NAND Flash manufacturers handling asynchronous devices and meets standards such as ONFI5.x, ONFI4.x, ONFI 3.x, ONFI 2, ONFI 1, Toggle 1, or Toggle 2. The Cadence NAND Flash PHY IP supports speeds up to DDR3600 for most process nodes, and is available as soft IP with a delay-locked loop (DLL), a firm PHY, or a hard PHY for your specific process and library. Ask your Cadence representative about hard PHYs at higher speeds. The Cadence SD/eMMC IP is compliant with the latest versions of Secure Digital and Embedded Multimedia Memory Card standards, which makes our IP the perfect choice for both high-performance and low-power solutions. The Cadence xSPI IP is compliant with a range of serial standards, including xSPI, Octal SPI (OSPI), Quad SPI (QSPI), NOR Flash, and some RAM, NAND, and novel NVM technologies.

	Protocol	Soft PHY	TSMC 16/12 FFC	TSMC N7	TSMC N5	Ctrl
xSPI	xSPI - Supports multiple serial standards including OSPI and QSPI	•				•
MMC	SD 4.0/eMMC5.1	•				•
SD/eMMC	SD 6.0/eMMC5.1	•				•
9	ONFI4.x/Toggle 2	•				•
NAND	ONFi 5.x Firm PHY and I/O / Hard PHY		•	0	0	
Combo	Multistandard PHY supporting NAND, SD/eMMC, and xSPI	•				

<sup>\*</sup> Information provided in this brochure is for planning purposes only. Contact Cadence to confirm availability and specifications.

Table 5: IP for storage

- Ready for design
- In progress





Cadence is a pivotal leader in electronic systems design and computational expertise, using its Intelligent System Design strategy to turn design concepts into reality. Cadence customers are the world's most creative and innovative companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic applications. www.cadence.com