DESIGN IP BROCHURE

Controller IP for PCIe 5.0

Overview

The cloud computing revolution and proliferation of mobile devices is increasing data traffic and driving changes in data center device architecture. High-speed communication within and between servers and storage is necessary to support video, as well as the growth of dataset and associated analytics. The PCI Express® (PCIe®) standard is constantly evolving, striving to double bandwidth every few years to support the required increase in data throughput.

The Cadence® Controller IP for PCIe 5.0 provides the logic required to integrate a root complex (RC), endpoint (EP), or dual mode (DM) controller into any system-on-chip (SoC).

Compliant with PCIe 5.0, 4.0, 3.1, 2.1, and 1.1 specifications, the Controller IP has over 100 configuration features to customize the controller to the specific needs of any computing, networking, or storage application.

The Controller IP is engineered to quickly and easily integrate into any SoC and connect seamlessly to a Cadence or third-party PIPE 5.x- or PIPE 4.4.1-compliant PHY. Client applications access the controller through an industry-standard Arm® AMBA® 3 or 4 AXI interface or through a native Cadence Host Adaptation Layer (HAL/HLS) interface.

The Controller IP has been extensively tested using Cadence Verification IP (VIP) for PCIe as well as the Cadence Palladium® series verification computing platform. Cadence offers a comprehensive IP solution that is in volume production and successfully implemented in dozens of applications.

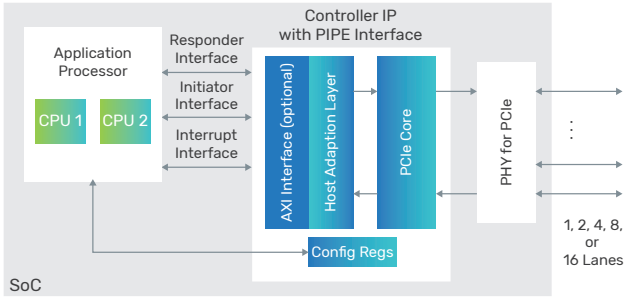

Figure 1: Example system-level block diagram

Benefits

- Superscalar design for high throughput and low latency
- Configured to your specific needs – efficient implementation with minimal gate count
- Optimized for use with Cadence PHY

Product Details

The Controller IP is designed for use in ASIC SoC devices to provide an industry-standard interface to the PCIe link. It utilizes a highly scalable, pipelined architecture and a small silicon footprint.

Key Features

- Compliant with PCIe 5.0, 4.0, 3.1, 2.1, and 1.1 specifications
- 32/16b interface for 500MHz or 1GHz core operation
- Modes supported: Root Complex, EndPoint, or Dual Mode
- SR-IOV and multifurcation options
- Support for up to 4K payload size and 256 functions
- ECNs, Error Counters, ECRC, and end-to-end datapath parity support

PCIe Core

The PCIe core implements the physical layer, data link layer, and transaction layer of the PCIe protocol. The physical layer provides the PIPE interface to easily connect to any PCIe-compliant PHY device, and the HAL/HLS or optional AMBA 3/4 AXI interface provides connectivity to the client. The PCIe core manages the functions of the PCIe protocol including data deskewing, replay buffers, flow control, and CRC check and generation.

Configuration Registers

The Controller IP implements a complete set of PCIe base configuration registers and PCIe capability registers for PCIe power management, MSI and MSI-X, PCIe, and Slot ID. In addition, the configuration registers have PCIe extended registers for advanced error reporting. APB is available to access configuration and internal registers within the controller.

Client Interface

The client interface is implemented to support AMBA 3/4 AXI or HAL/HLS. The client interface consists of separate initiator and responder interfaces.

The responder interface is used for receiving transactions from the link and sending responses back. With the initiator interface, the client or DMA engine can initiate a packet transfer to the PCIe link. The datapath width on the client interface is configurable to 32-, 64-, or 128-bits depending upon the core generation and link width.

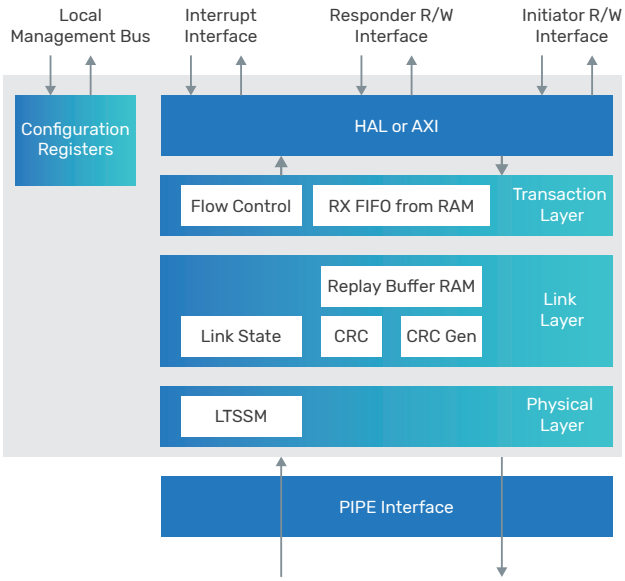

Figure 2: IP-level block diagram

PIPE Interface

The PIPE 5.x and 4.4.1 family of specifications are the industry-standard PHY interface for the PCIe architecture v1.1, v2.1, v3.1, v4.0, and v5.0. In addition, the PIPE interface has an optional PCLK input for running the PIPE interface at a different clock rate than the core.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and systems and peripherals IP.

Availability

- Controller IP for PCIe 5.0 x4 lanes
- Controller IP for PCIe 5.0 x8 lanes
- Controller IP for PCIe 5.0 x16 lanes

Related Products

- PHY IP for PCIe 5.0
- PHY IP for PCIe 4.0
- PHY IP for PCIe 3.1
- Controller IP for PCIe 4.0
- Controller IP for PCIe 3.1
- Integrated Solution IP for PCIe

Deliverables

- Clean, readable, synthesizable RTL Verilog files
- Verification testbench example with integrated stimulus and monitors
- Verification test-plan and reports
- Comprehensive user guide
- Register descriptions
- Synthesis and STA scripts

For more information, visit cadence.com/designip

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