DESIGN IP BROCHURE

cadence®

Controller IP for PCIe 3.1

Overview

Modern consumers need mobile devices capable of providing enough processing power to perform tasks like making payments, playing and streaming HD videos, and playing demanding video games. Mobile phones and tablets are first-choice computers for many, therefore the amount of processed mobile data is increasing on a daily basis. To serve them, operations must be performed effectively on a smaller area, and by using advanced nodes for good speeds.

The Cadence® Controller IP for PCIe® 3.1 is a solution created for mobile applications that provides the means for these goals. It has the logic required to integrate a Root Complex (RC), Endpoint (EP), or Dual Mode (DM) controller into any system on chip (SoC).

Compliant with PCI Express® 3.1, 2.1, and 1.1 specifications, the Controller IP has over then 100 configuration features, and 1500+ input parameters, to customize the controller to the specific needs of any application.

The Controller IP is architected to quickly and easily integrate into any SoC, and connect seamlessly to a Cadence or third-party PIPE 4.2-compliant PHY. Client applications access the controller through the industry-standard Arm® AMBA® 3 or 4 AXI interface or through Cadence's native Host Adaptation Layer (HAL) interface.

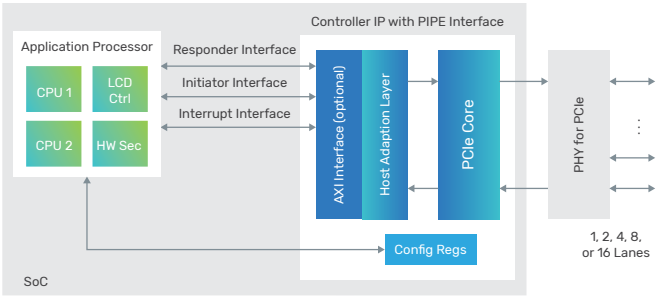

Figure 1: Example system-level block diagram

Benefits

- Low-risk solutions—silicon-proven design
- Ease-of-use—customizable with easy integration
- High performance—benchmarked at 95% of theoretical maximum throughput

Key Features

- Compliant with PCIe 3.1, 2.1, and 1.1 specifications
- Up to 256 PCI Physical Functions or Virtual Functions with Alternative Requester ID Interpretation support
- Configurable as Root Complex, Endpoint, or Dual Mode
- AMBA 3/4 AXI and HAL client interface options
- Ultra-low transmit/receive latency and high bandwidth
- 16- or 32-bit PIPE 4.2 interface
- Supports x1, x2, x4, x8, and x16 configurations
- Available separate PCLK input for PIPE interface
- Single-Root I/O Virtualization (SR-IOV) and bifurcation options
- Optional enhanced power management control

Product Details

The Controller IP can be customized as a RC, EP or operate in DM, supporting both the RC and EP functions.

PCIe Core

The PCIe Core implements the physical layer, data link layer and transaction layer of the PCIe protocol. The physical layer provides the PIPE interface to easily connect to any PCIe-compliant PHY device, and the HAL or optional AMBA 3/4 AXI provides connectivity to the client. The PCI Core manages the functions of the PCIe protocol including data deskewing, replay buffers, flow control, and CRC check and generation.

Configuration Registers

The Controller IP implements a complete set of PCI base configuration registers and PCI capability registers for PCI power management, MSI and MSI-X, PCIe, and Slot ID. In addition, the configuration registers have PCIe extended registers for advanced error reporting.

A local management bus (APB) is available to access configuration and internal registers within the controller.

Client Interface

The Client Interface is implemented to support AMBA 3/4 AXI or Cadence's HAL. The Client Interface consists of separate initiator and responder interfaces.

The Responder Interface is used for receiving transactions from the link and sending responses back. With the Initiator Interface, the client or DMA engine can initiate a packet transfer to the PCIe link. The datapath width on the Client Interface is configurable to 32-, 64-, 128-, or 256-bits depending upon the core generation and link width.

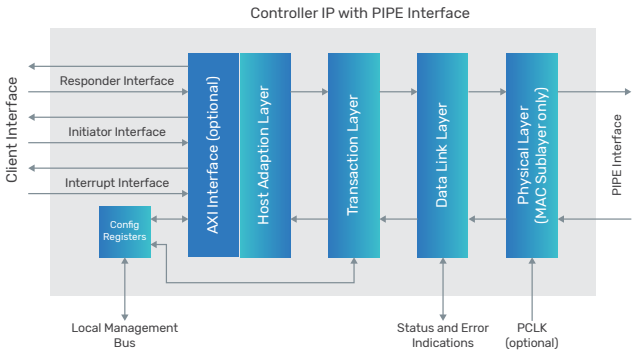

Figure 2: IP-level block diagram

PIPE Interface

The PIPE 4.2 specification is the industry-standard PHY Interface for the PCI Express Architecture v1.1, v2.1, and v3.1. In addition, the PIPE Interface has an optional PCLK input for running the PIPE Interface at a different clock rate than the core.

Related Products

- Controller IP for PCIe 1.1/2.1
- PHY IP for PCIe 3.1
- Integrated Solution IP for PCIe 3.1

Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench with integrated BFM and monitors

For more information, visit cadence.com/designip

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