DESIGN IP BROCHURE

10G/2.5G/1G Multi-Speed Ethernet Controller IP for Automotive Applications

Overview

Industrial, infrastructure, and consumer applications demand faster Ethernet speeds to solve ever-increasing bandwidth utilization. This trend also impacts automobiles with features like advanced driver assistance systems (ADAS) and in-vehicle infotainment (IVI) becoming mainstream. In addition, the push for autonomous driving requires multiple streams of data from cameras, sensors, and radars be transferred and processed in real time. This is leading to an exponential growth in in-vehicle data traffic. Automotive Ethernet is leading the way in resolving these issues by providing a high bandwidth, reliable, and time-sensitive communication link within an automobile. With a comprehensive and rich feature set, multiple integration options, and flexible configurations, Cadence® IP are leading the way in main stream Ethernet IP.

The Cadence 10G/2.5G/1G Multi-Speed Ethernet Controller IP for Automotive Applications is a highly customizable soft controller IP, which is compliant with the IEEE 802.3 standard. To support a range of Ethernet applications, the Controller IP for Automotive features integrated 1000BASE-X and USXGMII PCS modules, a high-performance DMA with advanced AXI offloading capabilities and descriptor caching, QoS, and IEEE 1588. The Time Sensitive Networking/ Audio-Video Bridging (TSN/AVB) functionality enables unified Ethernet communication of critical data without traffic congestion in shared networks. Furthermore, the Controller IP for Automotive supports a host of other features including IEEE 802.3az Energy-Efficient Ethernet (EEE), VLAN, TCP/ IP offload, and remote network monitoring (RMON).

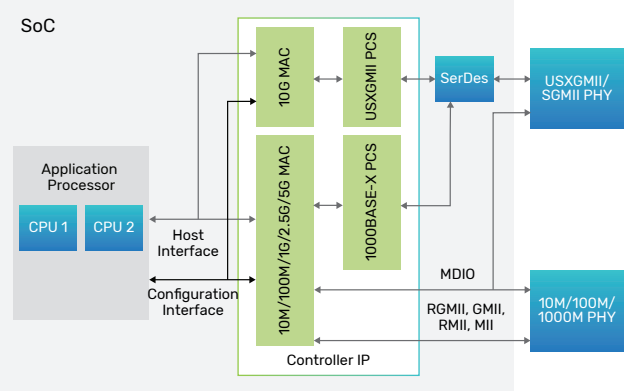

Figure 1: Example system-level block diagram

Benefits

- IEEE 802.3 compliant and ISO 26262 ASIL-B ready, simplifying path to SoC qualification
- Flexible configuration with enhanced functional safety features
- Silicon proven and widely licensed architecture

Key Features

- IEEE 802.3 compliant and ISO 26262 ASIL-B ready
- Enhanced active functional safety features
- Integrated 1000BASE-X PCS and USXGMII PCS
- Seamless DMA interfacing to Arm® AMBA® 3/4 AXI and AHB interconnects
- TSN/AVB protocol support including IEEE 802.1Qav, 802.1Qbv, 802.1AS, 802.1Qbu/802.3br, 802.1CB, 802.1Qci, and 802.1Qaz
- TCP/IP offloading capability and IEEE 1588 support
- MII, RMII, GMII, RGMII, USXGMII, and SGMII interfaces

The Controller IP for Automotive enables deterministic, real-time data transfer for virtually all types of applications in an automobile. It supports multiple functional safety features such as datapath parity protection for fault detection. A representative configuration of the Controller IP for Automotive has undergone Failure Modes, Effects, and Diagnostic Analysis (FMEDA). A functional safety manual is provided as one of the deliverables to help you perform your own FMEDA analysis.

In production with multiple devices in the field, the Controller IP for Automotive is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

Product Details

The Controller IP for Automotive is engineered to be quickly and easily integrated into any SoC. As shown below, the Controller IP for Automotive connects to a PHY through standard media independent interfaces such as MII, RMII, GMII, RGMII, XGMII, SGMII, or USXGMII. The host layer access to the Controller IP for Automotive is through industry-standard AXI or AHB interfaces when the DMA is being used or through an external FIFO interface. A separate APB interface allows the host applications to configure the Controller IP for Automotive.

10G/2.5G/1G Multi-Speed Ethernet MAC

Multi-speed MAC is compliant with IEEE 802.1Qbb priority-based flow control (PFC), and provides full-duplex flow control with recognition of incoming pause frames and hardware generation of transmitted pause frames. It supports a flexible and configurable screening algorithm based on VLAN, IP, TCP, UDP, and other indexed packet fields to map receive (RX) frames to priority queues. It provides address checking logic for up to 36 specific 48-bit source or destination addresses with byte masks, four type Ids, promiscuous mode, external address checking, hash matching of unicast and multicast destination addresses, and Wake-on-LAN. It performs padding and CRC generation for transmit (TX) frames.

TSN and AVB

Time-sensitive applications such as ADAS require timely and reliable data transfer with minimum latency, addressed by time sensitive networking (TSN) / audio video bridging (AVB) features supported by the Controller IP for Automotive. It supports time synchronization protocols such as IEEE 1588 and 802.1AS precision time protocol (PTP) via a Time Stamping Unit (TSU). For traffic management, features such as IEEE 802.1Qav (Credit Based Shaping), IEEE 802.1Qbv (Time Aware scheduling), IEEE 802.1Qbu/802.3br (frame pre-emption), IEEE 802.1CB frame elimination, and IEEE 802.1 Qci (Receive traffic policing), and algorithms such as Strict Priority, Deficit Weighted Round Robin (DWRR), and ETS (Enhanced transmission selection, or IEEE 802.1Qaz) are supported.

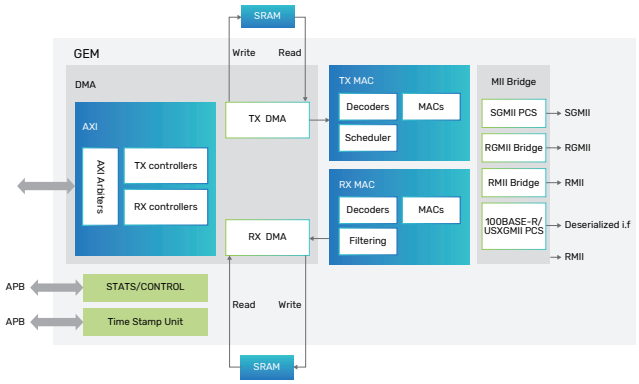

Figure 2: IP-level block diagram

Functional Safety Features and Documentation

The Controller IP for Automotive is ISO 26262 ASIL-B Ready, accelerating functional safety assessments at system level and helping the designers and integrators of this IP to reach the required ASIL levels. It is delivered with a safety manual intended to support safety system developers. This extra document describes additional system-level hardware or software safety mechanisms that should be implemented to achieve the desired system Safety Integrity Level. A representative configuration of the Controller IP core has undergone Failure Modes, Effects, and Diagnostic Analysis (FMEDA). The provided safety manual should be referenced, and the suggested external safety mechanisms should be, where possible, implemented in order to meet the required ASIL safety level.

DMA

The dynamic memory access (DMA) is an AXI or AHB initiator that improves performance and allows connections to system fabrics. It supports features such as local DMA descriptor buffering, support for multiple outstanding transactions spanning multiple frames on AXI channels, configurable data bus width up to 128 bits, configurable for 32- and 64-bit address bus width, support for either dual-port SRAM or single-port SRAM, extended Buffer Descriptor Modes for extra status capturing, programmable burst length up to 256 beats, automatic burst breaks at 4KB boundaries, options to help maximize burst efficiency, and support for full store and forward or low-latency partial store and forward.

Related Products

- Verification IP for Ethernet

Deliverables

- Documentation—Integration guide, user guide, quick start guide and release notes
- Functional Safety—FMEDA report, safety manual, and ISO 26262 ASIL readiness certificate
- Clean, readable, synthesizable Verilog RTL
- Synthesis scripts
- Sample verification testbench with integrated BFM, monitors, and confidence tests
- Reference drivers

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