

How Design IP Can Accelerate and Simplify Development of Enterprise-Level Communications and Storage Systems

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We're in an era of sizeable growth in data and compute demand, along with increasing global data traffic. As a result, enterprise-level data communications, networking, and storage systems are taking center stage in many application areas, from video and mobile to cloud computing. High performance and uptime, power efficiency, and small form factor are some of the key requirements for such systems, and these requirements impact their underlying electronic components and intellectual property (IP) building blocks. That's why it's essential for you to ensure that every level of your design meets these requirements and that each component operates as intended on its own and within the context of the entire communications infrastructure system. In this paper, we will examine how pre-verified, standards-based design IP can help in this regard, giving you the ability to deliver on your quality and time-to-market goals.

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Introduction

Driven largely by mobile and video applications and emerging cloud computing systems, our data-centric world is creating significant demand for servers, storage, and networking equipment, the core components of datacenters. The transition from on-premises datacenters to cloud infrastructures is already underway. Applications and data access on multiple platforms is the norm. Virtualization is one way to help increase utilization in datacenters, reducing energy waste and targeting underutilized servers.

Whether it's a traditional datacenter or an enterprise-level cloud infrastructure, all of these systems require high performance and 99.99% availability to meet the high uptime, data traffic, and compute requirements; power efficiency to save on energy costs; low cost to support massive scaling; and the smallest size possible to save on real estate and associated cooling costs (Figure 1). At the same time, the protocol standards required to support these applications have evolved. For designers addressing these challenges, it's a tall order, but one that can be met with the help of design IP.

Interface, analog, and memory IP can provide pre-verified building blocks that you can integrate into your design, saving time and effort in your design cycle. The IP can also help you meet your power and performance targets, solve integration and verification challenges, and adapt quickly to these continually evolving design standards. Industry estimates have noted that IP blocks may occupy as much as 80% of an SoC—including classical IP as well as IP subsystems that combine related blocks and system-level IP that traverses the chip and the board. Furthermore, buying off-the-shelf IP versus developing the blocks in house can provide assurance that the IP will comply with the latest (and ever-changing) interface protocols, as many IP providers consider such protocol expertise to be within their domain.



Figure 1: Datacenters increasingly require higher uptime and performance and power efficiency—requirements that can be met at the design phase via IP. Pre-verified design IP can also help accelerate time to market and meet quality goals.

Challenges of Designing for the Datacenter

Meeting the steep growth in data traffic and in compute demand is a primary consideration when designing components for datacenters. According to Cisco Systems, annual datacenter traffic is expected to reach 6.6 Zettabytes (billion terabytes) by the end of 2016. Much of this traffic stems from mobile applications. Through 2019, Cisco estimates that mobile video consumption will generate much of the mobile data traffic growth; by 2019, the mobile network will process 24.3 exabytes (million terabytes) of data per month, with 17.4 exabytes of this being video content¹. Another growing data-intensive application area is cloud computing. From fitness trackers to Big Data analytics to an array of financial and medical services, more devices and applications are collecting, analyzing, and deriving intelligence from growing amounts of data.

Accommodating this volume of traffic calls for fast memory access speeds in order to avoid any system bottlenecks. After all, it doesn't matter how fast your processor performs if memory access is slow. To meet today's datacenter needs, memory IP is expected to scale up to 3200Mbps and beyond. Similarly, data transmission speeds also need to be high to avoid bottlenecking the system. To this end, the standard now for SerDes is 10GTps, moving to 28G, with pressure mounting to increase beyond 56G. To capitalize on the benefits of speed and proximity that datacenters bring, many organizations are relying on high-speed interfaces such as PCI Express® (PCIe®). Here, controller and PHY IP compliant with PCIe can help.

Power is another key consideration, since datacenters not only have high energy consumption but also generate a lot of heat. U.S. datacenters consume from 1.5 to 3% of the country's energy production. Multiply the power consumption of all of the servers in a typical datacenter, and you can see that cooling the equipment becomes a considerably complex task. Research has indicated that active servers use less than 20% of datacenter energy, while a substantial amount of energy is used to cool the servers and to support power consumption in idle states².

Designing networking and other datacenter components is not getting any easier for other reasons as well. At smaller geometries, you gain the advantages of a better power/performance mix, but you also face increased parasitics, challenging layout due to double and even triple patterning, and expanded design rule checks (DRCs). With time-to-market pressures always looming, your schedules are greatly constrained. In some cases, you may not be able to wait until a standard has been finalized if you're aiming to capture a particular market opportunity.

Advantages of Designing with Pre-Verified IP

Pre-verified design and verification IP can help ease your design process, accelerate your time to market, and help you meet key considerations when designing SoCs for enterprise-level communications and storage systems:

- Compliance with industry standards
- Performance and power targets

- Customization requirements
- Reduced integration and verification effort
- Design risk mitigation
- High robustness for signal noise

Compliance with industry standards

IP really excels when it comes to supporting industry standards and helping you overcome any challenges or barriers related to knowledge gaps on a given standard. IP vendors gain a deep understanding of specifications, developing their IP according to the requirements of each standard. As a result, you don't have to worry about keeping up to date with specification changes and can be assured that your design will, in turn, meet the performance, power, bandwidth and other relevant specs. You can then focus more of your time on other design priorities that provide differentiation for your SoC, rather than poring through hundreds of pages of specification guidelines for each protocol that your design needs to support.

As an example, consider networking designs, where the Ethernet protocol is the standard for networked data transmission. The Ethernet protocol continues to evolve to meet increasingly demanding bandwidth requirements. Ethernet MAC, PCS, and PHY IP products can help you meet changing speed, power, and area requirements. Hard IP (IP delivered as GDSII) can help you handle extreme operating temperature ranges over an extended period of time, as well as manage the effects of electromigration/IR drop (EMIR) – important considerations in a networking or datacenter environment. Hard IP undergoes thorough testing under a variety of conditions, such as extreme operating temperatures, and is built to be durable beyond some single point in order to accommodate designers with different operating condition requirements. In fact, while standards generally address a common need, IP providers often go beyond the specs outlined in the standards for factors such as temperature range, signal strength, noise tolerance, and voltage differences between SoCs to provide increased robustness in real-world environments.

Power and performance targets

The performance and power specs discussed in the previous section are in the realm of the market's available IP offerings. For example, Cadence offers Denali™ DDR controller IP, Denali DDR4 PHY IP, and Denali LPDDR4 PHY IP that each operate at up to 3200Mbps. These IP products [recently achieved TSMC9000 Silicon Assessment](#) for TSMC's 16nm FinFET Plus process. Cadence also offers 16Gbps Multi-Protocol and Multi-Link PHY IP for PCI Express® (PCIe®) 4.0 that operates at speeds from 1.25Gbps to 16Gbps and meets the most stringent datacenter and networking requirements: 10-year lifetime, 110C for electromigration, and $V_{dd} +10/-5\%$.

PCIe 4.0, in particular, addresses the need for high performance and low latency to support east-west traffic, providing much needed capabilities including 16Gbps transfer speed (scalable to 256Gbps (x16)), multi-CPU data analytics, and broad deployment. Figure 2 compares old datacenter demands with new, where the emphasis is on east-west linear scalability. Cadence, in particular, has optimized its PCIe controller and PHY to support new L1 power-saving states.

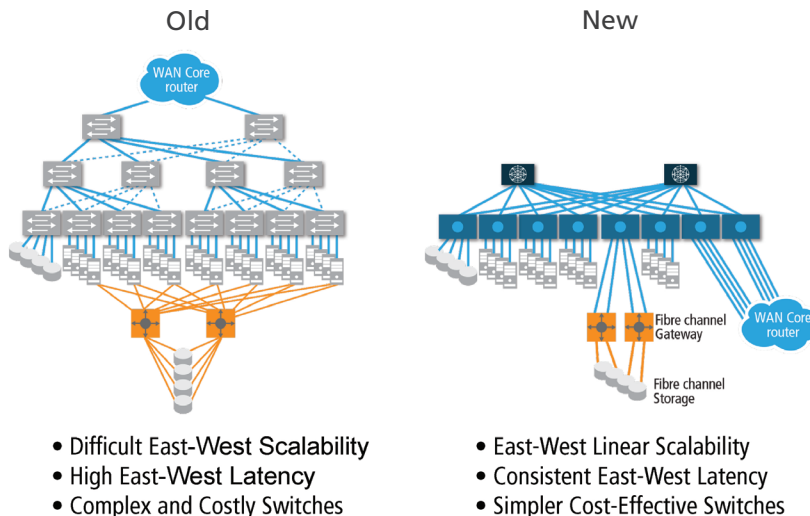


Figure 2: Requirements for meeting today's datacenter demands

IP for PCIe can help save significant power when servers are in idle state. PCI-SIG has updated the PCIe spec with engineering change notices (ECNs) that help improve system power consumption. With these advances, PCIe devices can support an increased dynamic range for power consumption based on activity and utilization, with better system energy proportionality.

Considering the cost and effort of chip design, you may want to future-proof your designs by adapting one chip for multiple target systems. For this approach, you would need to be able to adapt quickly to different standards. IP with support for multiple protocols can give you the flexibility to modify your design to accommodate standards across a range of application areas. Furthermore, the ability to multiplex a single port for different protocols also allows you to use one chip for different applications. For example, you might adapt your chip to an application that calls for PCIe x16 lane support, and utilize the same chip for another application requiring PCIe x8 lane support and eight lanes for another chip-to-chip protocol.

Customization requirements

IP designed with a configurable architecture, along with software and prototyping solutions, can help you meet your customization requirements. Select an IP vendor who can provide specific features and performance levels targeted to your unique SoC design. This way, you can integrate the IP into your design, rather than having to build your design around the IP.

Reduced integration and verification effort

Integrating IP into your design can be a challenge, but much less so if you are using IP and IP subsystems designed from the ground up with an integration focus. Controller, PHY, and firmware solutions that are fully integrated at the interface and subsystem levels can reduce your design risks as well as your integration effort. By the same token, being able to use fully verified IP from a vendor saves you the step of doing the groundwork to ensure that the IP will work with your design.

Design risk mitigation

The breadth of verification in the IP is another important consideration. Not all IP vendors are the same in this regard. IP vendors who are focused on early development of IP, collaborating closely with end customers as they build out their SoCs, have an advantage. These vendors are privy to insights about design challenges as their customers encounter them, so they can adjust and update their IP accordingly. They build into their design process all of their lessons learned and continue to enhance future iterations of IP. Also, the more customers an IP vendor works with, the more access the vendor has to platforms on which to test their IP, ultimately helping you mitigate your design risks. Not every vendor has the ability to continually gather data about interoperability and also ensure verification of their IP across multiple platforms.

Integration-Focused IP and IP Subsystems

In Cadence's broad portfolio of fully verified design IP, you can find cores that are ideally suited to SoCs for communications infrastructure applications such as servers, storage systems, and networking equipment. Cadence focuses on early development of IP, building its products from the ground up while working closely with multiple customers who integrate the IP into their designs as they are building them. As customers test and verify their designs while progressing toward tapeout, our IP developers test the IP along with way, providing the benefits of distributed verification. With access to so much silicon data early on, our IP developers can quickly understand advanced processes and their limitations and challenges and incorporate what they're learning into each generation of IP.

As an early driver of standards compliance, Cadence often plays a role in standards definition. Our technical experts are part of the working groups for various standards organizations. As another example, we were the first IP vendor to bring PCI Express Gen3 controllers to market and today, our controller and PHY IP for PCI Express supports the latest specification (4.0). Because we certify our IP in silicon, you can be assured that your design can pass the same certification.

Cadence develops integration-focused IP and IP subsystems that have demonstrated the ability to reduce risk and to accelerate SoC development. Strong relationships with foundries means early access to their processes and, as a result, the ability to proceed with early development, validation, and certification.

For enterprise-level data communications and storage systems, Cadence offers a variety of relevant design IP to meet performance, power efficiency, and other requirements (Figure 3), including:

- 16Gbps SerDes PHY IP for PCIe 4.0 for inter-device communication between chips, between boards, and between systems; high-performance data communication; high-performance storage access; and high-performance datacenter communication
- DDR4/3 controller and PHY IP providing low-latency data access and enhanced memory utilization, such as for Big Data local computation support. Features such as error correction code (ECC), parity, and memory built-in self-test (MBIST) enhance data reliability by minimizing undetectable data corruption in high-density computing environments.
- SATA 3.1 PHY IP for high-performance data storage from server to storage device. Its high-speed, low-power architecture features a unique automated calibration design that protects against process, voltage, and temperature variation.
- NAND Flash IP, providing fast Boot ROM code storage
- Ethernet MAC IP for 25G/100G and 10G/40G, supporting key Ethernet interoperability for system connections to the existing infrastructure. The MAC IP supports the latest IEEE specifications, including Energy-Efficient Ethernet, time stamping, and audio-video bridging, and provides a rich set of offload features with a low-latency DMA engine.

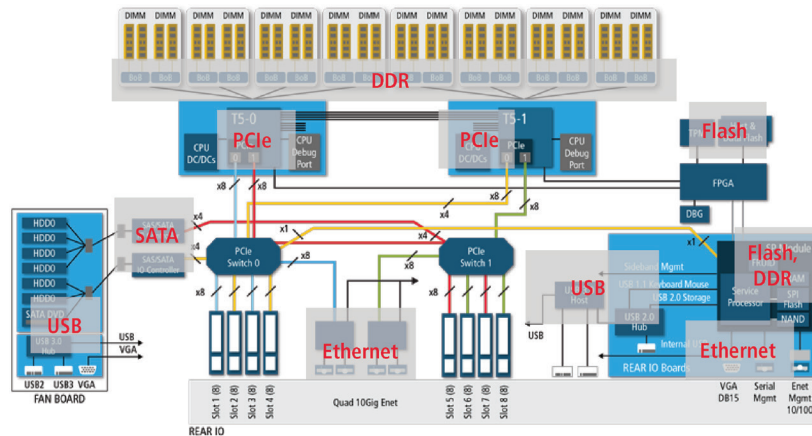


Figure 3: Cadence enterprise IP offering

In addition, the portfolio includes IP subsystems that support multiple protocols. For example, multi-protocol, multi-link PHY IP supports PCI Express 2.0, USB 3.0 SuperSpeed, SATA III, DisplayPort 1.2a, MIPI® M-PHY Gear 3, and SGMII. With this IP, you can meet the requirements of a variety of continually evolving interface standards, manage your design costs, and future-proof your designs. Cadence’s IP portfolio also includes memory interface IP supporting a variety of other standards, device interface IP, as well as analog IP such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), analog front-ends (AFEs), and phase-locked loops (PLLs).

Cadence also provides a wide-ranging portfolio of proven verification IP (VIP) for verifying SoC designs quickly and thoroughly. The VIP supports more than 40 communication protocols and 60 memory interfaces, saving substantial time by modeling interfaces as components that can be plugged into an SoC testbench and simulated along with your chip. As with design IP, the VIP incorporates the deep knowledge of protocol and interface experts, so you won’t have to worry about staying up to speed on changing specifications.

Optimizing Electronic System Design

Each of the electronic components within an end product can no longer be designed in isolation if you want the assurance of an optimized design, where all of the pieces work well together and you’re able to streamline your design cycle. Cadence’s design IP offerings are part of a broad portfolio of hardware, software content, and services that help streamline the design and verification of your entire communications/storage system, from chip to package to board and the final product. With these integrated design solutions, you can efficiently ensure that each component in your system will function as intended on its own and in conjunction with all of the other

components. You can also account for environmental and other operating conditions. In short, with Cadence's system design technologies, you can turn your ideas into differentiated end products, working productively, reducing risks, and focusing on high quality.

Summary

Increased reliance on servers, storage systems, networking equipment, and other communications infrastructure applications mean that high performance and uptime, low power consumption, and reduced area are more critical than ever for the underlying SoCs. Proven, pre-verified design, analog, and memory IP can go a long way in mitigating design risks, lowering costs, and helping you meet your power, performance, and area (PPA) and time-to-market targets.

[Click to View Design IP Portfolio](#)

Footnotes

¹ Source: Cisco Systems http://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/white_paper_c11-520862.html

² Source: Arif Khan and Osman Javed, "Software and System Solutions Drive Datacenter Efficiency," Electronic Design; <http://electronicdesign.com/power/software-and-system-solutions-drive-datacenter-energy-efficiency>



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