

Dual-Role Device Controller IP for USB 3.0

Overview

Today's Universal Serial Bus (USB) 3.0 IP meets the demands of PC and mobile products for energy efficiency and higher performance. Cadence understands these technical challenges and offers the Dual-Role Device Controller IP for USB 3.0.

Certified for compliance with USB 3.0 Specification v1.0, and xHCI Specification v1.0, the Cadence® Dual-Role Device Controller IP for USB 3.0 operates in SuperSpeed (5Gbps), High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) modes. The USB 3.0 PHY interface complies with the PHY interface for the PCIe® and USB 3.0 architectures (PIPE) Specification v3.0, while the USB 2.0 PHY interface complies with UTMI+ Specification, Revision 1.0.

Combined with Cadence IP for USB Type-C designs, the Cadence Dual-Role Device Controller IP for USB 3.0 provides a complete solution for USB applications that will make use of the new, flexible USB Type-C connector.

The Controller IP is silicon-proven, and has been extensively validated with multiple hardware platforms. The Cadence Dual-Role Device Controller IP for USB 3.0 is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

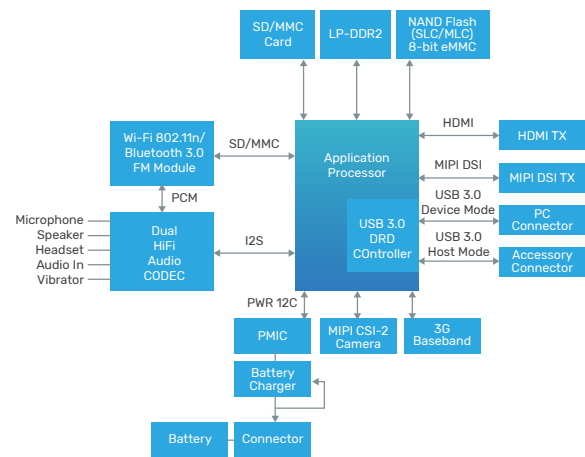


Figure 1: Example system-level block diagram

Benefits

- ▶ Complete hardware and software solution—less time spent on application development
- ▶ High level of configurability—better fit for application needs
- ▶ Industry-standard interfaces—simple system integration

Key Features

- ▶ Compliant with the following specifications: USB 3.0, USB 2.0, and xHCI 1.0
- ▶ Arm® AMBA® 3 AXI support with outstanding transactions and out of order support
- ▶ AMBA APB configuration interface
- ▶ SuperSpeed (5Gbps), High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) operation
- ▶ USB 3.0 PHY support with 32-bit PIPE, and USB 2.0 PHY with 8-bit UTMI+ interface
- ▶ Full Link Power Management (U0, U1, U2, and U3) with LFPS and power/clock gating support
- ▶ Compatible with the Cadence 16Gbps Multi-Link Multi-Protocol SerDes IP
- ▶ xHCI-compatible DMA for Host mode and scatter-gather DMA for Device mode

Product Details

The Cadence Dual-Role Device Controller IP for USB 3.0 implements the USB standard to manage connections for all types of USB applications, including but not limited to mass storage, video, audio, communication, and vendor-specific applications.

AXI Initiator Interface

The AXI Initiator Interface provides access to system memory and internal interfaces for xHCI Host Engine. Compliant with the AXI Protocol specified by the AMBA AXI and ACE Protocol Specification, this interface is implemented in a way that enables support for up to 16 outstanding transactions.

Design IP for USB xHCI Host Controller

The xHCI Host Controller is comprised of three main modules: xHost, xRootHub, and xPort. The xHost contains the majority of the functions that are called out in the xHCI specification. It performs the data movement from host memory to the target device.

Peripheral Device Controller

The Peripheral Device Controller is comprised of four main modules: SuperSpeed controller, High-Speed and Full-Speed controller, DMA Engine, and Endpoint Logic.

The SuperSpeed Controller implements the USB 3.0 protocol for peripheral devices. Functions are distributed among link layer and protocol layer modules, which allows the Peripheral Device Controller to reach maximum transfer speeds of almost 98% of the theoretical maximum value.

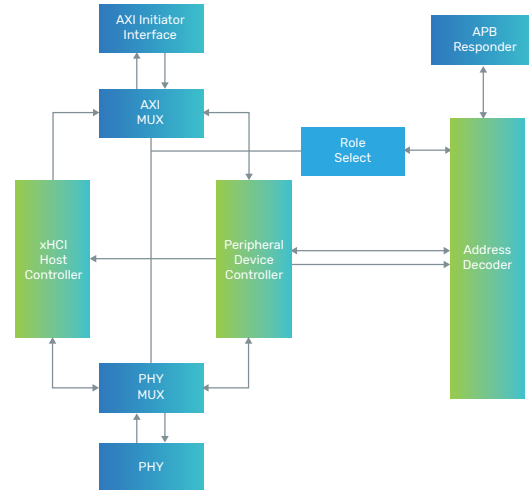


Figure 2: IP-level block diagram

Address Decoder

The Address Decoder module assigns APB requests to an appropriate controller: xHCI Host, Peripheral Device, or Role Select. By writing to the Role Select registers, the application can define the active mode (host or peripheral).

Availability

The Cadence USB 3.0 Dual-Role Device Controller is available with various configurations.

Related Products

- ▶ VIP IP for USB 3.0
- ▶ PHY IP for USB 3.0/2.0
- ▶ 16Gbps Multi-Link Multi-Protocol SerDes IP

Deliverables

- ▶ Synthesizable RTL
- ▶ Testbench
- ▶ Synthesis and simulation support files
- ▶ Documentation

For more information, visit [cadence.com/designip](https://www.cadence.com/designip)

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