DESIGN IP BROCHURE

Design IP for USB 2.0 OTG Controller

Overview

Certified for compliance with Universal Serial Bus Specification, Revision 2.0 and On-The-Go and Embedded Host Supplement to the USB Specification Revision 2.0, the Cadence® Design IP for USB 2.0 On-The-Go (OTG) Controller operates dynamically as either a Device or embedded Host controller. The PHY interface complies with UTMI+ Specification, Revision 1.0.

The Controller IP, made for one of the most ubiquitous interfaces in electronics commonly used in consumer products, phones, and computers, is architected to quickly and easily integrate into any system on chip (SoC), and to connect seamlessly to a Cadence or third-party, UTMI-compliant PHY. Both configuration and data interfaces of the controller are compatible with industry-standard Arm® AMBA® AXI interfaces.

The Controller IP is delivered with a low-level driver to ease integration into the target application. Controller IP supports all available USB 2.0 classes.

The Controller IP is silicon-proven, and has been extensively validated with multiple hardware platforms.

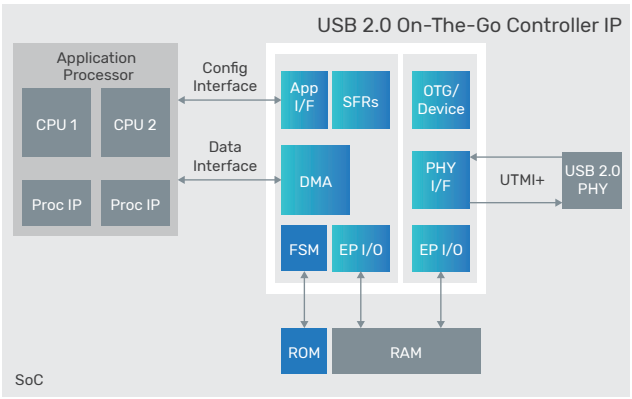

Figure 1: Example system-level block diagram

Benefits

- Complete hardware and software solution - less time spent on application development
- High level of configurability - better fit for application needs
- Industry-standard interfaces - simple system integration

Key Features

- Compliant to USB 2.0 specification and USB 2.0 OTG and EH supplement
- Supports High-Speed (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps)
- Supports Host Negotiation, Session Request, and Attach Detection Protocols
- Scatter-gather DMA engine with AXI interface
- 8-bit UTMI+ interface
- TSMC Soft - IP9000 compliant

Product Details

The Controller IP handles data transfer autonomously, and bridges the USB interface to a simple read/write parallel interface.

The Controller IP supports a DMA interface to optimize controller operation for your specific application.

OTG Controller

The Controller IP implements On-The-Go and Embedded Host functionality as defined in the USB 2.0 OTG supplement. Special Function Registers provide control of the Host Negotiation and Session Request protocols.

Embedded Host Controller

The Embedded Host Controller implements the USB 2.0 protocol for host devices, which includes initiation of data transactions on the USB, suspend and resume signaling, and USB reset signaling, and host-interrupt generation. In addition, the Embedded Host Controller automatically generates SOF tokens for frame and microframe timing, and device keep-awake functions.

Endpoint Logic

The Endpoint Logic generates control signals for two synchronous, dual-port RAM components, one port for OUT endpoints and one port for IN endpoints. RAM size is fully configurable for the number, size, and buffering requirements of endpoints.

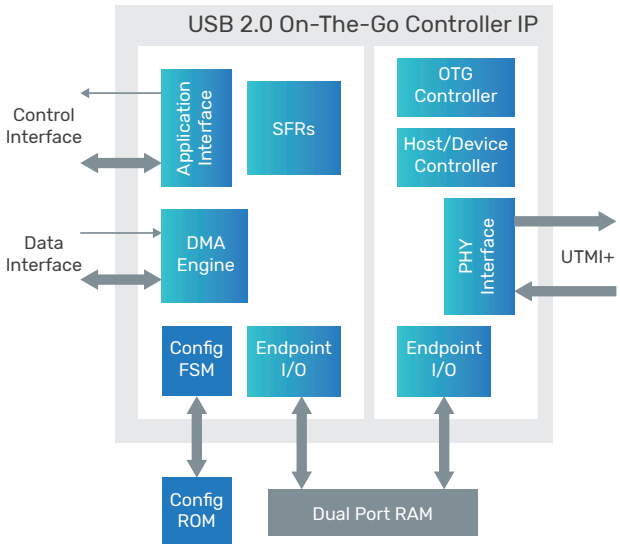

Figure 2: IP-level block diagram

PHY Interface

The Controller IP connects to the PHY through an 8-bit UTMI+ interface.

Application Interface

The Controller IP supports the AXI interface for configuration and data access. Access to the DMA engine is realized through a responder FIFO interface. The DMA engine features an AMBA AXI interface.

Related Products

- Verification IP for USB Protocols
- PHY IP for USB 2.0

Deliverables

- Synthesizable RTL
- Testbench
- Synthesis and simulation support files
- Documentation

For more information, visit cadence.com/designip

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