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Design IP for USB 2.0 Device Controller

Overview

Certified for compliance with Universal Serial Bus Specification, Revision 2.0, the Cadence® Design IP for USB 2.0 Controller operates in High-Speed (480Mbps) and Full-Speed (12Mbps) modes. The PHY interface complies with USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, version 1.05.

The Controller IP is architected to quickly and easily integrate into any system on chip (SoC), and to connect seamlessly to a Cadence or third-party UTMI-compliant PHY. Both configuration and data interfaces of the controller are compatible with industry-standard Arm® AMBA® AXI specifications.

The Controller IP is delivered with a low-level driver to ease integration into the target application. The Controller IP supports all available USB 2.0 classes.

The Controller IP is silicon-proven, and has been extensively validated with multiple hardware platforms.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and systems and peripherals IP.
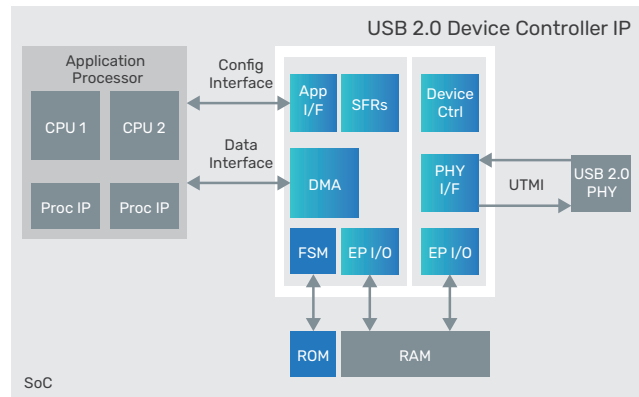

Figure 1: Example system-level block diagram

Benefits

▸ **Complete hardware and software solution—Less time spent on application development**

▸ **High level of configurability—Better fit for application needs**

▸ **Industry-standard interfaces—Simple system integration**

Key Features

▸ Supports High-Speed (480Mbps) and Full-Speed (12Mbps) data transfer rates

▸ Scatter-gather DMA with AMBA AXI interface

▸ Up to 8 IN and 8 OUT configurable endpoints

▸ Certified for compliance with USB 2.0 specification

▸ AXI configuration interface

▸ Supports Link Power Management (L0 through L3)

▸ Supports Attach Detection Protocol

▸ Support for Remote Wake-Up

Product Details

The Controller IP handles data transfer autonomously and bridges the USB interface to a simple read/write parallel interface.

The controller operation can be customized for specific applications.

Device Controller

The Device Controller implements the USB 2.0 protocol for peripheral devices. Data transactions, suspend and resume behavior, and interrupt generation are all handled by the Device Controller. Special Function Registers are provided for programming the behavior of the Cadence USB 2.0 Device Controller IP.

DMA Engine

The DMA Engine transfers data between endpoint buffers and external memory. The DMA Engine can be configured for least significant byte (LSB) and most significant byte (MSB) transfers. The advanced DMA Engine supports scatter-gather operation.

Endpoint Logic

The Endpoint Logic generates control signals for two synchronous, dual-port RAM components, one port for OUT endpoints and one port for IN endpoints. RAM size is fully configurable for the number, size, and buffering requirements of endpoints.
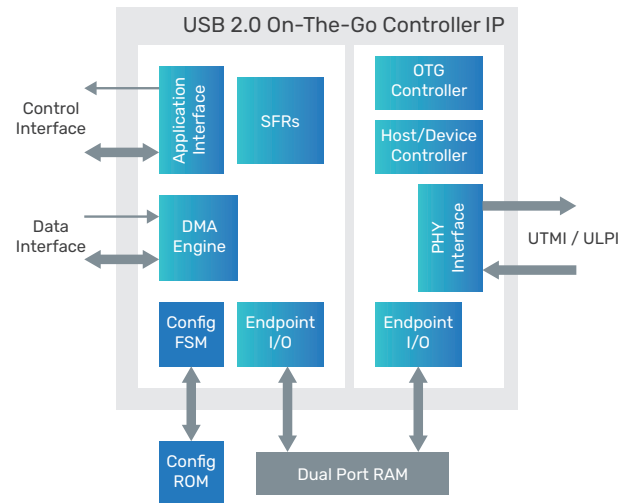

Figure 2: IP-level block diagram

PHY Interface

The Controller IP connects to the PHY through an 8-bit UTMI interface.

Application Interface

The Controller IP supports AXI interface for configuration and data access.

Availability

The Controller IP is available with support for the following protocol:

Protocol	Speed
USB 2.0	480Mbps

Related Products

‣ PHY IP for USB 2.0

‣ Cadence Verification IP for USB Protocols

Deliverables

‣ Synthesizable RTL

‣ Testbench

‣ Synthesis and simulation support files

‣ Documentation

For more information, visit cadence.com/designip

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