Design IP DATA**SHEET**

cadence

Denali Controller IP for GDDR6

GDDR6 devices to 16Gbps, 18Gbps, 20Gbps, and beyond

Overview

Artificial intelligence (AI), high-performance computing (HPC), cryptocurrency mining, and graphics applications generate and consume large volumes of data and video and require very high memory bandwidth. The Cadence® Denali® DDR IP is a family of high-speed on-chip interfaces to external memories, with the bandwidth necessary to support these applications.

The latest, the Cadence Denali Controller IP for GDDR6, provides low latency and very high bandwidth, while supporting extensive value-added features including, but not limited to reliability features.

Developed by experienced teams with industry-leading domain expertise and based upon Cadence's widely proven DDR controller IP, the Controller IP for GDDR6 can provide customers with ease of integration and fast time-to-market.

The Controller IP is engineered to quickly and easily integrate into any system-on-chip (SoC), and is verified with the Cadence Denali PHY IP for GDDR6 as part of a complete memory subsystem solution that also includes Cadence Verification IP (VIP). The Controller IP is designed to connect seamlessly and work with Cadence or third-party DFI-compliant PHY IP. Developed for and available in alignment with the PHY IP on advanced semiconductor process nodes, the Controller IP is designed to be robust under various traffic loads and to have interoperability with various supplier memory chips. The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Denali memory interface, analog, and systems and peripherals IP.

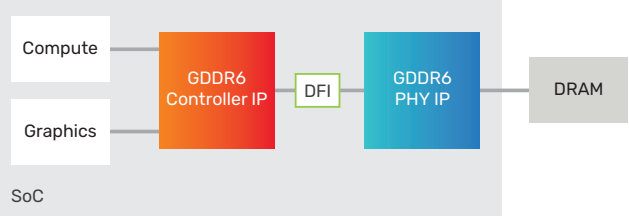

Figure 1: Example system-level block diagram

Benefits

- Configurable to meet specific data traffic profiles
- Optimized low latency for data-intensive applications
- Future-proof system design for emerging GDDR6 standards

Key Features

- Compatible with GDDR6 devices compliant to JESD250B
- Supports in-line ECC
- Single and multi-port host interface options
- Flexible paging policy including auto-precharge-per-command
- Supports advanced RAS features including SEC/DED ECC, error scrubbing, parity, etc.
- Priority-per command on Arm® AMBA® 3 AXI and low-latency Denali interface
- QoS features allow command prioritization on Arm AMBA 4 AXI interfaces

Product Details

The Controller IP is designed to provide the flexibility needed to enable application-specific configurations ranging from high-performance networking and mobile to consumer. The host-side port interface can be configured to support multiple ports, each of varying width and with different AMBA protocol and clocking options. The command queue intelligently schedules traffic from the port arbiter to maximize data throughput efficiency. The Controller IP includes various feature options such as low-power modes required by mobile applications and several reliability features required by enterprise applications.

DDR DRAM Controller

The Controller IP was engineered to be highly configurable, allowing the selection of application-specific features, which in turn yield an area-optimized solution per application. The controller is also developed to provide maximum throughput across many different traffic profiles.

The Controller IP uses multi-stage reordering algorithms architected for use with traffic profiles from many different applications. Performance-tuning parameters allow performance optimization based on individual system and memory requirements.

The Controller IP supports one 2x16-bit GDDR6 device (coplanar) or two 2x16-bit devices in clamshell configuration. Multiple channels may be instantiated for capacity or bandwidth expansion.

The Controller IP also delivers a wide array of capabilities to address emerging DDR DRAM subsystem reliability, availability, and serviceability (RAS) requirements. Some of these capabilities include embedded support for ECC and other vital error detection and error prevention capabilities such as parity protection and DRAM data scrubbing. All the Controller IP configurations support power-down and self-refresh.

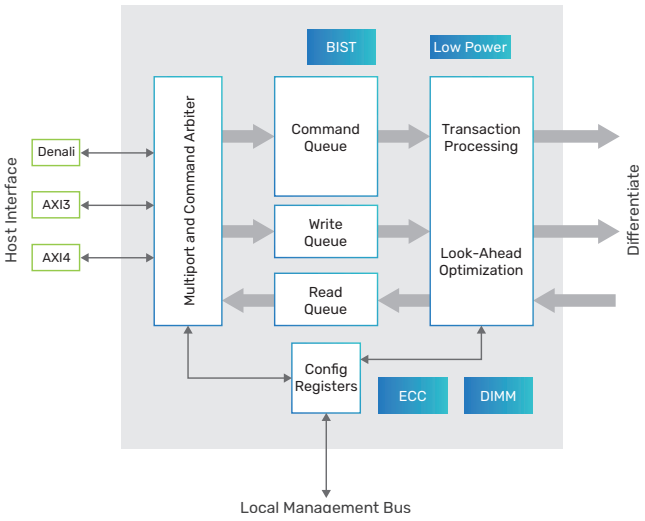

Figure 2: IP-level block diagram

Host Interface

Natively supports any mix of Denali and AXI interfaces. Priority-per-command on AMBA 3 AXI interfaces and QoS on AMBA 4 AXI interfaces improves latency and controller QoS, especially for transactions delivered through an interconnect fabric. Flexible synchronization allows low-latency synchronous port connection, reduced-latency pseudo-synchronous ratio port connection, or highly flexible asynchronous port connection.

DFI Interface

The DFI 5.0-like PHY interface connects to Cadence or third-party PHYs. An 8:1 frequency ratio is used between the DRAM and the memory controller to assist timing closure.

Availability

The Controller IP is available with various configurations and supports the following protocol:

Protocol	Speed
GDDR6	Up to 20+Gbps

Related Products

- Verification IP for GDDR6
- Denali PHY IP for GDDR6

Deliverables

- Clean, readable, synthesizeable Verilog RTL
- Synthesis and STA scripts
- Documentation—integration and user guide, release notes
- Sample verification testbench with integrated BFM and monitors

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