cādence®

64GTps PHY IP for PCIe 6.0 for TSMC 5nm FinFET

Overview

The Cadence® PHY IP for PCI Express® (PCIe®) 6.0 for TSMC 5nm delivers a data rate of up to 64GTps in PAM4 mode and 32/16/8/5/2.5GTps in NRZ mode. Designed specifically for infrastructure and data center applications, the PHY features advanced long-reach equalization and clock-data-recovery capabilities to achieve exceptional performance and reliability. Optimized for low latency and low active/standby power consumption, the PHY is ideal for deployment in time-critical and power-sensitive applications in high-performance computing (HPC), artificial intelligence / machine learning (AI/ML), data communications, networking, and storage systems.

Cadence PHY IP is highly versatile and scalable. The PHY can be configured to support X1, X2, X4, X8, and X16 lane widths. The embedded bifurcation capability allows multiple PCIe links of various link widths to co-exist and operate independently in the same macro.

A comprehensive set of diagnostic and test features is incorporated to enable faster silicon bring-up and simplify troubleshooting. EyeSurf graphic interface provides convenient access to real-time eye scope and bit-error-rate (BER) computations to monitor the link performance during live traffic.

The PHY IP is fully compliant to PCIe 6.0, 5.0, 4.0, 3.1, 2.1, and 1.1 as well as Compute Express Link (CXL) 2.0, 1.1 specifications. It is engineered to quickly and easily integrate into any system-on-chip (SoC) design. Moreover, the PHY IP connects seamlessly to Cadence's PCIe and CXL controllers. The integrated total solution from Cadence ensures faster time to market by reducing the development cycle and minimizing risks.
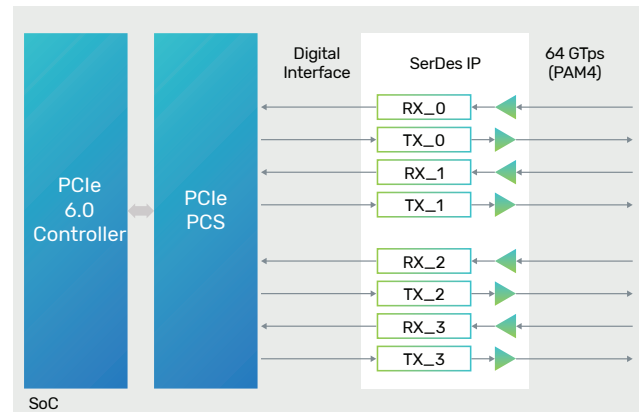

Figure 1: 4-lane example system-level block diagram

Benefits

▸ Performance - Novel DSP-based architecture delivers superior performance and reliability

▸ Flexibility - Maximum configurability and scalability

▸ Maturity - Built from a strong legacy of Cadence designs for PCIe, billions of Cadence PCIe lanes in production

▸ Ease of use - Best engineering support to ensure ease of integration, quick bring-up, and faster time to market

Key Features

▸ DSP-based Long Reach (LR) equalization and clock data recovery (CDR) provide superior performance and reliability

▸ 8-bit DAC-based transmitter provides ultimate finite impulse response (FIR) equalization flexibility and superior signal integrity

▸ Low active and standby power consumption, supports L1 sub-states standby power management

▸ On-chip EyeSurf oscilloscope interface offers real-time traffic analytics

▸ Extensive set of isolation, test modes, and loopbacks including APB and JTAG

▸ Selectable serial pin polarity reversal for both transmit (TX) and receive (RX) paths

▸ Supports lane aggregation and bifurcation

▸ Supports 20-bit and 32-bit PIPE interfaces

Product Details

The Cadence PHY IP for PCIe 6.0 is designed to address the most demanding enterprise applications. The novel DSP-based receiver and DAC-based transmitter deliver unmatched performance, reliability, and robustness.

The PHY IP is composed of a hard macro providing Physical Media Attachment (PMA) layer functions and a soft core providing Physical Coding Sublayer (PCS) functions. The PHY IP supports up to 64GTps (PAM4) / 32GTps (NRZ) operation over LR channels with up to 40 dB of insertion loss. For power-sensitive applications, the PHY offers best-in-class active power efficiency and supports advanced standby power management features (i.e., PCIe L1 sub-states). For added robustness, the PHY is designed to operate over an extended temperature range from -40°C to 125°C.

The PCS complies with the latest PCIe PIPE specification and provides support for the dynamic equalization features for PCIe and CXL.
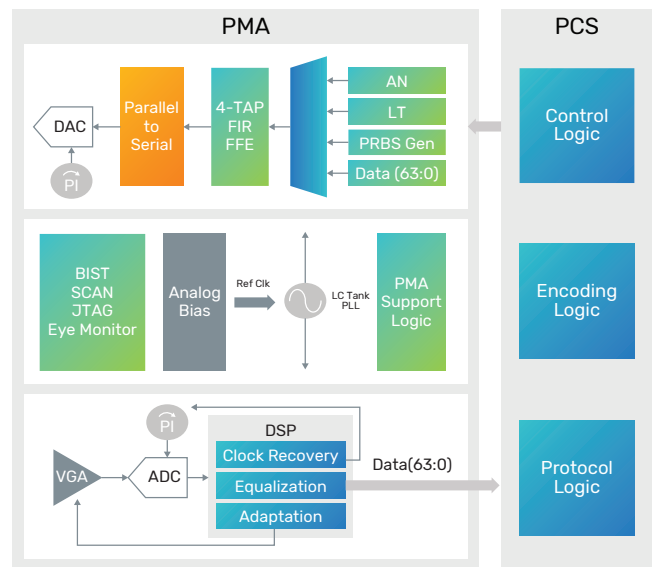

Figure 2: IP-level block diagram

PHY Architecture

The PHY IP for PCIe 6.0 is designed with a multi-link lane - based architecture. A Common module provides low-jitter, high-frequency clocks to the lane modules. Multiple lane modules can be instantiated and tiled to aggregate data throughput (x1 to x16). The modular approach provides greater control over floorplanning, placement, packaging, and I/O integration while maintaining the reliability and ease of integration associated with GDSII macros.

Availability

The PHY IP is available with various configurations and supports the following protocols:

Protocol	Data Rate (GTps/Lane)	Process Node
PCIe 6.0/5.0/4.0/3.1/2.1/1.1	Up to 64	5nm FinFET
CXL	Up to 64	5nm FinFET

Related Products

▸ Controller IP for CXL

▸ Controller IP for PCIe 6.0, 5.0, 4.0, 3.1, 2.1, 1.1

Deliverables

▸ Integration Views: Verilog behavioral model, GDSII, CDL, and power models

▸ Synthesizable RTL

▸ DFT-Verilog netlists with SS/FF, CTL, and BSDL

▸ Reference Verilog testbenches used for generating SoC-level VCD ATE test patterns for PHY

▸ IBIS-AMI kit

▸ Documentation: XML, integration and user guide, release notes

▸ Test boards available on demand

For more information, visit cadence.com/designip