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Master Controller IP for MIPI I3C

Overview

Rapidly increasing numbers of sensors creates new design challenges for mobile, automotive, and Internet of Things (IoT) devices. These design challenges include significantly higher signal count and increased bandwidth requirements. To address these challenges the MIPI® Alliance has defined the I3C^SM interface for connecting all the sensors in a system.

The Cadence® IP Family for MIPI Protocols delivers area-optimized interface IP with the low power and high performance required for today's leading-edge devices. One member of this family is the Cadence Master Controller IP for MIPI I3C^SM.

Compliant with the latest MIPI I3C specification and legacy compatible with I2C^SM, the Controller IP is engineered to quickly and easily integrate into any mobile embedded system on chip (SoC) device and expand sensor communication capabilities with better power efficiency.

Developed by experienced teams with industry-leading domain expertise, verified by silicon-proven and mature I2C IP and validated on a FPGA platform to reduce risk for designers, the IP will connect seamlessly to the Controller IP.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, Memory, Analog, System and Peripheral IP.
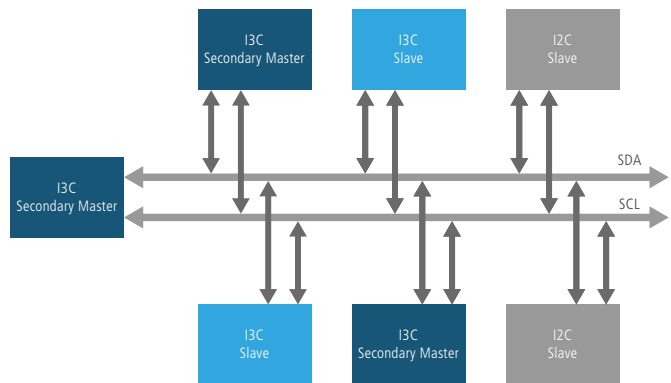

Figure 1: Example System-Level Block Diagram

Benefits

- Superior performance to power ratio compared to established sensor interfaces - I2C, SPI

- Complete solution—complementary master/slave IP

- Fully verified on FPGA

Key Features

- Support for multiple transmission modes: Single Data Rate (SDR) and High Data Rate (HDR)

- Compliant with the latest I3C specification

- Support for I3C common command codes

- Dynamic address assignment (DAA) support

- Support for in-band interrupts, hot-join, peer-to-peer request, mastership request

- I2C legacy device support

- APB interface support for register access

- Command queue support

Product Details

The Controller IP is compliant with the MIPI Alliance I3C sensor specification for embedded systems applications enabling the incorporation of more sensors in a device. This is a soft IP ideally suited for implementation in ASIC SoC designs with increasing numbers and types of sensors. It provides reduced energy consumption and higher performance over legacy designs.

Architecture

The Controller IP is split into hardware and software functions. The I3C manager handles packet forming and message handling in hardware. It includes an interconnect protocol and support for 32-bit APB slave mode to access the registers interface and external DMA. There is an optional FIFO to reduce load on the host servicing the I3C interface. It functions primarily as a master controller, with optional secondary master support.

The IP supports I3C standard-compliant protocols including legacy I2C mode, backward compatible to Fast Mode (FM—up to 400kHz) and Fast Mode Plus (FM+—up to1 MHz), single data rate I3C mode (up to 12.5 MHz), and optional High Data Rate (HDR-DDR).

The IP features include I3C common command codes, dynamic address assignment, in-band interrupts, hot-join request, and mastership takeover request support.

Clock Domains

The default system configuration will define fully asynchronous clock structure, no correlation between pclk and sys_clk. Pclk and
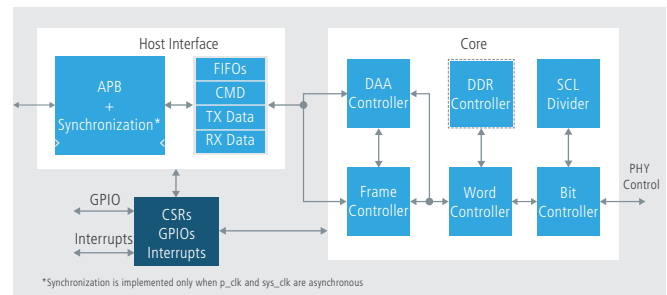

Figure 2: IP-Level Block Diagram

sys_clk are asynchronous to each other (in phase and frequency). Proper synchronization between pclk and sys_clk allows any combination of frequencies between 50 and 200MHz.

Host Command Interface

The host command interface provides command interface which can be queued. Commands are sent through the APB interface, with optional payload (write data or read data). Two separate RX/TX data FIFOs enable the controller to have mixed write/read command in the command queue FIFO. Immediate command provides a mechanism to send higher priority commands (CCC commands only).

Configurations Options

- FIFO (RX and TX FIFO depth)
- Secondary master support
- HDR-DDR mode enable/disable
- Command queue depth
- I3C devices that can reside on the I3C Bus with maximum number

Related Products

- Cadence Simulation VIP for MIPI I3C
- Cadence IP for MIPI I3C Slave Controller
- Cadence Inter Integrated Circuit (I2C) Controller IP

Deliverables

- Documentation—Integration guide, user guide, and release notes
- Clean, readable, synthesize-able Verilog RTL
- Synthesis scripts
- Sample verification testbench with integrated BFM, monitors, and sanity tests

For more information, visit ip.cadence.com