

BEAN IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The Cadence Backplane Ethernet Auto-Negotiation (BEAN) IP provides the logic required to integrate BEAN features into an Ethernet interface.

The Cadence BEAN IP is compliant with Clause 73 of IEEE Standard 802.3ap.

The Cadence BEAN IP is architected to quickly and easily integrate into any system-on-chip (SoC), and to connect seamlessly to a Cadence or third-party 3.125GHz SerDes (10/40G operation) with a 10-bit or 20-bit interface, or to a 10.3125GHz SerDes (40/100G operation) with a 16-bit or 32-bit interface. Other SerDes interfaces are supported through additional transmit and receive gearboxes. A separate 32-bit interface allows the host application to configure the Cadence BEAN IP.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

Product Details

The Cadence BEAN IP sends and receives Device Management Entity (DME) frames to advertise the node's capabilities, and gather the link partner's capabilities. The host application supplies the node capabilities, and reads the link partner's capabilities.

SerDes Interface

The Cadence BEAN IP can be configured to connect to a 3.125GHz SerDes with a 10- or 20-bit interface, or to a 10.3125GHz SerDes with a 16- or 32-bit interface. Internally,

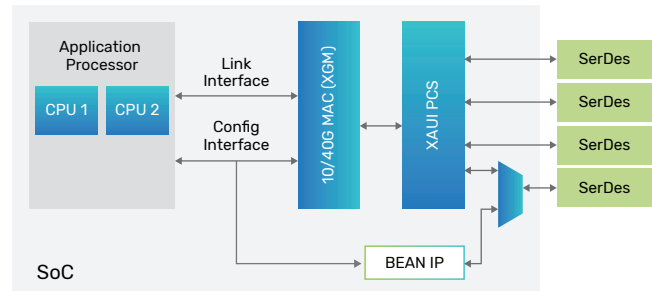


Figure 1: Example system-level block diagram

Benefits

- ▶ Low-risk solutions—silicon-proven design
- ▶ Ease-of-use—customizable with easy integration
- ▶ Designed by an industry leader—Cadence is an active contributor to the IEEE 802.3 standards working groups

the Cadence BEAN IP datapath is configured for a 20-bit SerDes interface clocked at 156.25MHz. For other bit widths, transmit and receive gearboxes are needed.

For a 10-bit SerDes interface, the transmit (TX) path, receive (RX) path, and the SerDes interface are clocked at 312.5MHz. The 10-bit receive data is stored and presented to the Receive Path 20 bits at a time. An internal toggle signal activates the Receive Path every other clock cycle.

For a 16- or 32-bit SerDes interface, the interface is clocked at 644.53MHz or 322.265MHz, and Transmit Path and Receive Path are clocked with a separate 156.25MHz clock. A receive gearbox deletes bits from the incoming data stream to deliver

Key Features

- ▶ Compliant with the IEEE 802.3ap Clause 73 standard
- ▶ Supports 10-, 20-, 16-, and 32-bit SerDes
- ▶ Generates and recognizes DME frames
- ▶ Generic 32-bit interface for register configuration
- ▶ Interrupts generated for completion of auto-negotiation and when new pages received
- ▶ Supports next page reception and transmission

20 bits of data every 6.4ns to the receive align module in the Receive Path. A transmit gearbox takes data from the Transmit Path and presents the data to the SerDes at the required clock rate.

Priority resolution is performed by the Cadence BEAN IP. Control signals are provided for top-level control to switch to the appropriate configuration.

Configuration Interface

The Configuration Interface connects to the on-chip configuration interface so that the Cadence BEAN IP can be configured by the host application.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Ethernet controllers to meet your design requirements.

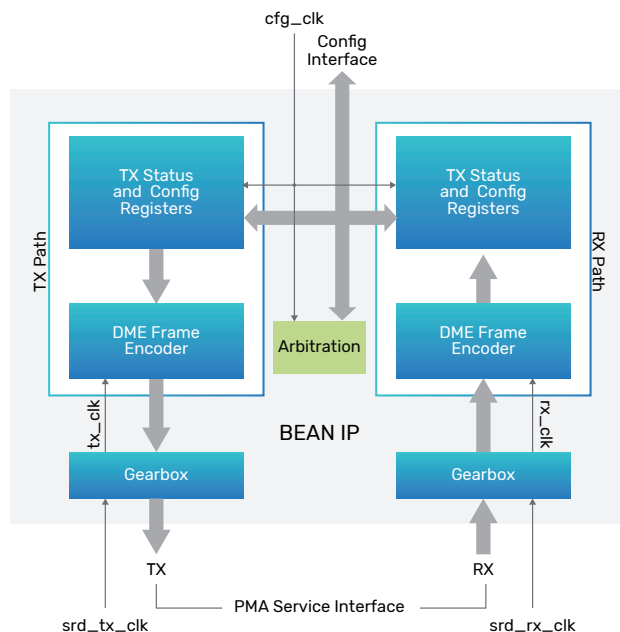


Figure 2: IP-level block diagram

Available Products

- ▶ Ethernet BEAN IP

Related Products

- ▶ Verification IP for Ethernet
- ▶ 100GBASE-R PCS IP (PCSCG)
- ▶ 10G Ethernet MAC IP (XGM)

Deliverables

- ▶ Verilog HDL
- ▶ Synthesis scripts
- ▶ User guide with full programming interface, parameterization instructions, and synthesis instructions
- ▶ Verilog testbench

For more information, visit [cadence.com/designip](https://www.cadence.com/designip)