DESIGN IP BROCHURE

112Gbps ELR SerDes IP for TSMC 7nm and 6nm

Overview

The Cadence® 112Gbps Extended Long-Reach (ELR) SerDes IP for TSMC 7nm/6nm operates at a full-rate of 112Gbps using PAM4 modulation and half-rate of 56Gbps using PAM4 modulation, as well as 56/28/10Gbps using NRZ. This IP enables high-speed communications between chips, backplane, and long-haul optical interconnects by converting between parallel data and extremely high-speed serial data streams with improved signal reliability. The ELR PHY provides additional performance margin to high-loss and reflective channels by incorporating reflection cancellation and enhanced digital signal processing. The area- and power-optimized design is ideal for high port-density applications that require long-reach and medium-reach links.

The 112G SerDes IP supports primary Ethernet data rates listed in Table 1 within +/- 200ppm. An integrated micro-controller allows for fully autonomous startup, adaptation, and service operation without requiring ASIC intervention. A programming and observation interface is provided via a parallel bus with MDIO-style addressing (port, device, address).

Table 1. Transceiver operating data rates	
PAM4 full-rate	103.125Gbps, 106.25Gbps
PAM4 half-rate	51.5625Gbps, 53.125Gbps
NRZ full-rate	51.5625Gbps, 53.125Gbps
NRZ half-rate	25.78125Gbps, 26.5625 Gbps
NRZ 10G	10.3125Gbps

There are several comprehensive on-chip diagnostic tools that enable testability and easy debugging. A post-equalized histogram is available for accurate estimation of bit error rate (BER) even in the absence of actual bit errors. Vertical eye statistics can be logged to allow optional optimization of the device settings. The Channel Estimator hardware allows the accurate measurement of the channel response to assess package, connector, and trace characteristics.

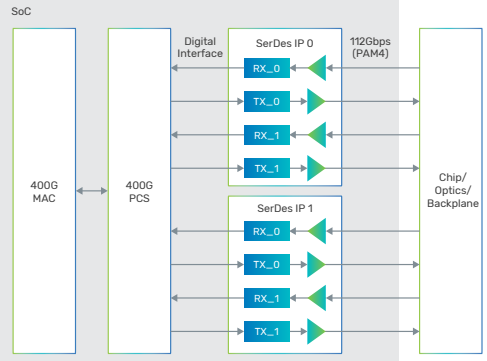

Figure 1: Example system-level block diagram

Benefits

- Best-in-class DSP supports ELR lossy and reflective channels
- Small area and low power is ideal for high port-density applications
- Symmetric floorplan allows north-south and east-west SoC edge placement
- Comprehensive on-chip diagnostic features make system testing/debugging quick and easy

Key Features

- TSMC 7nm/6nm FinFET CMOS Process
- Power-optimized for ELR LR and MR links
- Fully autonomous startup and adaptation without requiring ASIC intervention
- 112/56Gbps PAM4 or 56/28/10Gbps NRZ data rates
- Compact footprint for high-density designs
- Compact footprint for high-density designs

Product Details

There are two instances of the transmitter and the receiver in the IP.

Transmitter

The transmitter (TX) includes standard encoding, a DAC (microcontroller auto-calibrated) that converts digital signals to an analog output, with a digital FIR filter for waveform pre-emphasis. The transmitter drives a 100Ω differential output with adjustable swing.

Receiver

The receiver (RX) includes an analog front-end, an ADC (microcontroller auto-calibrated) that converts the analog input to digital signals, a DSP equalizer, and standard decoding.

Built-In Self Test (BIST)

The TX may be configured to transmit data from an internal PRBS generator using a list of selectable patterns. The RX may similarly be configured to deliver decoded bits to an internal self- synchronizing PRBS checker to count bit errors in the data stream. Received data may be looped back to the transmitter (see Figure 2).

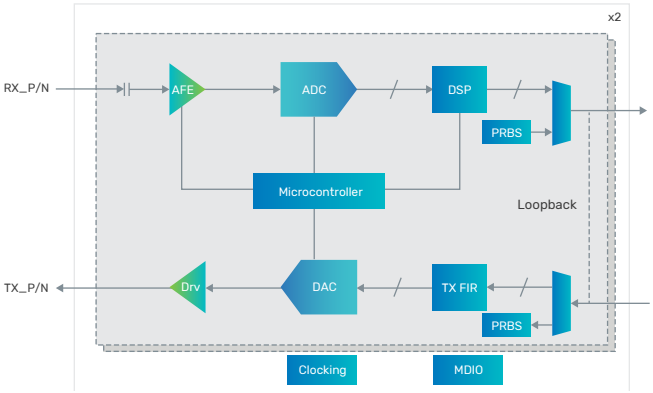

Figure 2: IP-level block diagram

Clocking and Reference Clocks

All timing is derived from an external clock reference via an internal PLL and separate phase interpolators for the TX and RX lanes. The RX timing is locked to the incoming data, while the TX timing reference may be configured to derive either from the external reference, or optionally from the RX timing.

Deliverables

- GDS II macros with abstract in LEF
- Verilog post-layout netlist
- STA scripts for use at chip or standalone PHY levels
- Liberty timing model
- SDF for back-annotated timing verification
- Verilog models of I/O pads, and RTL for all PHY modules
- Verilog testbench with memory model, configuration files, and sample tests
- Documentation, including integration and user guide, release notes
- Verification IP setup files

For more information, visit cadence.com/designip

cadence®

Cadence is a pivotal leader in electronic systems design and computational expertise, using its Intelligent System Design strategy to turn design concepts into reality. Cadence customers are the world's most creative and innovative companies, delivering extraordinary electronic products from chips to boards to complete systems for the most dynamic applications. **www.cadence.com**