DESIGN IP BROCHURE

10Gbps Multi-Link and Multi-Protocol PHY IP

Overview

SerDes requirements for system-on-chip (SoC) designs are becoming increasingly demanding and must support increasing numbers of protocols that must be optimized for cost-and power-sensitive mobile, wireless IoT, consumer, and automotive designs.

The Cadence® 10Gbps multi-protocol PHY IP provides a flexible PHY IP that simplifies the design process without compromising performance, power, or silicon die area (PPA). The PHY IP is a lower-active and low-leakage power design crafted for mobile, wireless IoT, consumer, and automotive designs.

The PHY IP is designed for multi-protocols running on single PHY macro and is compliant with USB 3.1, PCI Express® (PCIe®) 3.1, DisplayPort TX v1.4, Embedded DisplayPort TX v1.4b, SATA 3, QSGMII, and SGMII specifications. The PCS complies with the PIPE 4.2 interfaces, and provides support for the dynamic equalization features of different protocols.

The PHY IP is architected to quickly and easily integrate into any SoC, and to connect seamlessly to Cadence or third-party PIPE-compliant controllers. It provides a cost-effective, versatile, and low-power solution for demanding applications. It offers SoC integrators the advanced capabilities, flexibility, and support that meet the requirements of high-performance designs.

The PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

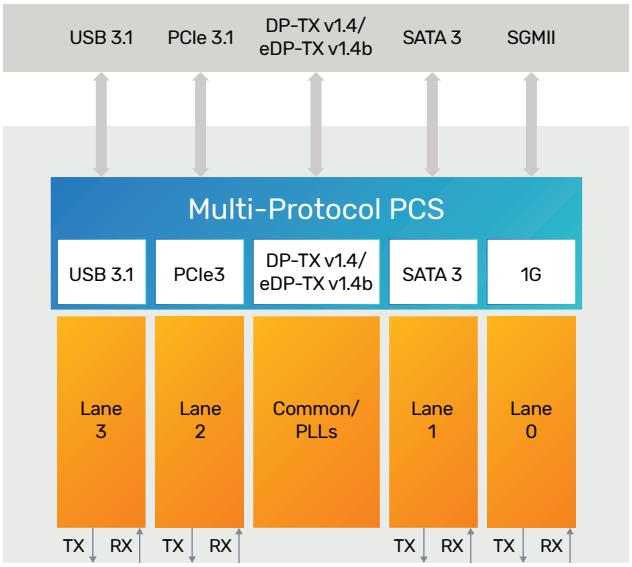

Figure 1: Example system-level block diagram

Benefits

- Multi-protocol multi-link offers optimum SoC configurability
- Optimized PPA for mobile and consumer applications
- Extensive BIST and DFT enable ease of integration, faster bring-up, and quick debugging

Key Features

- Supports USB 3.1, PCIe 3.0/2.0/1.0, DP-TX v1.4/ eDP-TX v1.4b, SATA 3, QSGMII,and SGMII
- Supports PCIe L1 sub-states
- Supports SRIS and internal SSC generation
- Multi-protocol support for simultaneous independent links
- Supports internal and external clock sources with clock active detection
- Automatic calibration of on-chip termination resistors
- Flexible lane configuration from 1 to 8 lanes
- Scan, BIST, and serial/parallel loopback functions

Product Details

The PHY IP is a hard PHY macro available for SMIC processes. I/O pads and ESD structures are included. It is designed to easily integrate with a Cadence controller IP for PCIe, or any third-party controller with a PIPE-compliant interface.

PHY Architecture

The PHY IP macro consists of a physical media attachment (PMA) layer and a physical coding sublayer (PCS). The multiprotocol and multi-link architecture PHY IP is highly-configurable, allowing the PHY to be easily configured to your specific needs.

The PHY IP is designed with a lane-based architecture featuring one common support for up to eight lanes, providing greater control over floorplanning, placement, packaging, and I/O integration than other hard PHY solutions, while maintaining reliability and ease of use associated with GDSII macros.

The PCS portion of the PHY provides the control, encoding, and protocol logic. The architecture partitions the PMA core into different primary sub-modules: common PLL, transmitter, and receiver lane modules. The PMA block provides the transmit, common PLL, and receive functions. The common PLL module also provides the interface between Scan, Arm® AMBA® Bus, JTAG, and analog test including BIST, ABT, Scan, JTAG control, eye plotting, and PMA support logic functions.

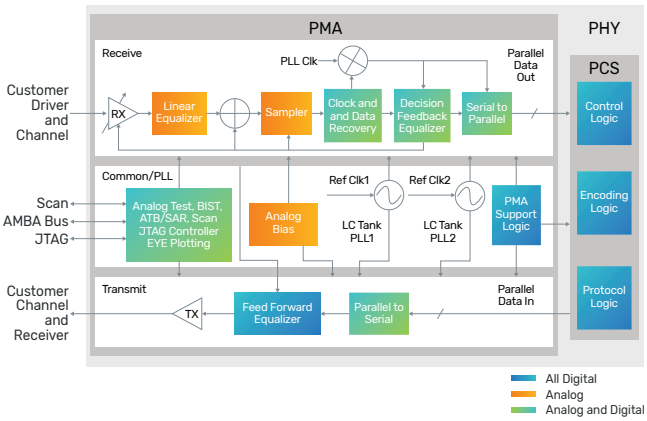

Figure 2: IP-level block diagram

The transmitter module converts parallel data from the PCS interface to a serial data stream. The receiver module converts an input serial data stream to parallel data going to the PCS interface.

Availability

The PHY IP is available with support for the following process nodes:

Process Node	Speed
14SFP	10Gbps
12SFe	10Gbps

Related Products

- Controller IP for USB 3.1
- Controller IP for PCIe 3.1
- Controller IP for DisplayPort v1.4
- 16Gbps Multi-Protocol Multi-Link PHY

Deliverables

- Standard integration views: LEF abstract, timing views (.LIB), behavioral model (Verily), gate-level netlist, SDF, DRC, LVS, ANT reports, and GDSII layout and layer map
- Synthesizable soft PCS with SDC
- Complete documentation including user guide, integration guide, and programmer guide
- HVM kit
- Testboards available upon request

For more information, visit cadence.com/designip

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