New Techniques to Address Layout Challenges of High-Speed Signal Routing

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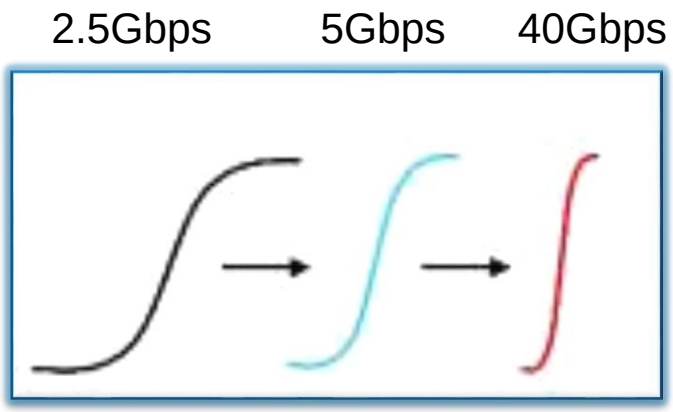
Trend Today

- Ever increasing data rates; more high-speed signal routing
- Signal quality issues arise: Reflection, loss, cross-talk
- Need for decreased design cycle time



Fast Data Rates and Faster Edges

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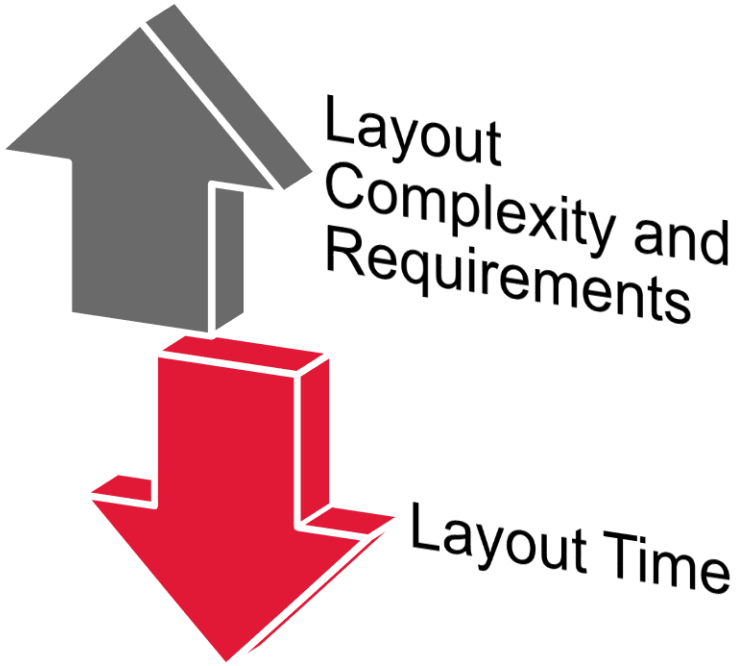
How Does This Impact the PCB Design Task?

- Greater layout requirements
- New and more complex routing strategies to better control impedance and crosstalk
  - Implementation is oftentimes manual, time-consuming, and prone to layout errors or misses
- Increased need for pre-layout simulation
- Less layout time



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In this Session…

- We will talk about new layout techniques that provide a faster and easier mechanism to meet today's complex high-speed signal routing requirements

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High-Speed Signal Requirements We Will Cover…

- Return path
- Mitigating fiber weave effect
- New tabbed routing technology

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Return Path

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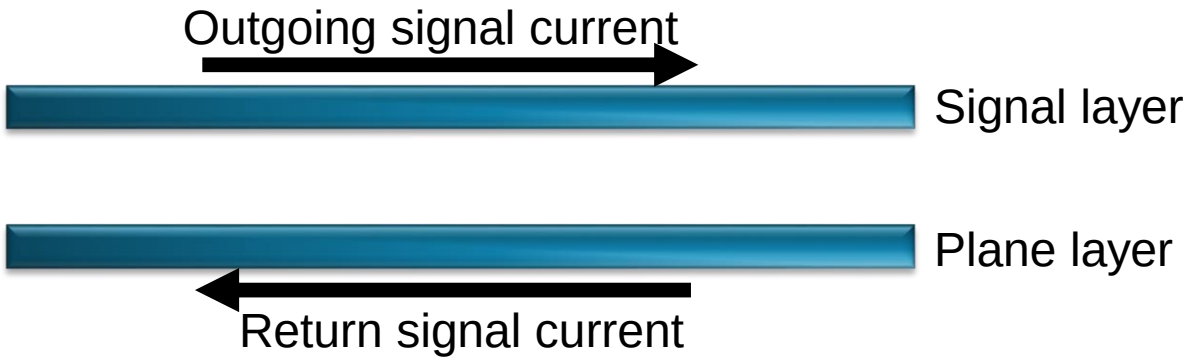
Understanding Return Path

- Currents must always return to their source
- Return current will return to their source along the path of the least impedance



The return currents must complete the loop

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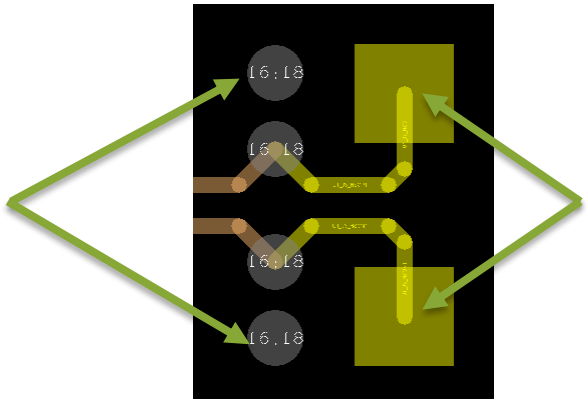
Providing Return Path

- For system clocks and high-speed I/O interfaces—such as **DDR, PCI Express® (PCIe®), USB, SATA**, etc.—if via transition is necessary, it is required to place return path via(s) as close as possible to the location of transition
- Without proper placement of return path vias, the return current must find its own way
- Results in the current spread over a large area, which greatly increases the possibility of cross contamination with other signal currents, creating a loss of SI

Ground vias at layer transition

Provides low impedance path for current to return to source



High-speed differential signals

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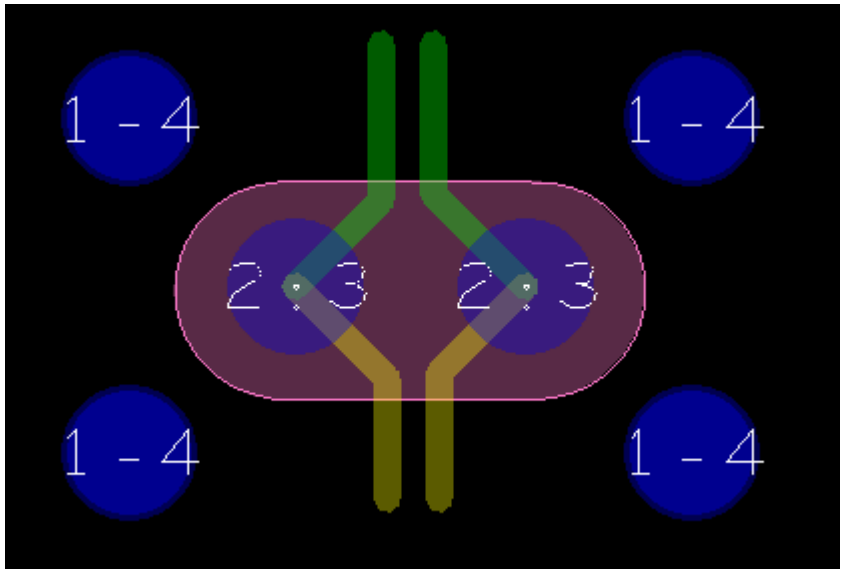
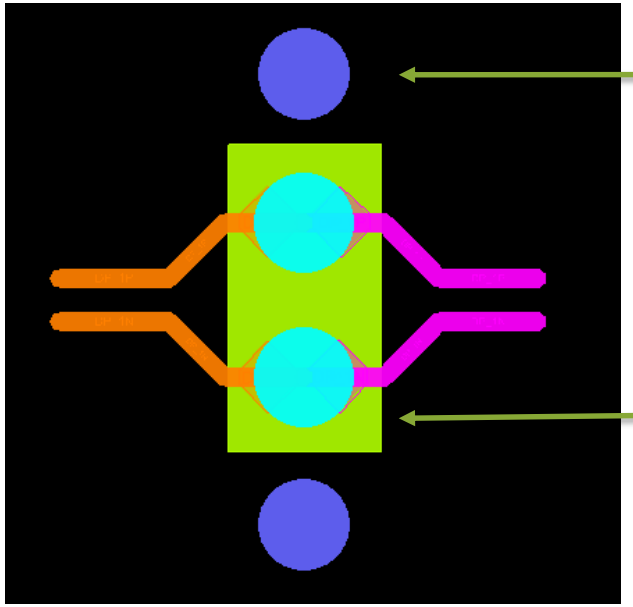
Most Common Guidelines for High-Speed Via Transitions

- Use closely coupled impedance matched differential vias
- Use return vias in close proximity to signal vias
- Use large clearance hole (anti-pad) in the via stack





Use Return Vias

Clearance Holes

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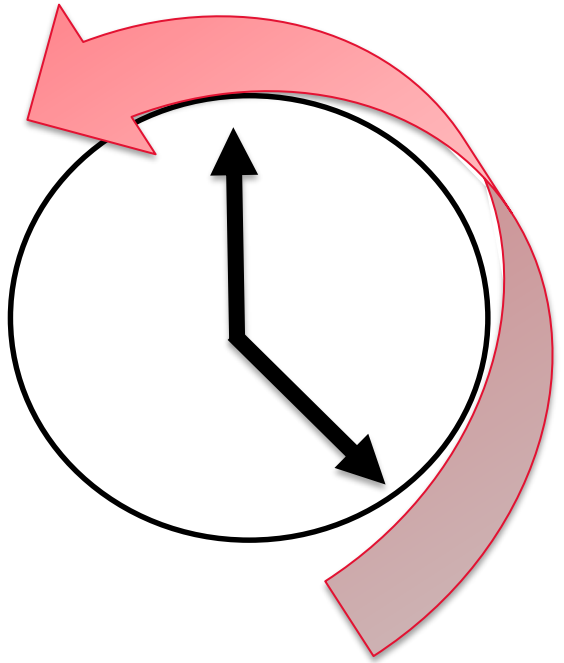
Today’s Typical User Flow

- Some don’t worry about return path vias until finished with all connections
- Some will route the high-speed signals and follow up manually with return path vias
- Some have convoluted solutions where they have built schematic/physical symbols and put these into the netlist



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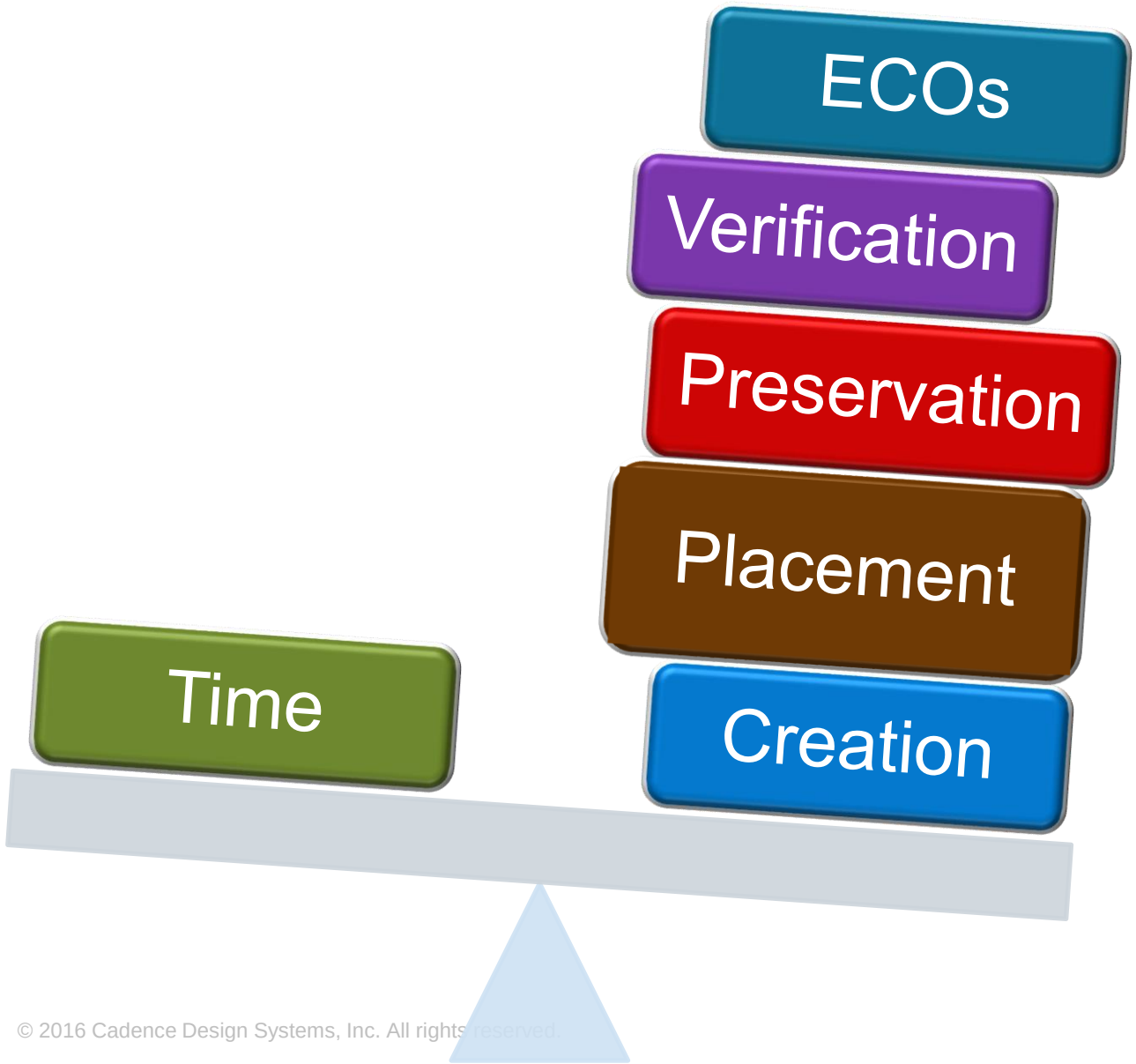
Layout Challenges



- Engineering change orders can be time consuming
- Return path vias placed that do not meet SI guidance can be hours if not days of re-work to correct
- Placed return path vias are left behind/forgotten when users slide routes to another position during edit
- Tedious and painful to add return path vias to hundreds of high-speed signals
- Re-route needed to make room
- Prone to forget adding return path vias to some critical signals
- SI teams are being more specific with return path requirements, slowing down layout process

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New Layout Technique to Address These Challenges

- Use of via structures—A unique methodology that allows you to create reusable elements where you can define correct-by-design high-speed via transitions with custom return paths and voids

- The following slides will describe this new technique using **Cadence® Allegro® high-speed via structures**

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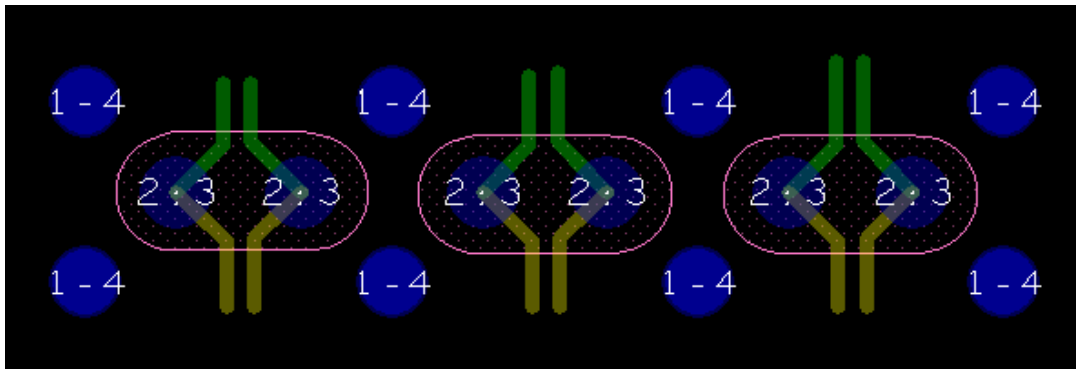
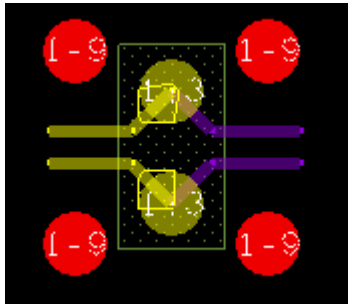
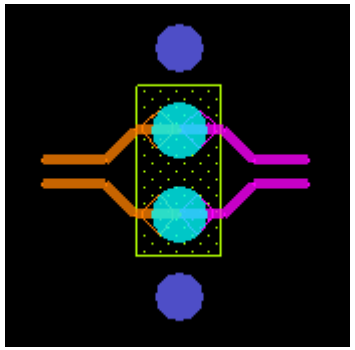
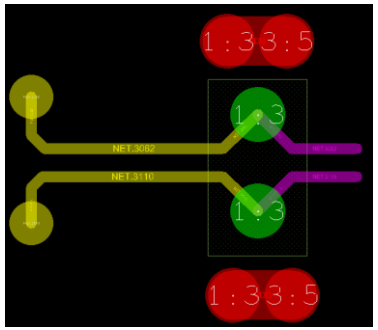
What Is a Via Structure?

- Combine vias, clines, shapes, and route keepouts into a single reusable design element
- Defined as non-component symbols in database
- Supports import and export of XML files containing via structure definition for analysis and re-use in other database









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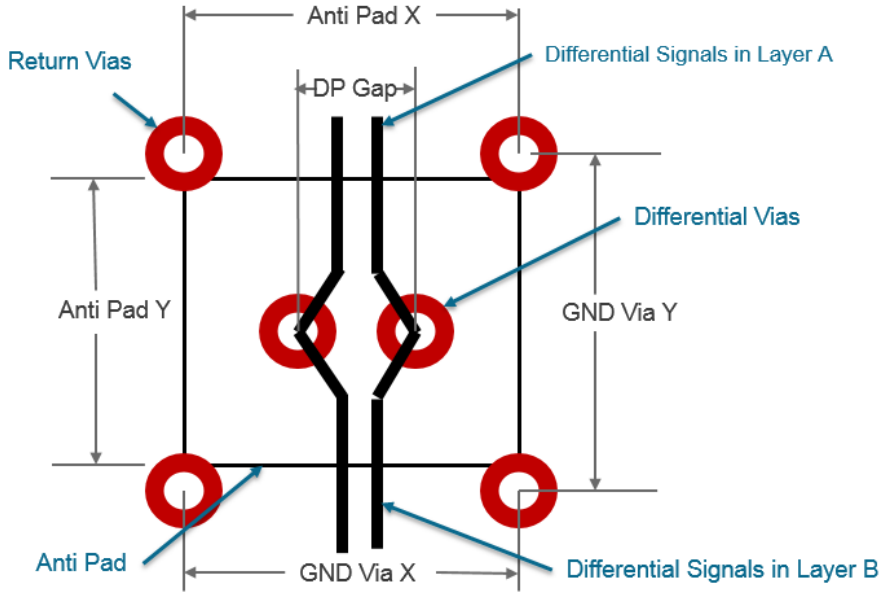
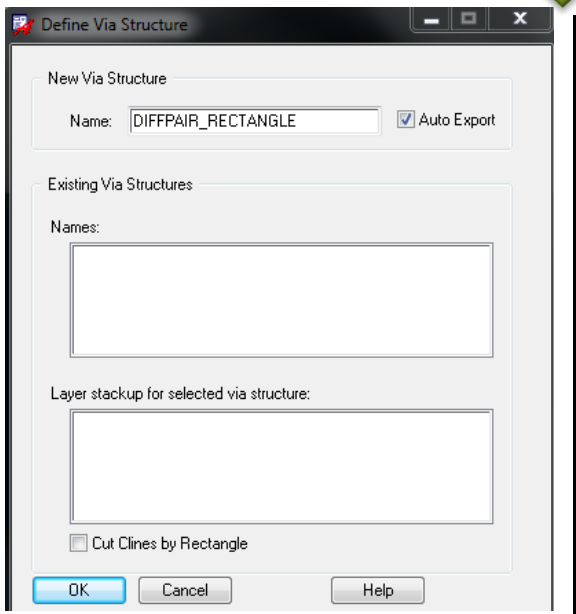
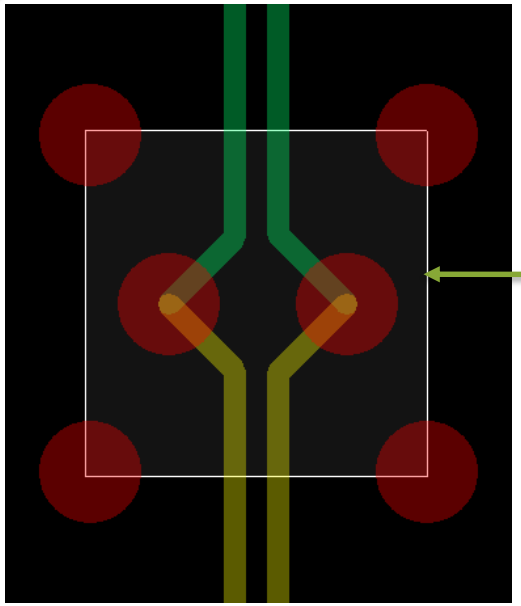
Create It Once

- SI engineers are getting more creative, which results in more complex requirements on:
  - Return path vias: type (thru, BB stacked/staggered), quantity, pattern, and proximity locations
  - Differential pair pad entry/exit (trace width, entry/exit pattern)
  - Void (layers, pad clearance, shape)
- Create one instance per requirement and define as via structure







Use Route Keep-Out for Custom Voids

Allegro Platform Creates High-Speed Via Structure

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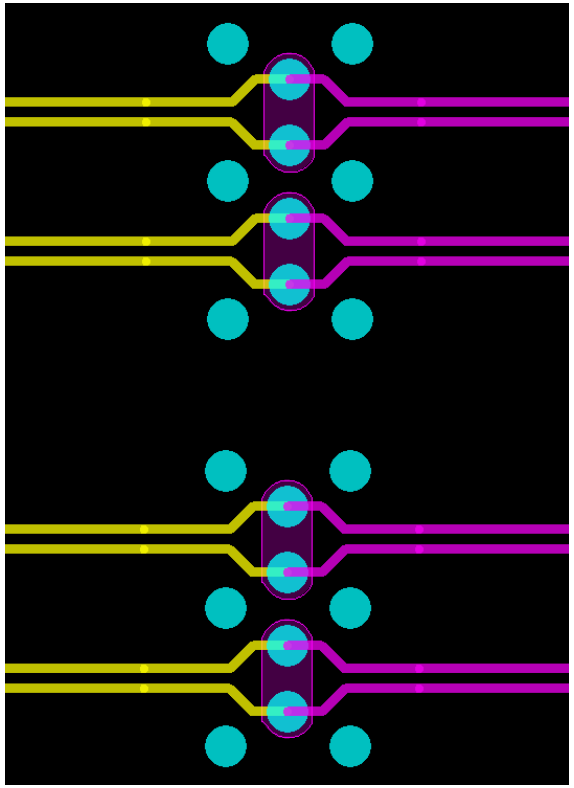
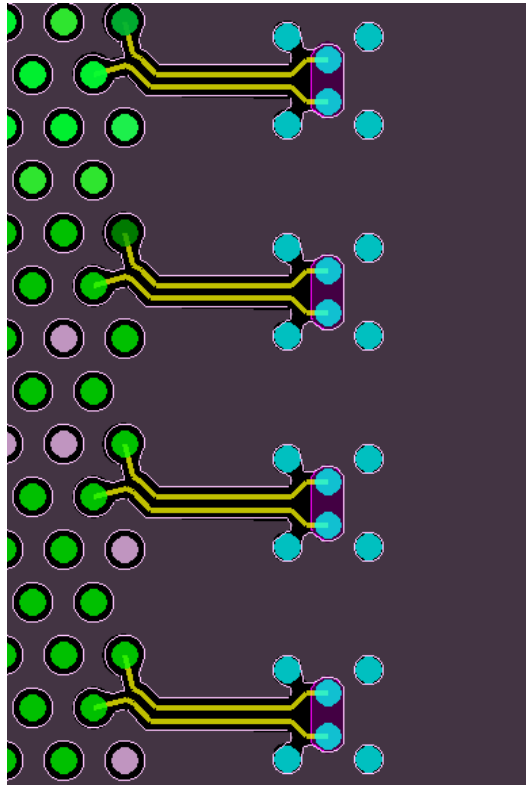
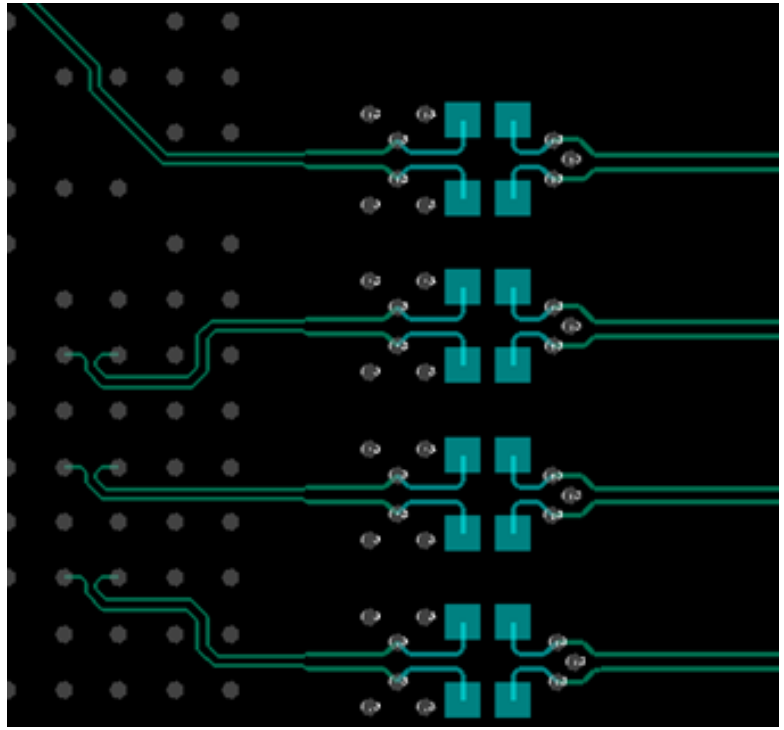
Re-Use Multiple Times

- Place high-speed via transitions as one entity—is a whole lot faster to add and manage in design
- Re-use in same design or another database
- Via structures stay together during placement and interactive editing so they can never be unintentionally altered to ensure the design intent always remains intact







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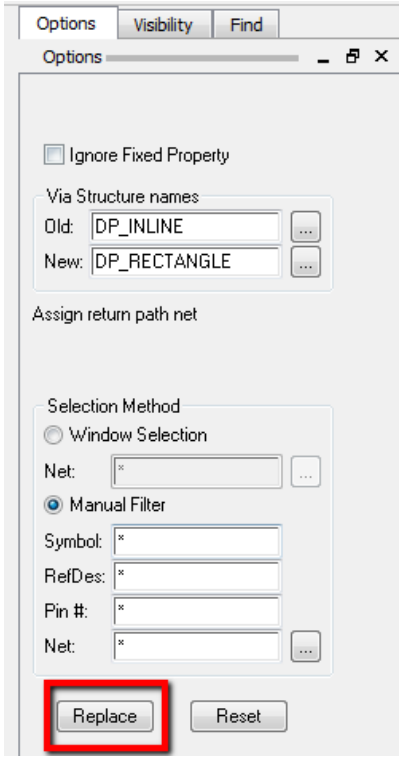
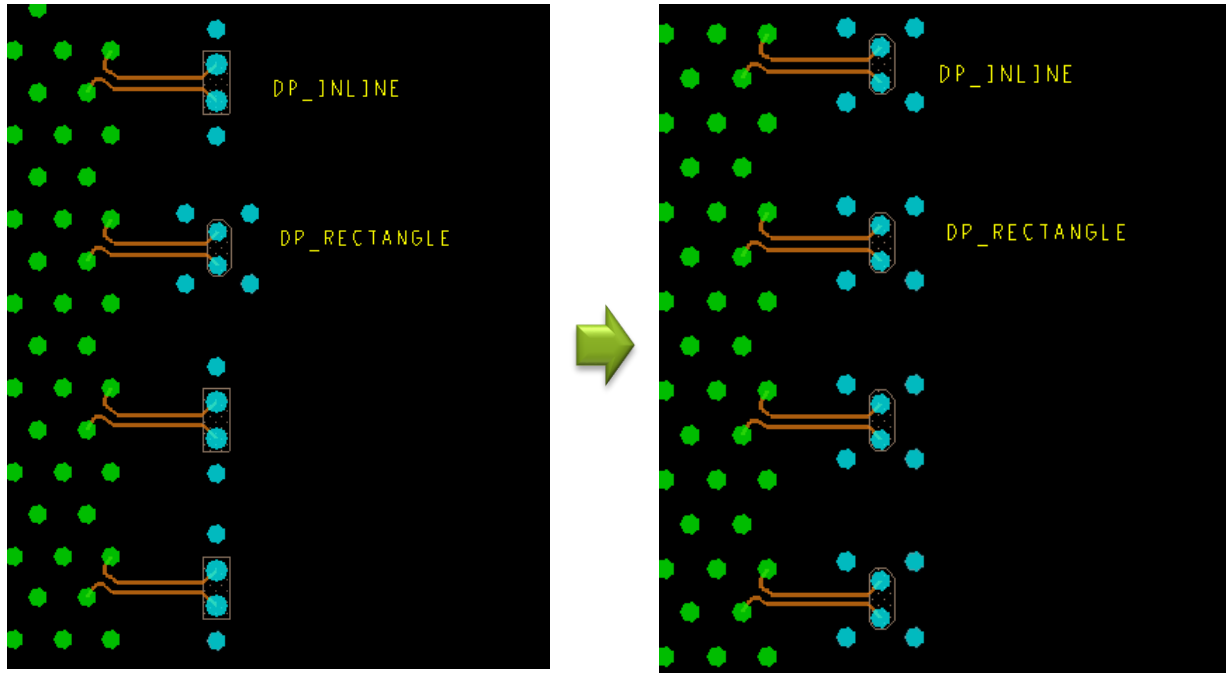
Change Is Easy

- Using via structures makes it easier to replace some or all instances with a different via structure





Allegro Platform Replaces Via Structure

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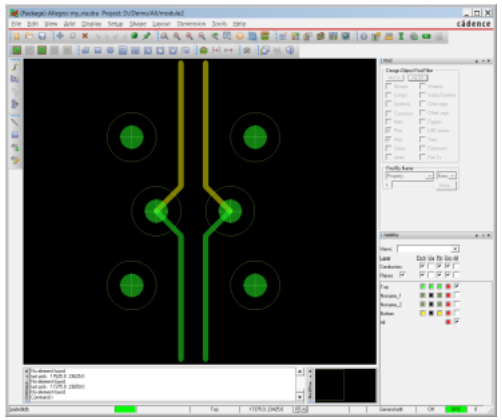
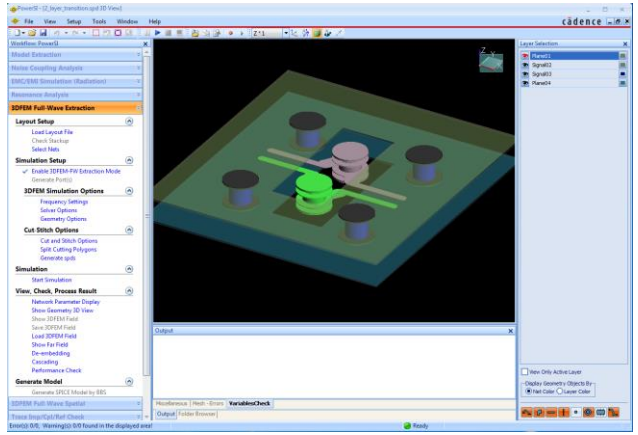
Analysis Is Key, Optimize



Allegro

Physical Extraction



Sigrity™ 3D-EM

Via Structure library

Import/Export

eXML structures

Import/Export

- Allegro platform directly consumes via structures during physical design
- Allegro platform builds necessary pad stacks, no library dependencies
- Allegro can create and edit via structures
- Via structures stay together during edits in layout

- Allow SI to define and drive high-speed via transition structures directly into Allegro designs
- Reduce burden and overhead on physical design teams to meet and adjust to SI guidance

Allegro – Sigrity 3DEM Integration

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Fiber Weave Effect

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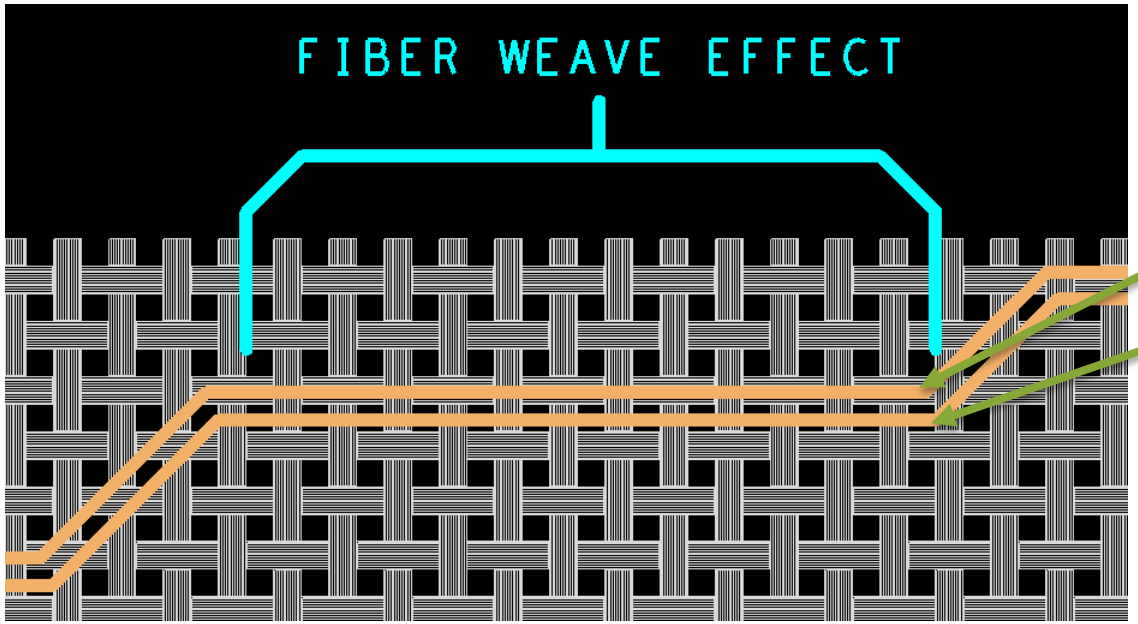
What Is “Fiber Weave Effect”?

- Timing or phase skew caused by fiberglass reinforced dielectric substrate between two transmission lines of the same length
- Traces routed directly over the fiberglass weave will see a different dielectric constant than the traces that are routed over the voids in the weave where only epoxy resin is present
- At high data rates, this dielectric constant mismatch can cause signal integrity issues when running these high-speed signals parallel to the void areas of PCB fiberglass weave



Trace running directly over glass fiber

Trace running directly over epoxy

This results in a degraded differential signal as glass and epoxy have different permittivities on PCBs

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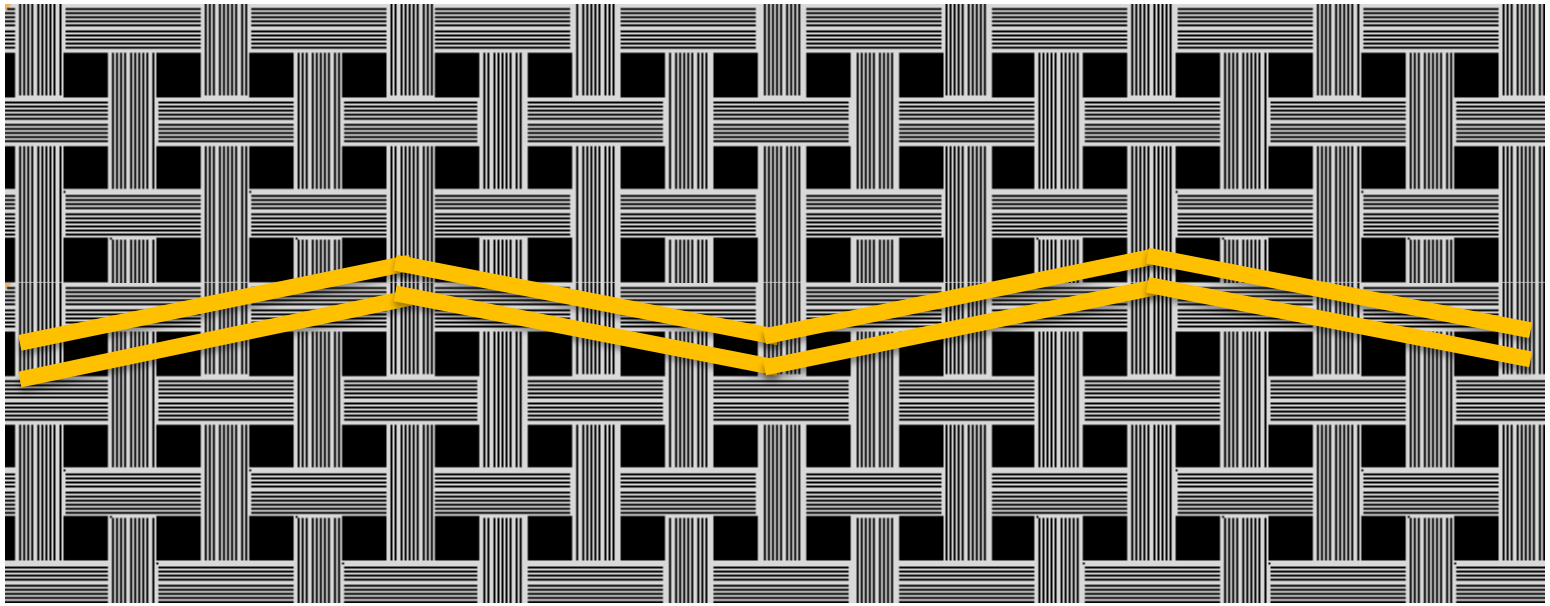
Typical Layout Routing Guideline

When routing for a considerable length, it is oftentimes recommended to do zigzag routing to mitigate the negative effects of fiber weave on high-speed differential signals by forcing the traces to be out of alignment with the fiber weave

- Angle of zigzag can be 1-10 degrees to skew traces relative to weave
- Typical value used is 10 degrees to sufficiently skew trace



Typical for **>5GT/s**, the fiber weave effect becomes significant when the trace alignment to weave is 4”or longer

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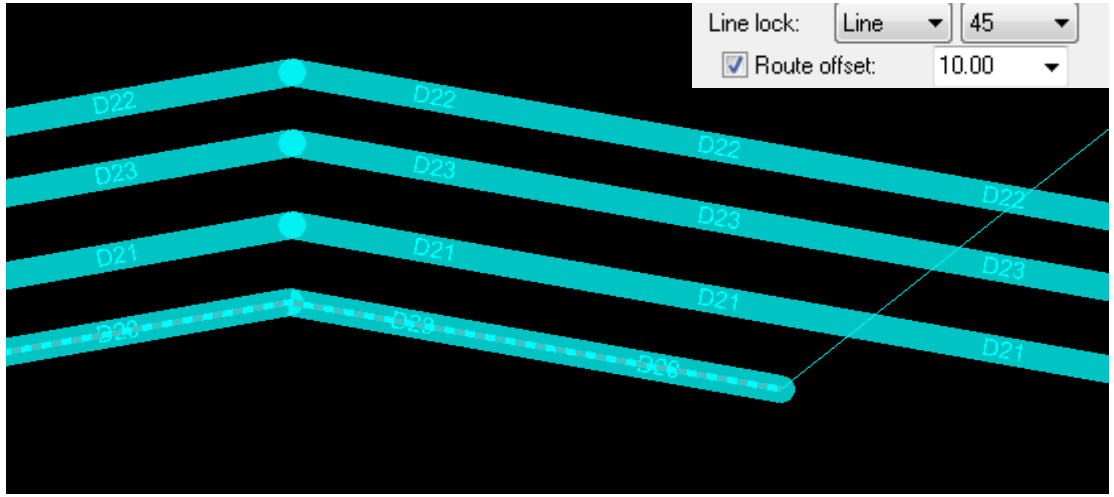
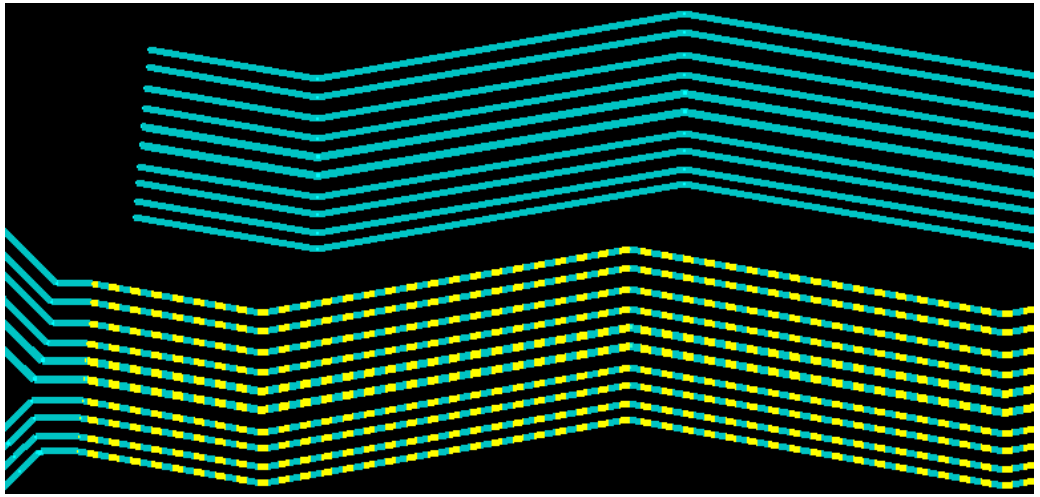
Typical User Flow

- User manually constructs routes rotated at 10 degrees
- If doing zigzag routing, user will have to manually ensure lengths of each “zig” do not go beyond maximum recommended length
- Copy zigzag routes to other buses



Using Allegro Route Offset in Add Connect



Copying Zigzag Routing

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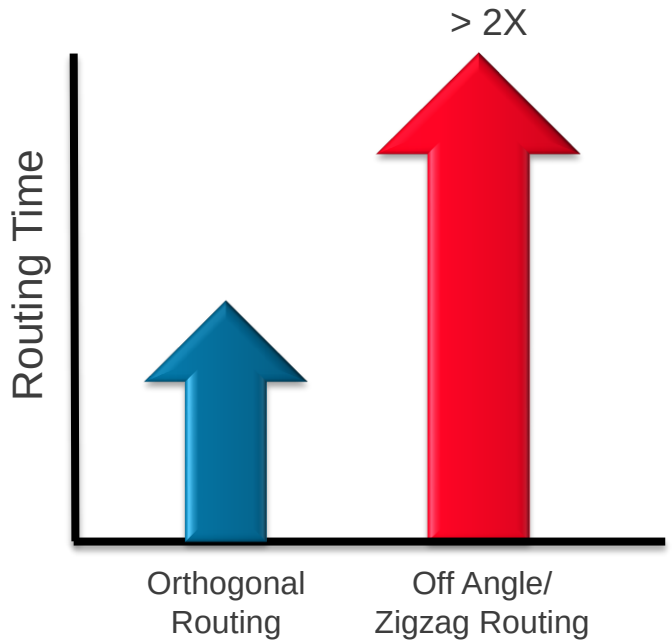
Layout Challenges

- CAD tools don’t easily support routing at angles other than 0, 45, or 90 degrees
- Significant increased layout time
  - Estimated routing time is at least doubled compared to typical orthogonal routing
  - More painful and time consuming to edit layout



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New Layout Technique to Address These Challenges

- Route in normal orthogonal or 45 degrees, which is easier to finish connections and make edits as necessary
- Once routing is final, convert orthogonal or 45 degree traces to zigzag

- The following slides will describe this new technique using **Allegro Add Zigzag Pattern**

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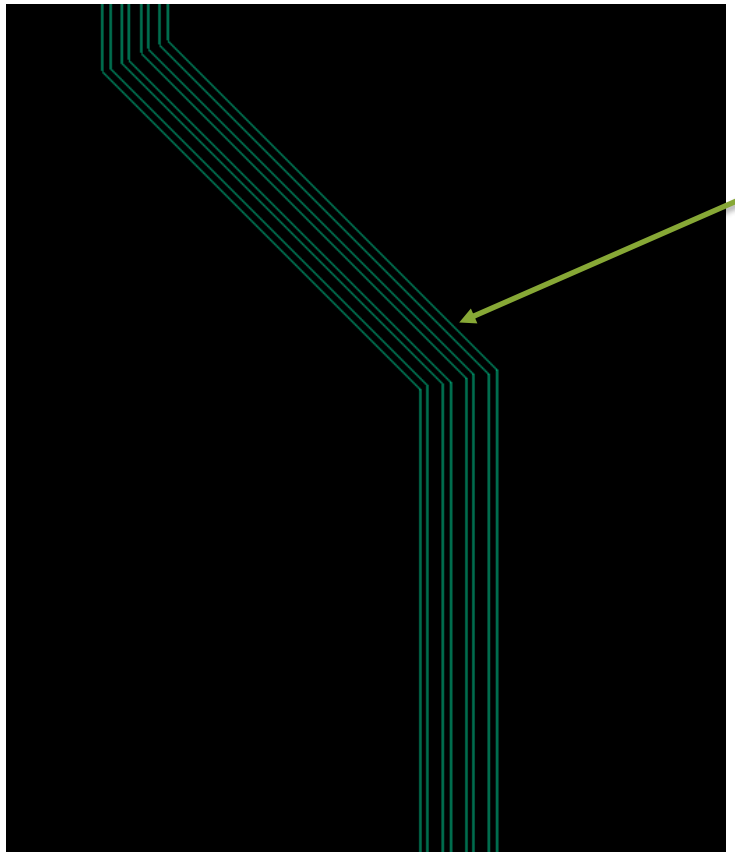
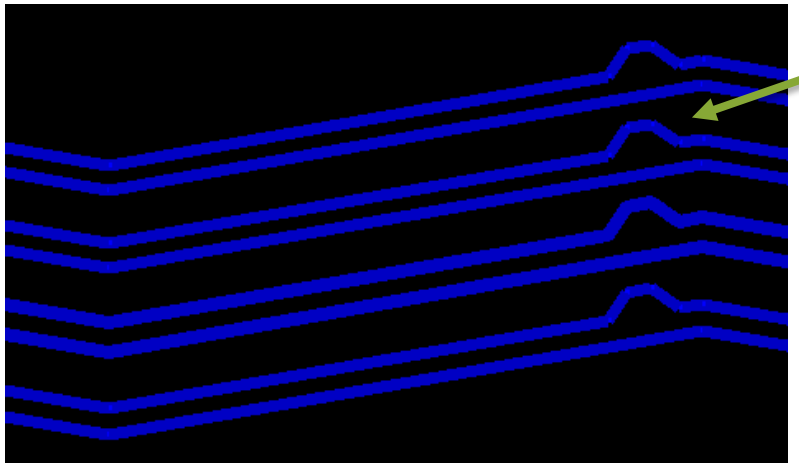
Recommended Design Preparations

- Route high-speed signals as normal in orthogonal or 45 degrees
- Make sure that traces are parallel
- Plan ahead and leave enough spacing when routing traces for phase bumps



Route in orthogonal or 45 degrees
Keep traces parallel



Plan for phase bumps as needed

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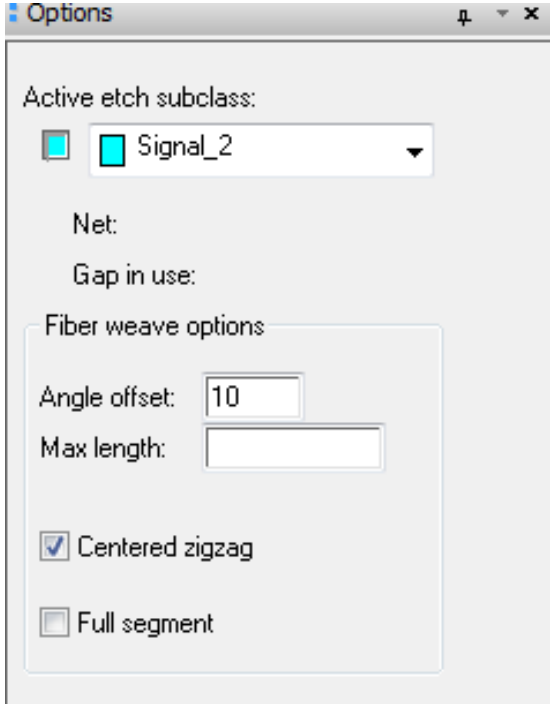
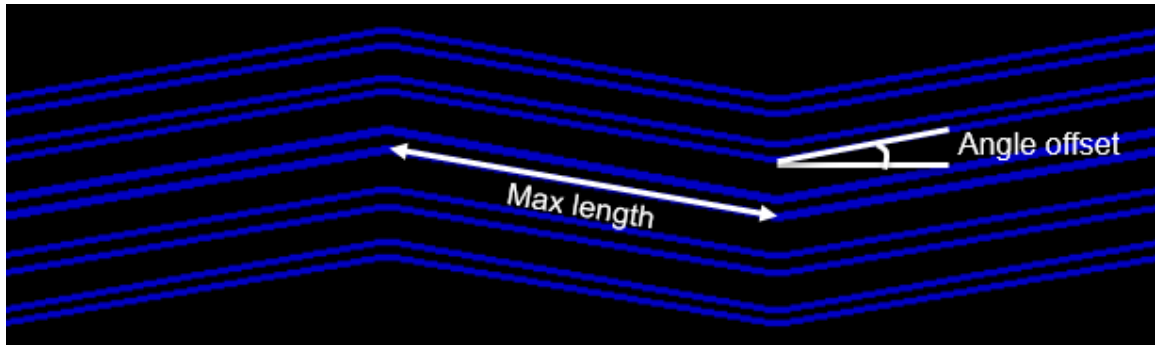
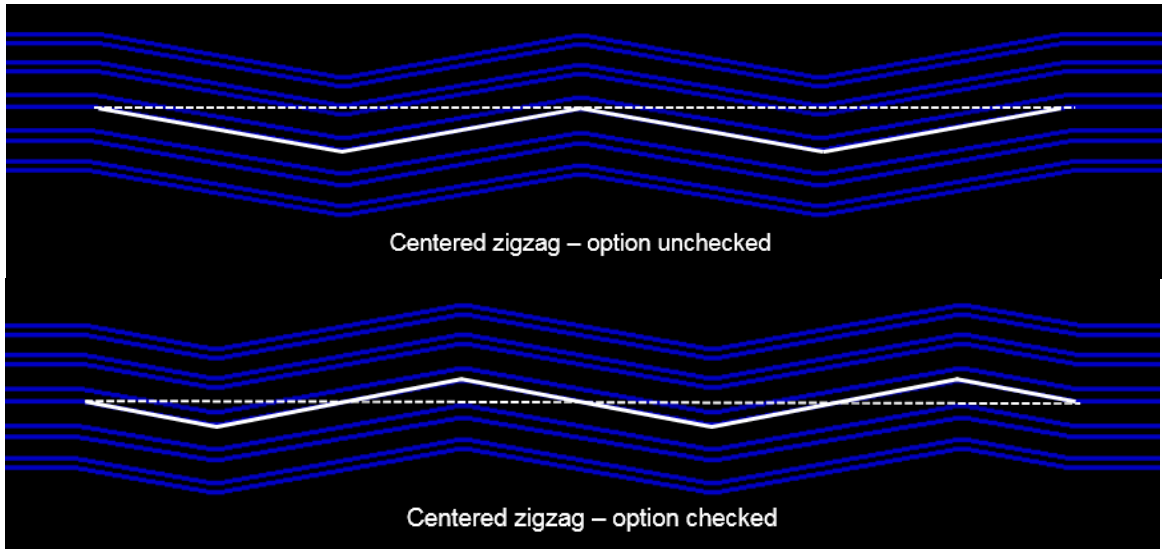
Using Add Zigzag Pattern

- Specify zigzag angle and max length per SI guidance
- Based on area spacing, specify whether to place zigzag centered relative to axis of original segment



Allegro Add Zigzag Pattern





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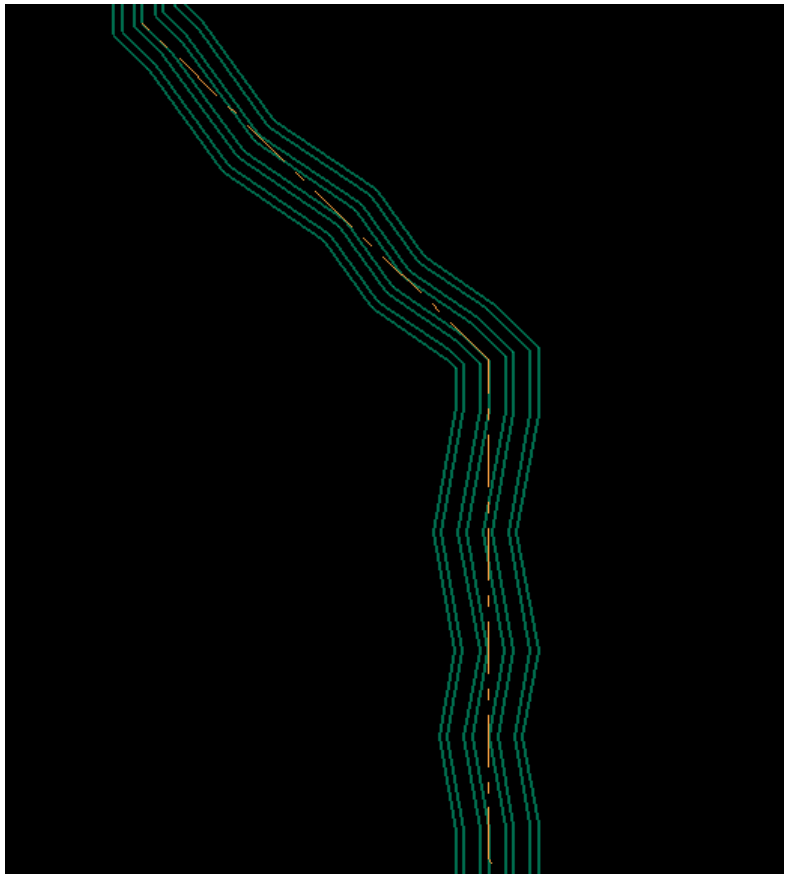
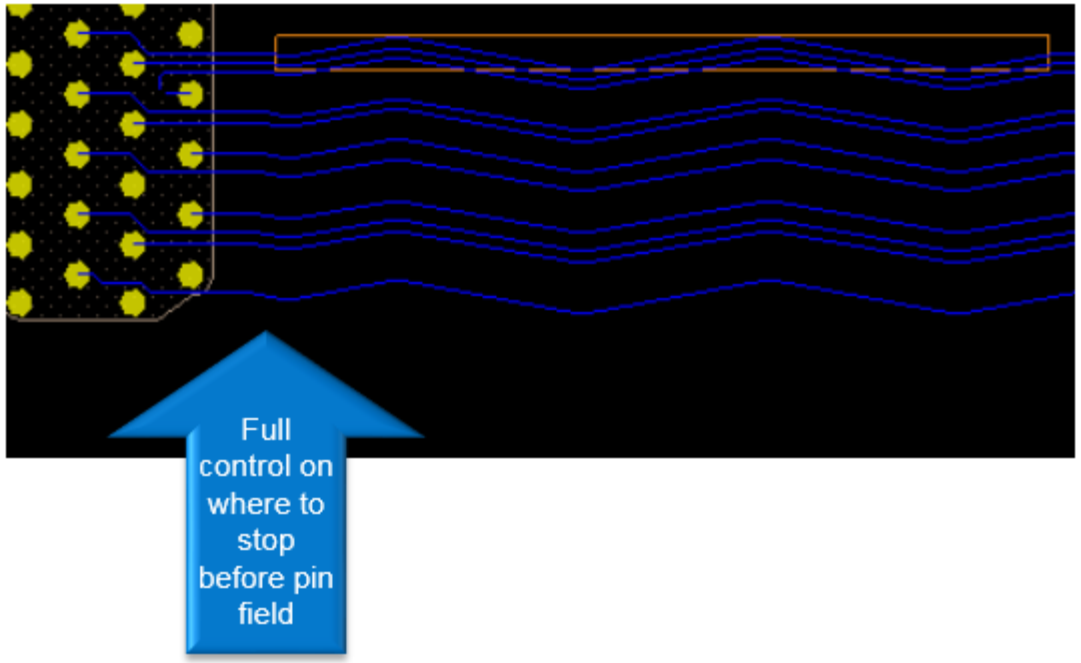
- Convert full parallel segments automatically or dynamically define start/end points of zigzag conversion



Full Segment Zigzag Conversions

Dynamically define start/end points to maintain routing in pin fields



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Tabbed Routing

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What Is “Tabbed Routing”?

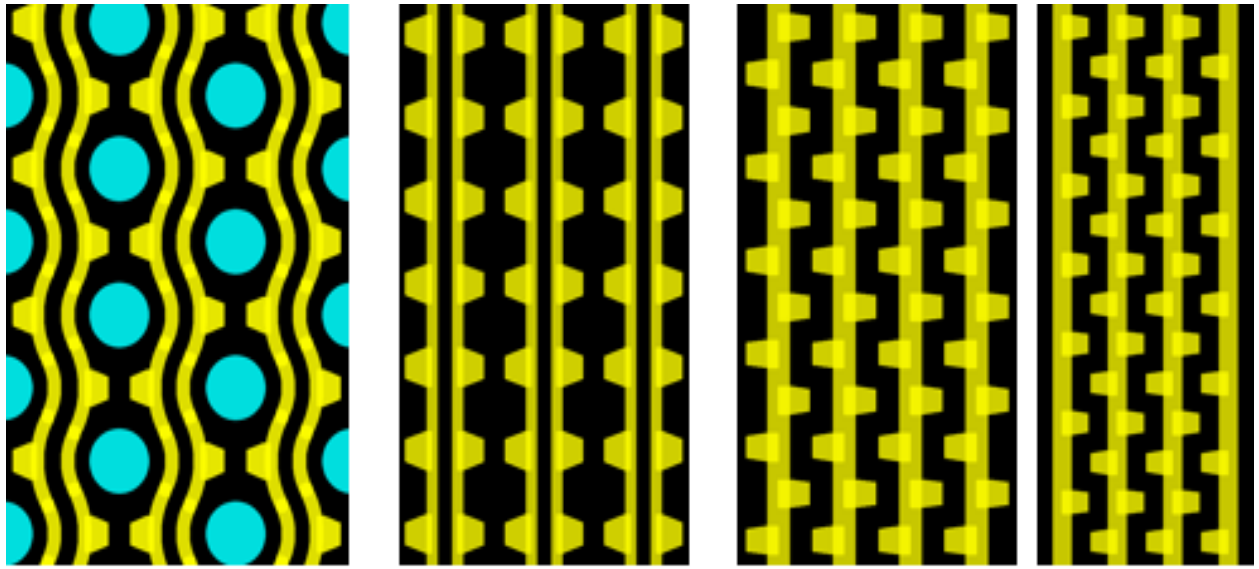
- New routing method in which trapezoidal shapes called tabs are added to parallel traces

Benefits

Impedance control in pin field/breakout region

Manage crosstalk in open field region

Allows for longer trace lengths and more compressed routing



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Layout Challenges

- Adds a lot of layout complexity to meet requirements
- Design engineers must maintain spreadsheet to do manual tab count matching required to maintain same flight time and achieve crosstalk cancellation effect
- Difficult to manage tabs once placed on routes

The following slides will describe tips and new techniques using **Allegro Tabbed Routing** to address these routing challenges

Tabbed Routing Features

Allegro PCB Designer High-Speed Option enables:

- Tabbed route generation
- Tab count validation
- Tab pitch validation
- Move and Delete Tabs
- Manage tabs when traces are edited

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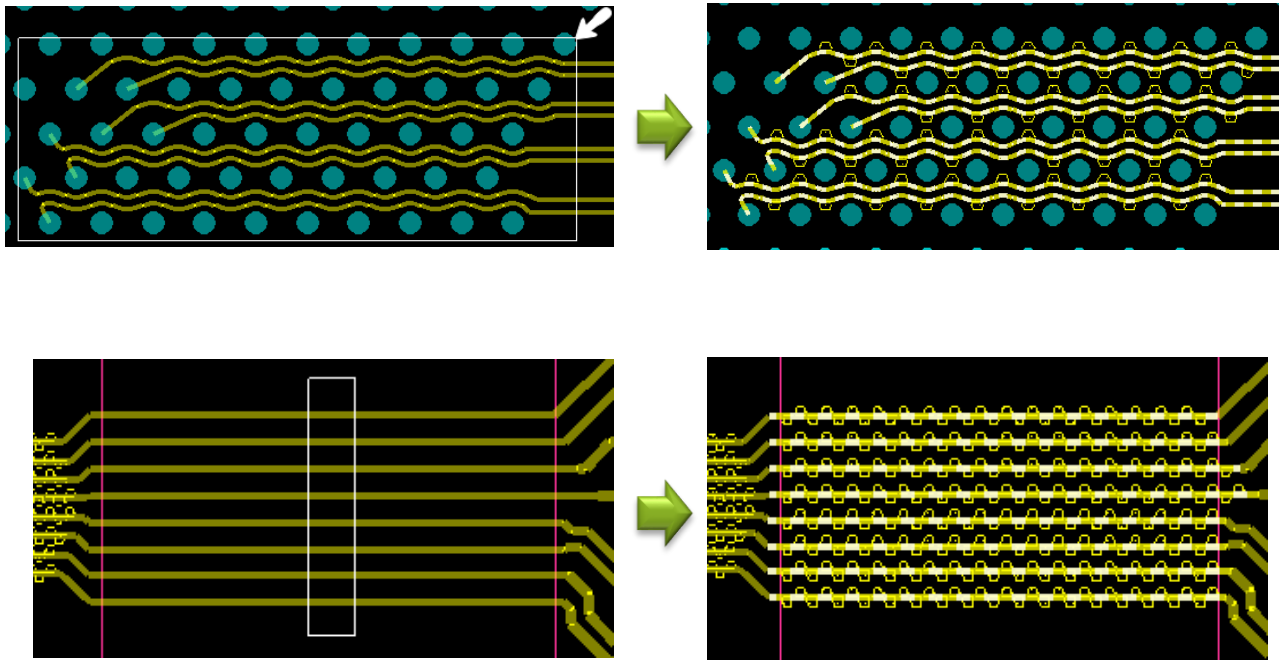
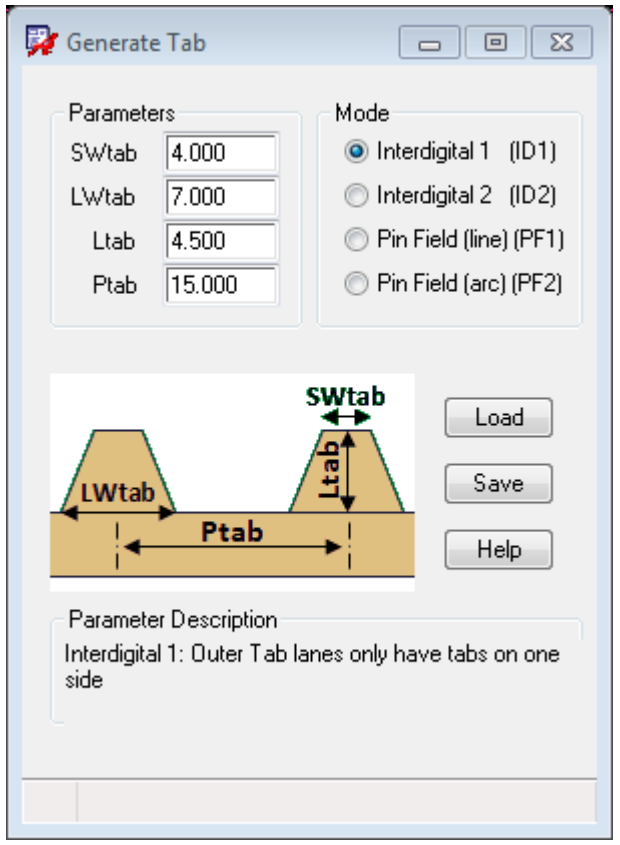
Layout Tips and Techniques

- It is recommended to finalize routing and verify trace spacing before adding tabs to cline segments
- To generate tab, select mode, enter tab size/pitch values, and select parallel cline segments to generate tabs using Allegro generate tab





Allegro Generate Tab

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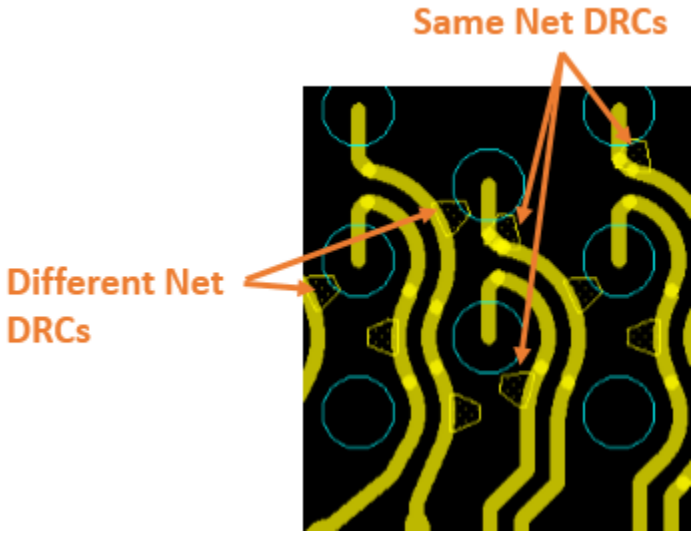
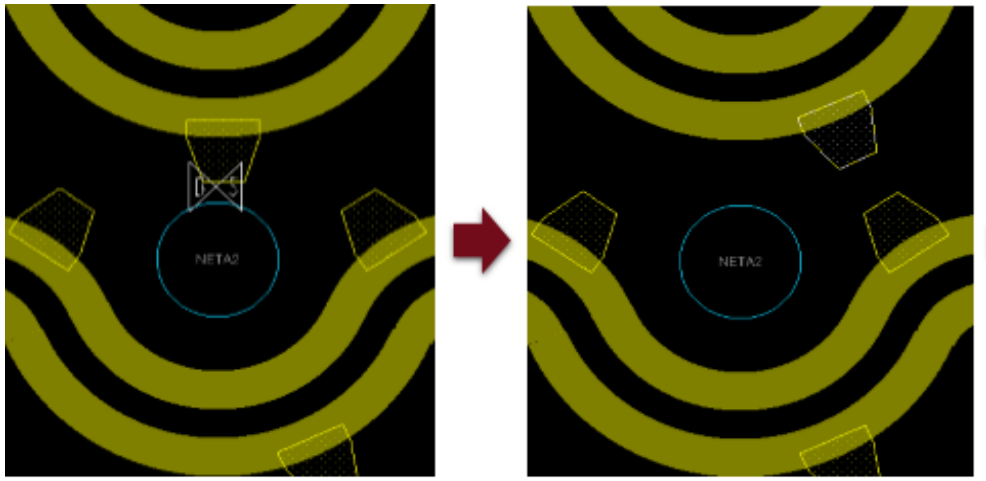
- It is recommended to create the proper constraint regions around the segments with tabs for the different routing regions (i.e., pin field, breakout, and open field) to limit invalid DRCs
- Do not forget to enable the relevant different net and same net spacing checks to capture DRCs, such as below



Users will oftentimes need to move a tab to resolve DRCs created during generation of tabs. Below, Allegro Move Tab is used to move tab along segment while maintaining centerline connectivity. It provides dynamic DRC feedback so you can easily resolve these types of spacing violations.



"Generate Tab" command creates tab on center of arc causing DRC

Use "Move Tab" command to resolve DRC

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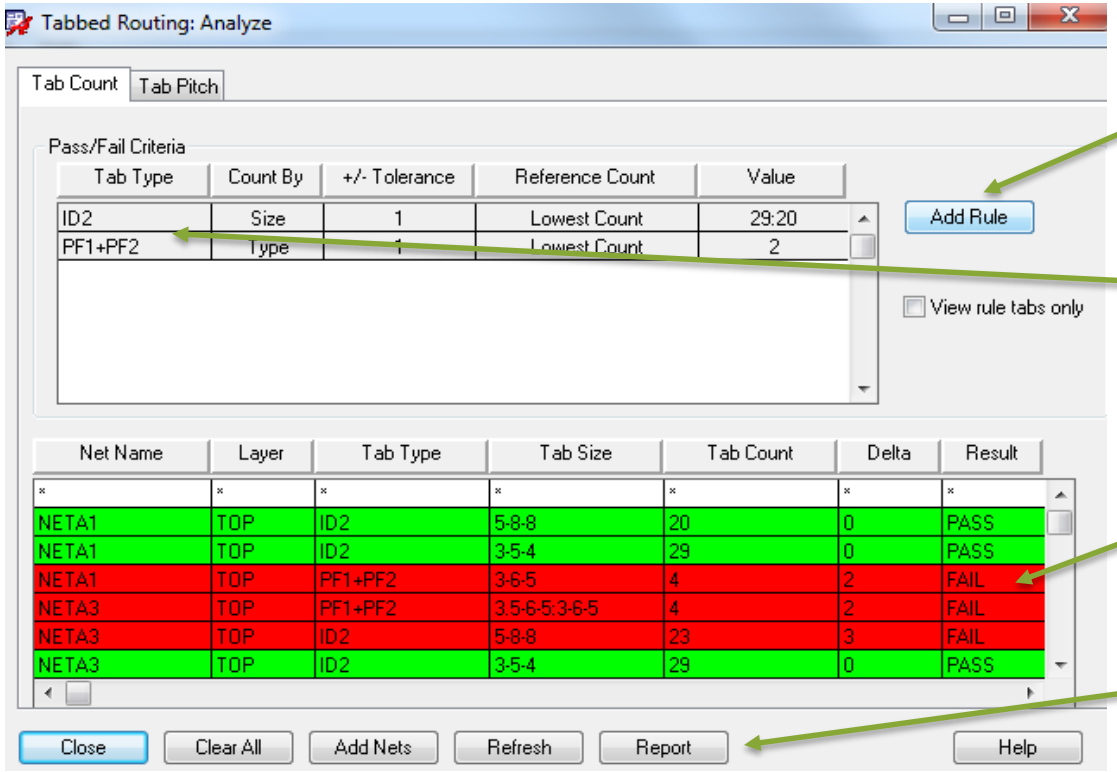
Tab Count Matching

- Typical requirement is that tab # difference between bits in same byte cannot be more than a certain difference (typically 1 or 2) to maintain same flight time and achieve crosstalk cancellation effect
- Allegro tabbed routing analyze is used to validate and find violations in design:



Allegro Analyze Tab

Define custom rules for pass/fail criteria and cross-probe violations in canvas for fast fixing

Pin Field Tab # and Interdigital Tab # are usually separate when matching, they cannot be added or removed to meet tab number matching requirements

Violations shown in red—when selected, cross probes in design for easy identification and fixing

Generate custom reports to suit various data needs

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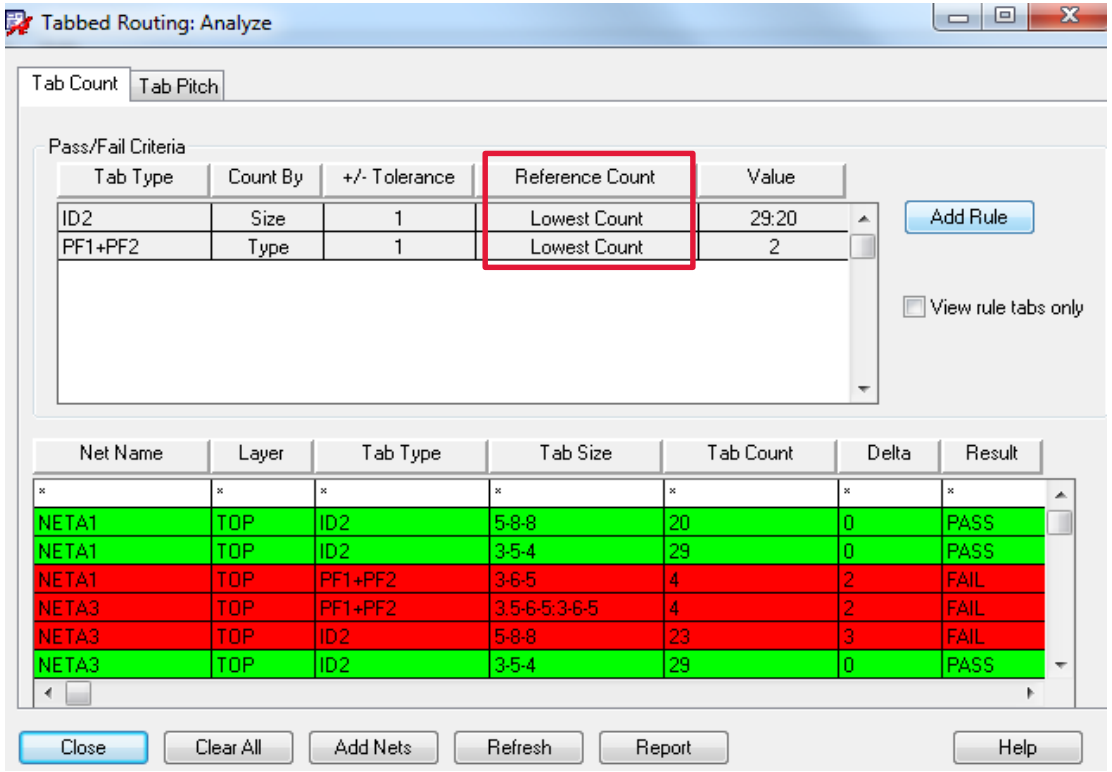
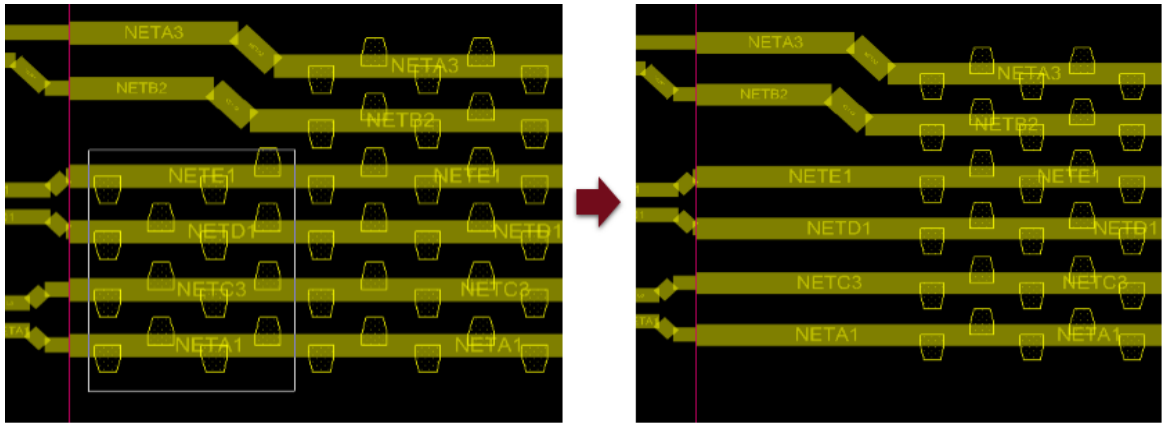
- Easier to delete tabs to meet tab count matching requirement than to add tabs
- Recommend to set Reference Count = Lowest, which sets reference count used for Pass/Fail criteria during tab count matching to be the lowest tab count from selected nets per tab type/size



If Allegro Delete Tab is used to delete tabs, analyze table results is automatically updated to make is easy for users to see results



Allegro Delete Tab can delete tabs by instance, cline segment, or cline

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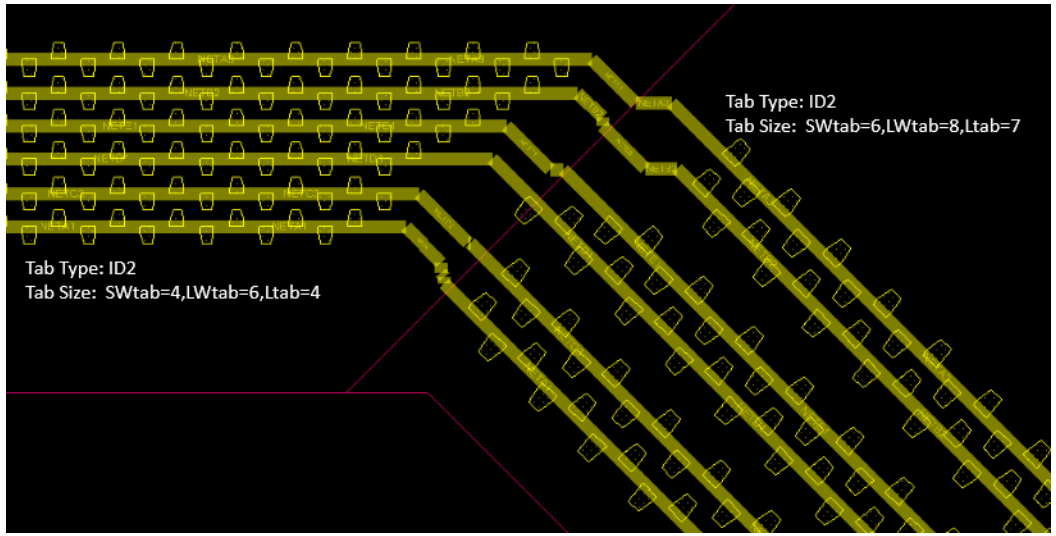
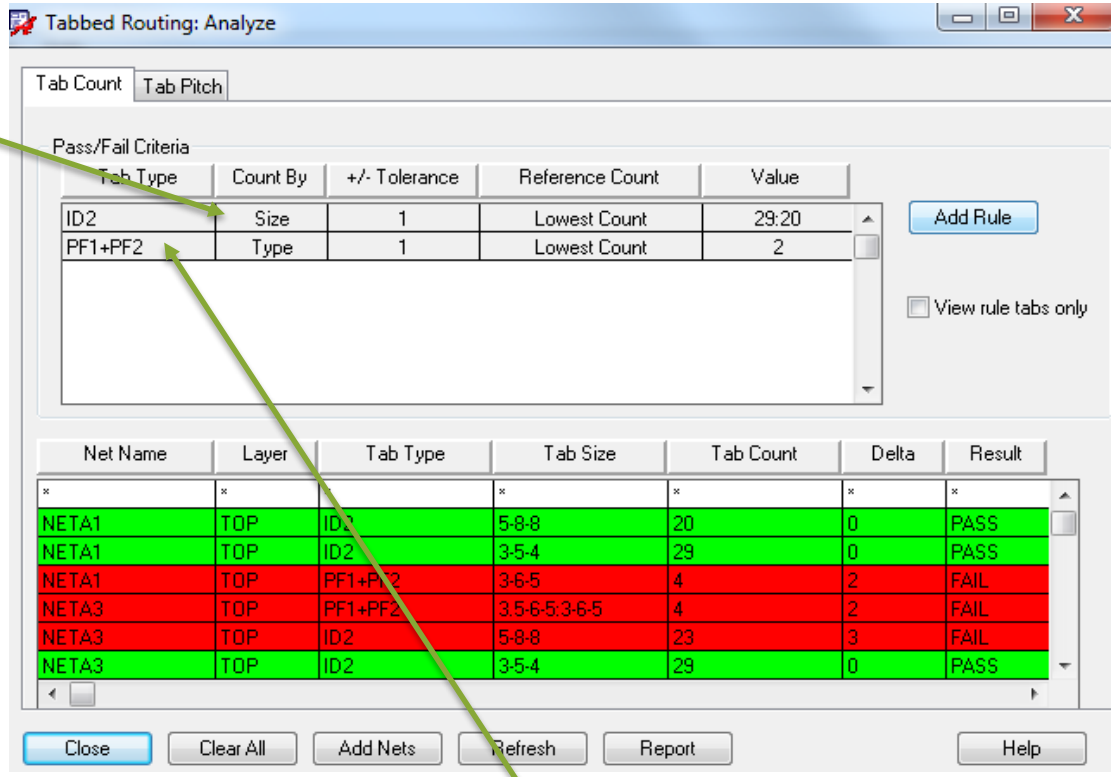
- When different trace widths and spacing are used in open region, different interdigital tab dimensions (sizes) are used

Option is available to do tab count matching separately for each tab size for a given tab type. As an example below, the tabs are all type ID2 but have 2 different tab sizes used for different area of routing.





- Typically, same tab dimension in both pin field (PF2) and breakout (PF1) region is applied and tab count is combined

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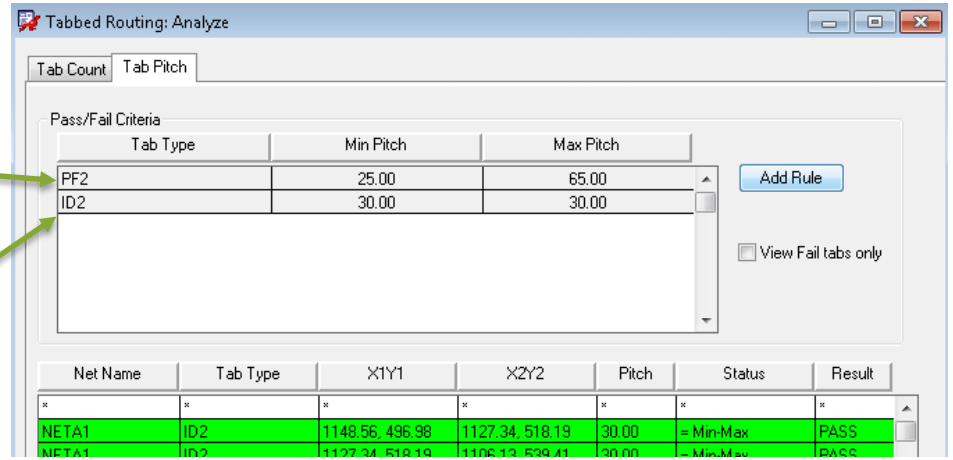
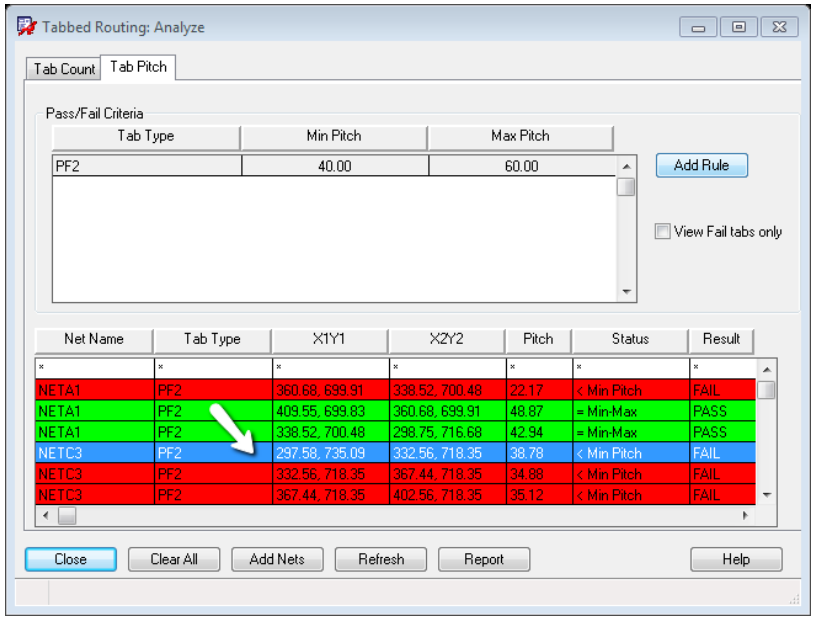
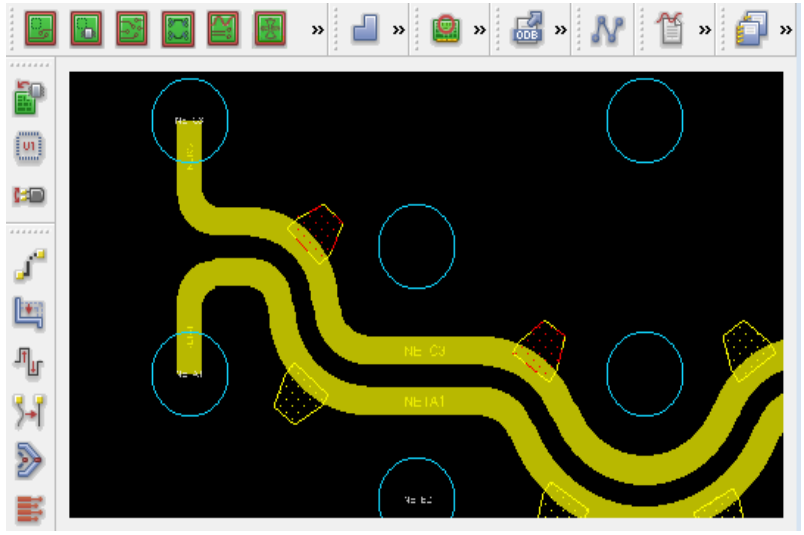
Tab Count Pitch

- For pin field and breakout region where pitch requirement might be relaxed due to non-uniformity in routing, user can set min and max pitch rule values per design guideline
- For Interdigital tabs where the pitch requirement is typically an absolute value, user can set min and max pitch rule values to be the same value







Use move tab to resolve identified pitch violations

Create custom rules and cross probe to easily find violations and fix

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THANK YOU,

PCB WEST SHOW MANAGEMENT