Managing Backdrilling from Library until Handoff to Manufacturing

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PCB WEST 2016
Conference & Exhibition

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Managing Backdrilling from Library until Handoff to Manufacturing
Today's challenges

- High-speed interfaces handling 5Gbps or higher are commonplace in many electronic designs today

- Transitioning these high-frequency signals between layers can greatly affect signal integrity when a portion of plated through-hole (PTH) is left unused, forming a stub

- Utilizing the full length of the barrel or introducing buried or blind vias in the design can minimize the stub effects

- Stubs can be removed using a board fabrication process called backdrilling, sometimes referred to as controlled-depth counter-boring

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Managing Backdrilling from Library until Handoff to Manufacturing
What is backdrilling?

- Backdrilling is a board fabrication process that removes the unused section of PTHs, typically connector pins and signal vias

- A secondary, controlled depth drilling pass(s) removes all electro-deposited plating material in the PTH, ensuring signal stubs are minimized

- Backdrilling can be performed from either side of the PCB and to multiple depths

- Tradeoffs between signal quality and manufacturing costs must be considered as well as the trade between signal integrity and board testability

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# Managing Backdrilling from Library until Handoff to Manufacturing
This paper will…

- Discuss why PCB designers should be concerned with unused section of PTHs when routing high-speed interfaces

- Provide an overview of the manufacturing process, expectations, and fabrication vendor requirements for backdrill

- Outline design practices in support of backdrilling and developing a complete data package to streamline the release to manufacturing

- Review functionality in Cadence® Allegro® PCB Designer 17.2 – 2016 to support backdrilling

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Why Is It Important to Minimize PTH Stubs?

- ● Electrical stubs
    - – PTH stubs are the unused section of the barrel where the signal is not required to travel
    - – In general, stubs are a source of impedance discontinuities and signal reflections, which become more critical as data rates increase

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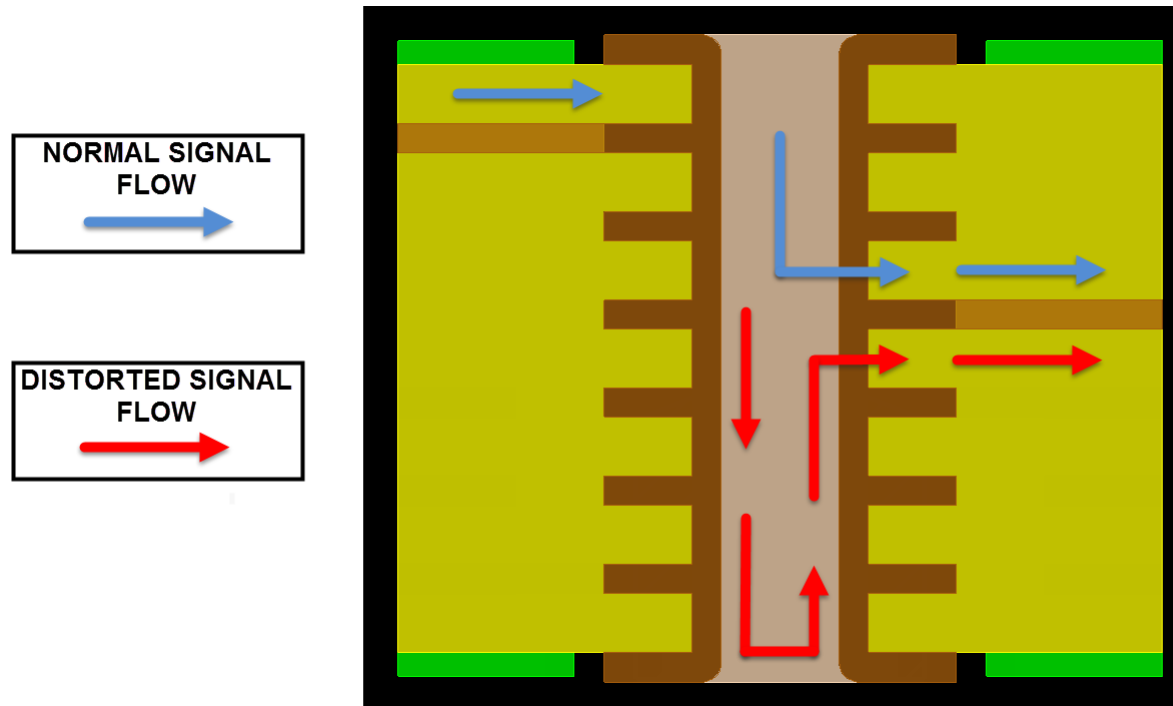
What Can Be Done to Minimize PTH Stubs?
Routing technique

- During route planning of high-speed interfaces, define constraints to only allow connections on layers closer to the surface

- Helps minimize stubs but may cause extra delay as the routes transition further up or down the PTH

- High-speed routing normally has a minimum stub length requirement and delay (length) requirement
  - Using this method may require taking into account the Z-axis length of the route in the PTH

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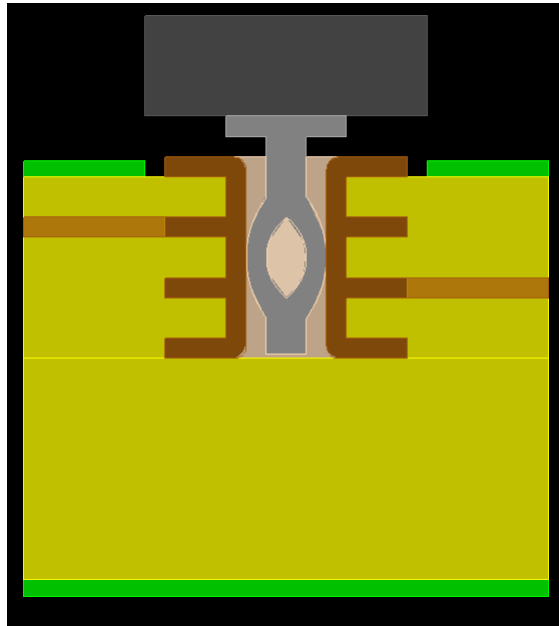# What Can Be Done to Minimize PTH Stubs?
PCB construction – Routing vias

- Use different technologies in design for routing high-speed signals:
  - Blind or buried vias: Sequential lamination using mechanical drilling
  - Micro vias: Sequential build-up using laser drilling

- Leads to higher PCB manufacturing costs due to multiple lamination cycles
  - Not all nets can have stub minimized unless multiple sub composite are constructed on sequential lamination

- In most cases, limited to routing vias and does not address minimizing the stubs on high-speed connector pins

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What Can Be Done to Minimize PTH Stubs?
PCB construction – Press-fit connectors

- Even if design budget can support added expense of different via technologies, you may have an issue with press-fit connectors that limits use

- Compliant pin of a press-fit connector has a collapsible press-in zone that requires full contact to the PTH barrel

Press-fit pin in blind drill (rare)
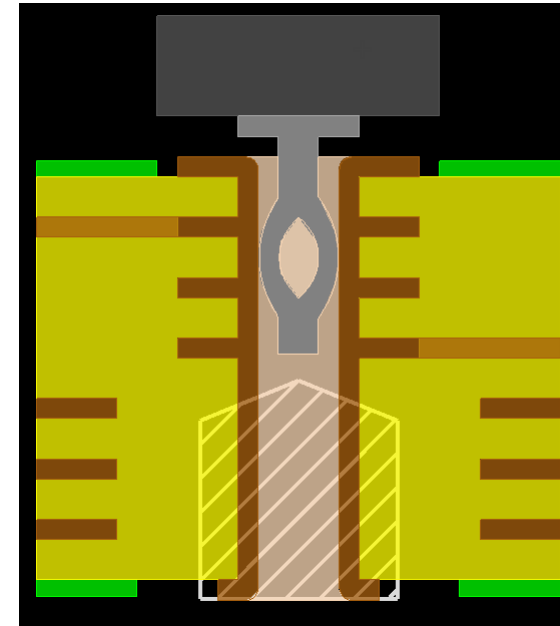
Press-fit pin in through drill backdrilled

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What Can Be Done to Minimize PTH Stubs?
Backdrilling away the stub – In the early years

- Fabrication vendor-identified backdrill opportunities based on critical net list and make all the appropriate adjustments to support backdrilling

- Would remove as much stub as possible on the identified high-speed signals, adjusting features at each backdrill location and verifying copper clearances due to the increased backdrill size to maintain design integrity

- Could be a nightmare to manage and required working very closely with your fabrication vendor to ensure design intent is maintained
  - Necessary to keep a close eye on non-recurring engineering (NRE) charges when relying solely on fabrication vendor to make all appropriate adjustments to support backdrill!

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What Can Be Done to Minimize PTH Stubs?

Backdrilling away the stub – Design requirement to reduce modification by fabricator

- Identify backdrill layer depth pairs required for backdrilling to eliminate stubs
  - Be careful to not backdrill locations which are required for assembly in-circuit testing (ICT)

- Pad size updates in support of the backdrill process
  - Reduction of copper pad size on backdrill start layers
  - Increased solder mask opening on backdrill start layers

- Backdrill clearance
  - Extra clearance on signal and plane layer at backdrill locations
  - Critical step in process to avoid having adjacent connections drilled away or possibly creating internal shorts

- Backdrill size
  - Larger backdrill size compared to the initial PTH size

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What Can Be Done to Minimize PTH Stubs?
Backdrilling away the stub – Fabrication data package requirements

- Separate NC Drill files for backdrilled locations
  - Backdrill holes of different depths require separate drill files
  - Backdrill holes on different sides of the PCB require separate drill files

- Fabrication drawing drill chart should contain unique drill figures identifying backdrill locations and should not be mixed with standard drill locations

- Fabrication notes should indicate backdrill side, backdrill depth identifying which layer is to remain electrically intact after backdrilling
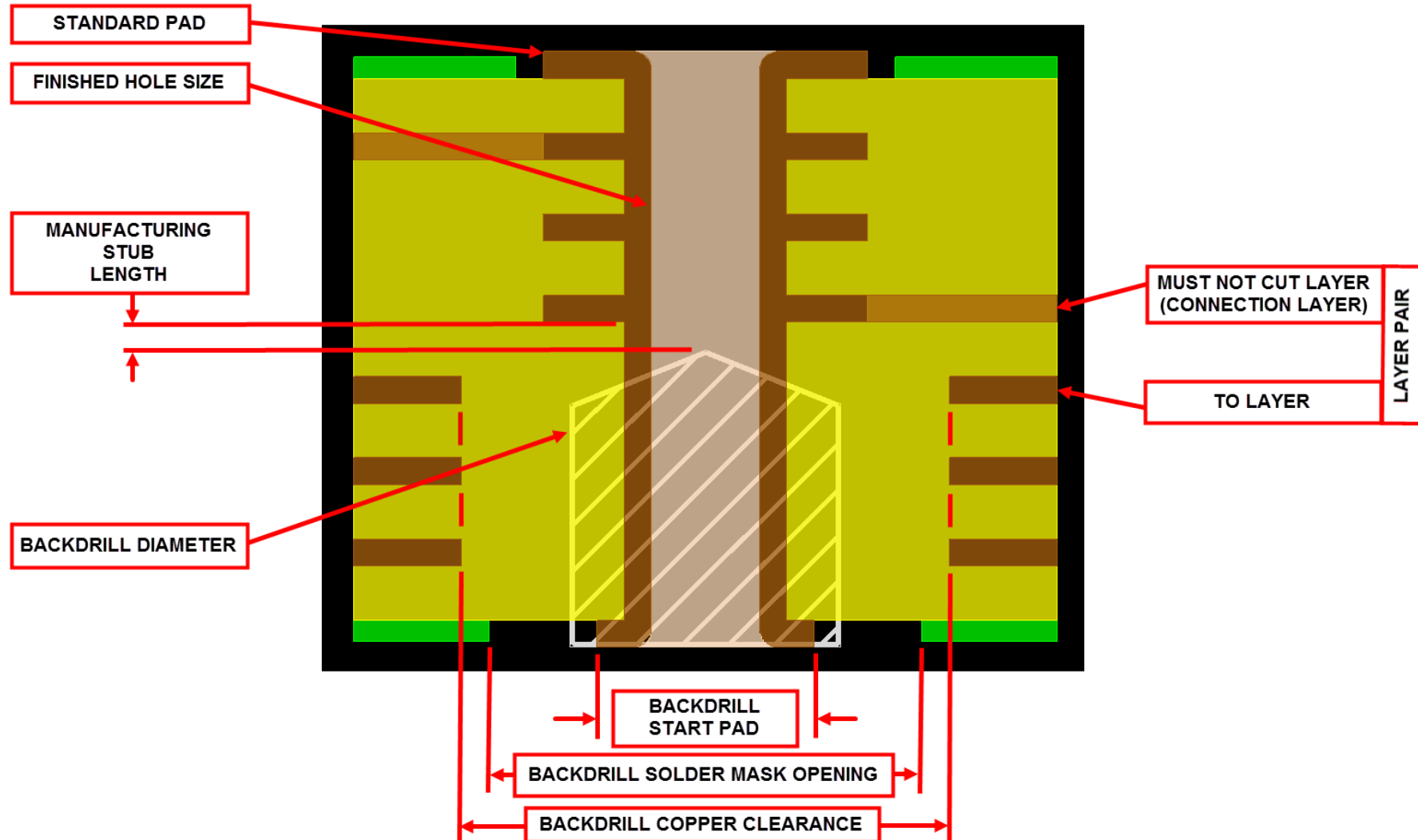
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What Can Be Done to Minimize PTH Stubs?

Backdrilling away the stub – Fabrication process

- Tool the backdrill depth to terminate as close to the target layer as their process capability will allow (Manufacturing stub length)

- Need to take into account distances between dielectric layers to ensure it is not greater than minimum manufacturing stub length
  - Cut layer may need to be shifted to avoid a risk of cutting into the must not cut layer

- Suppress unconnected pad (non-functional pads) in the path of the backdrill to reduce copper drilling

- Verify that all pad sizes have been adjusted and clearance is maintained in the path of the backdrill

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Typical Backdrill Location
Design modifications to support backdrill

STANDARD PAD

FINISHED HOLE SIZE

MANUFACTURING STUB LENGTH

BACKDRILL DIAMETER

MUST NOT CUT LAYER (CONNECTION LAYER)

TO LAYER

LAYER PAIR

BACKDRILL START PAD

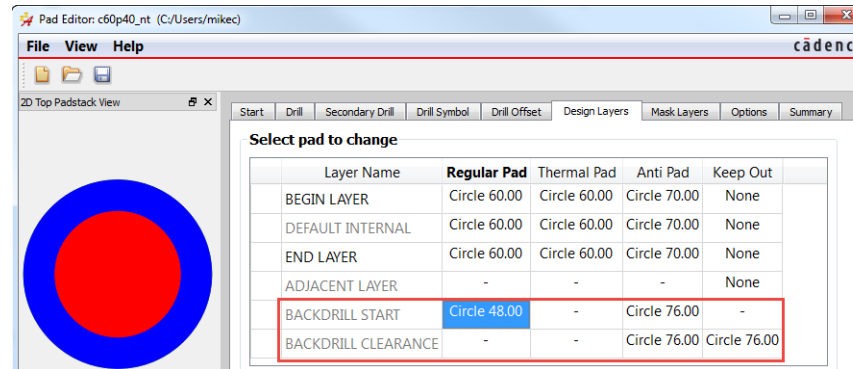BACKDRILL SOLDER MASK OPENING

BACKDRILL COPPER CLEARANCE

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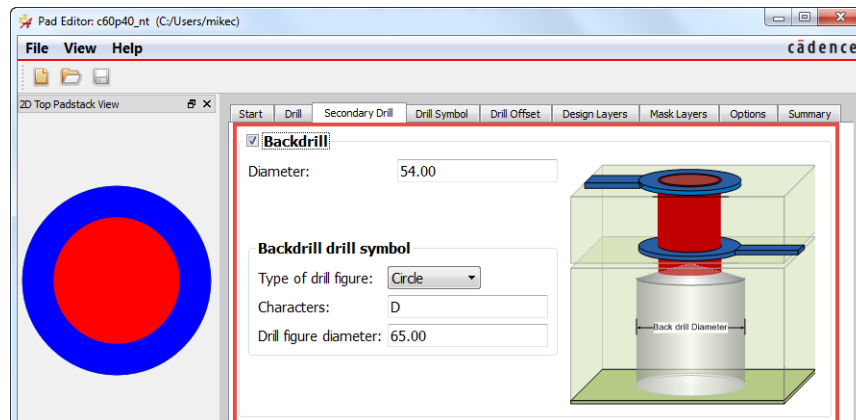# Enhanced Backdrill in Allegro Technology

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Enhanced Backdrill Support in Allegro Technology
Padstack library

- **Padstack the definition support backdrill data**
  - Backdrill size and special drill legend figure
  - Backdrill start layer copper pad and solder mask geometries
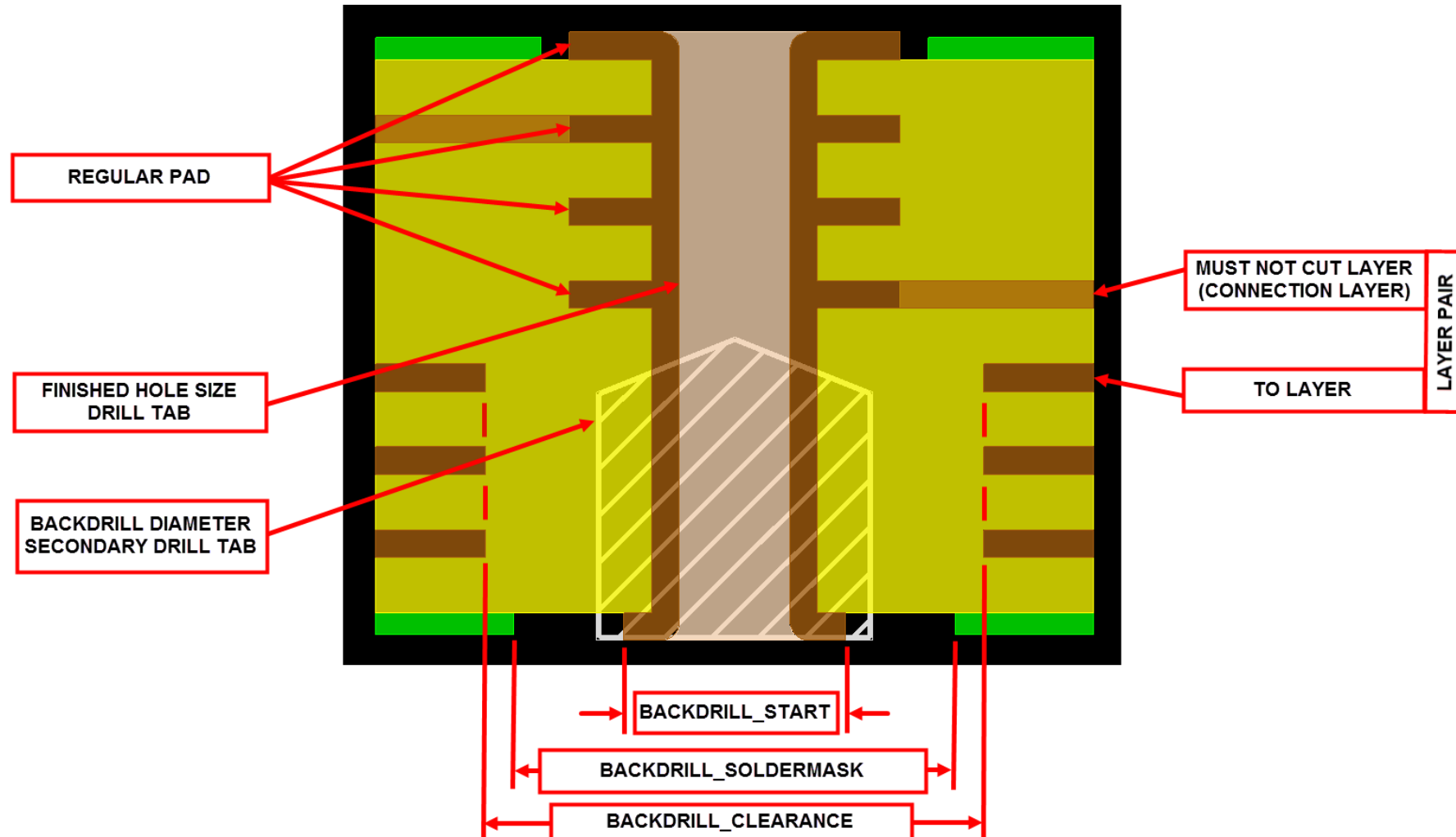 - Backdrill clearance anti-pad and route keepouts on backdrill layers

Fabrication vendor can assist you in determining the correct values for pad adjustments and clearances for backdrill

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Enhanced Backdrill Support in Allegro Technology
Padstack library

REGULAR PAD

MUST NOT CUT LAYER (CONNECTION LAYER)

TO LAYER

LAYER PAIR

FINISHED HOLE SIZE DRILL TAB

BACKDRILL DIAMETER SECONDARY DRILL TAB

BACKDRILL_START

BACKDRILL_SOLDERMASK

BACKDRILL_CLEARANCE

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Enhanced Backdrill Support in Allegro Technology
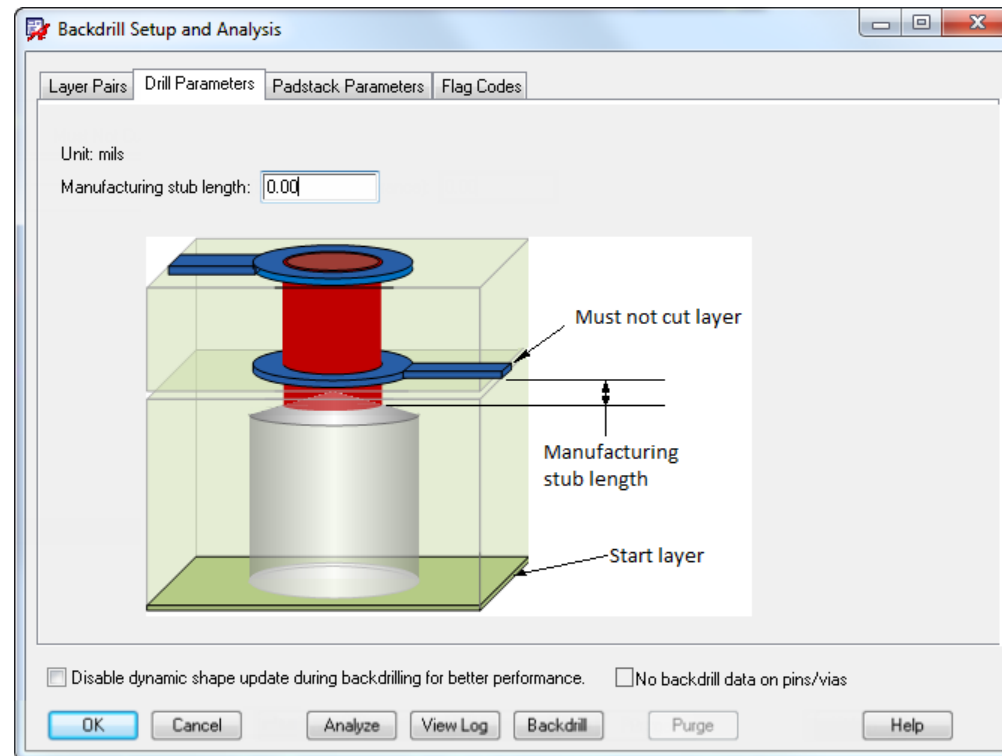## Backdrill layer setup and analysis

- Automatically create backdrill layer pairs based on design analysis (layer pair initialization)
  - Initialization: Deepest backdrill layer from top and bottom layers
  - Analysis: Minimized electrical stub length (treats stub as 0 – aggressive) or minimize layer pairs (based on uses stub value)
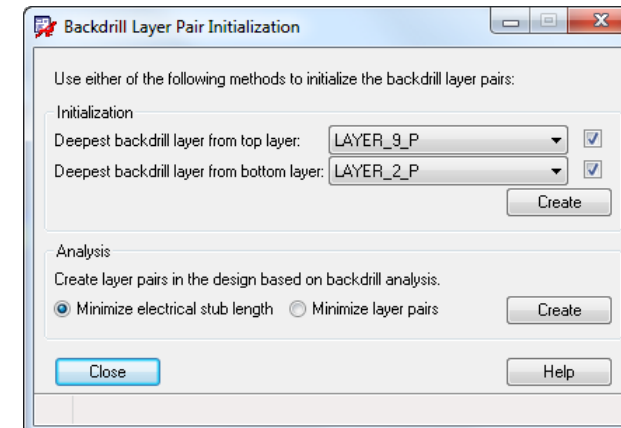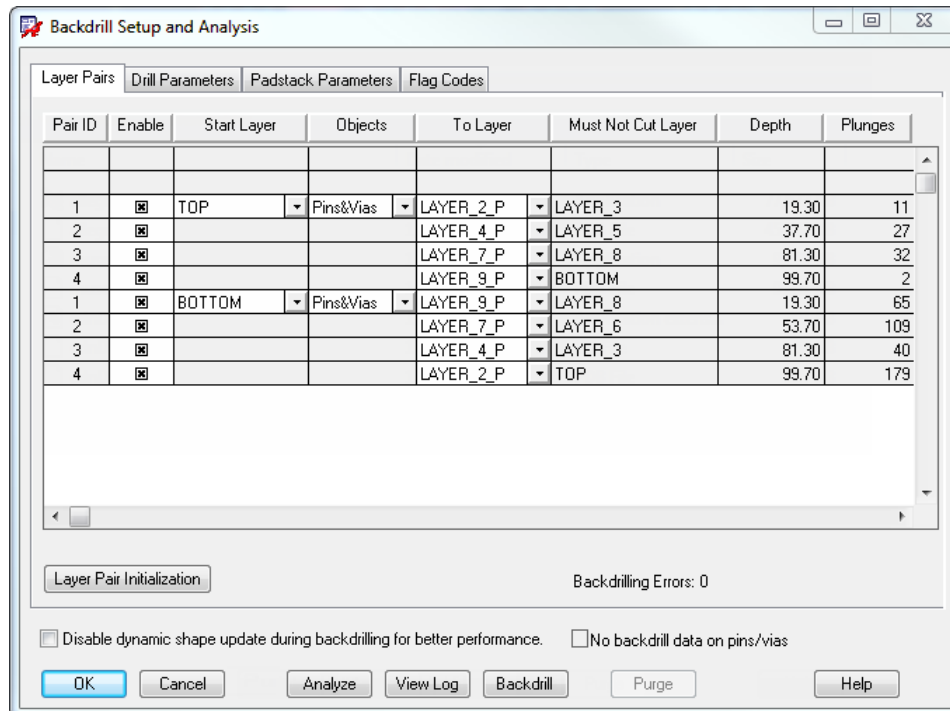
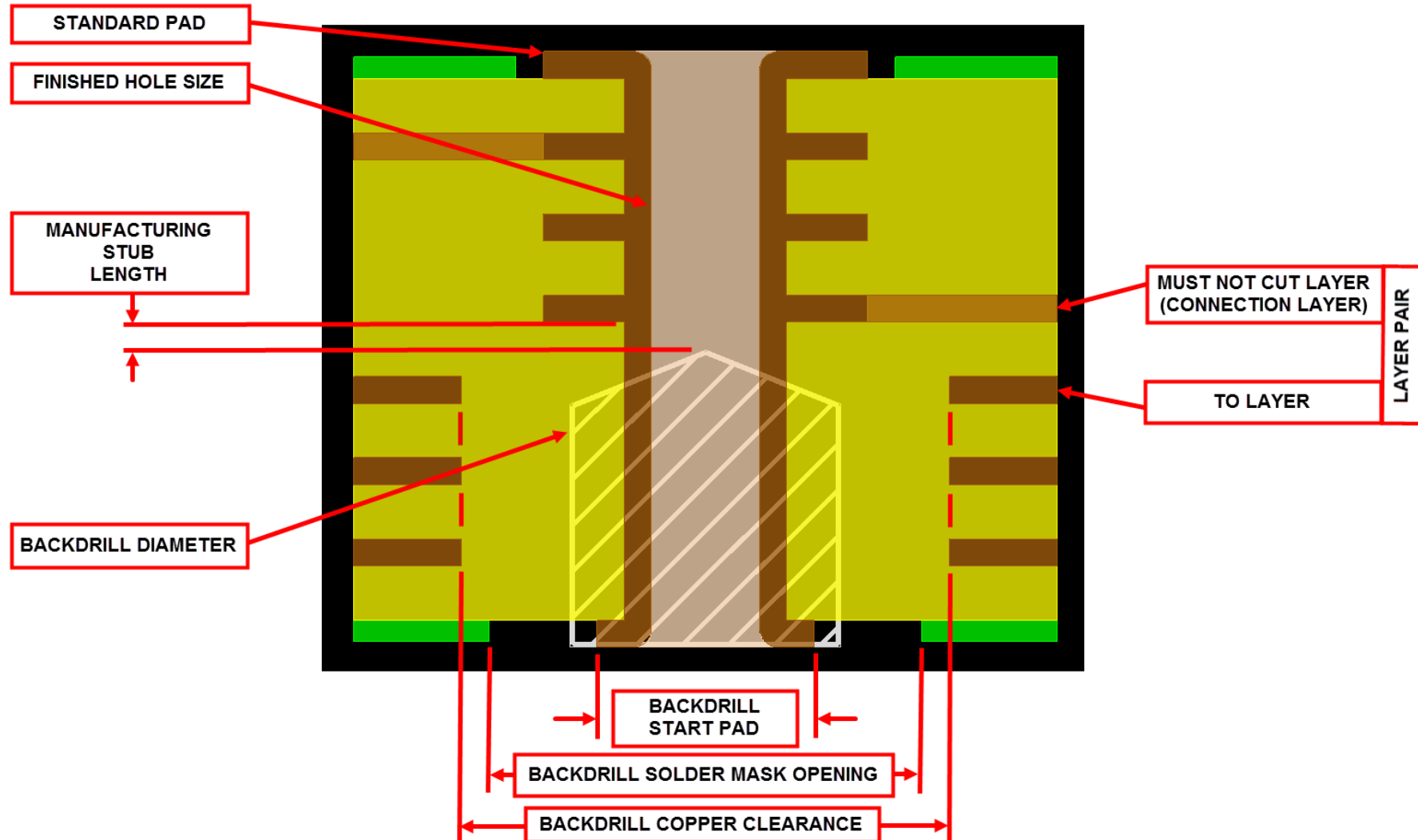# Enhanced Backdrill Support in Allegro Technology
Backdrill layer setup and analysis

- Manufacturing stub length – Remaining stub length after backdrill
  - Remaining manufacturing stub length measured down from the *must not cut layer*, which acts as a target backdrill depth into the dielectric
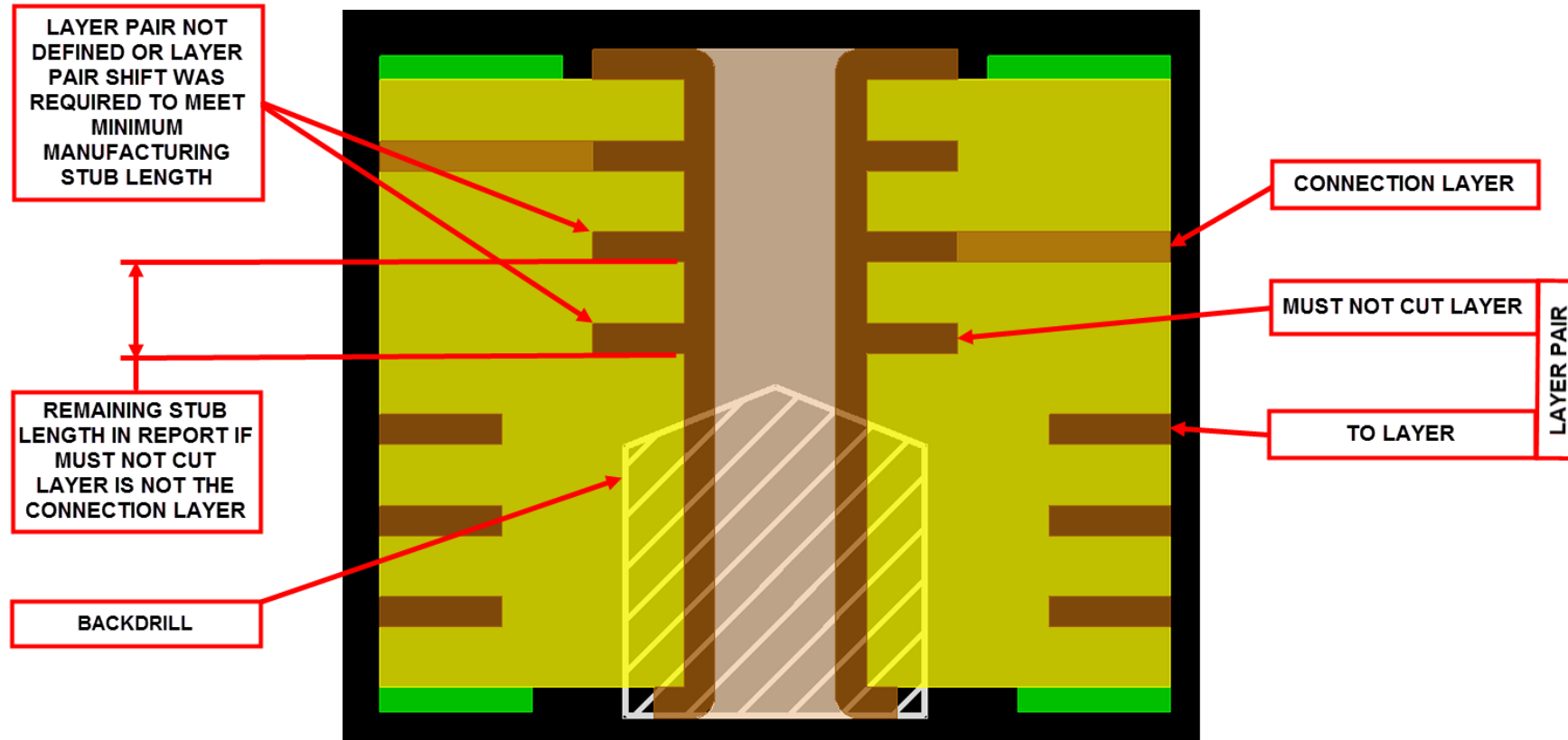
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Enhanced Backdrill Support in Allegro Technology
Backdrill layer setup and analysis

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Enhanced Backdrill Support in Allegro Technology
Backdrill layer setup and analysis

LAYER PAIR NOT DEFINED OR LAYER PAIR SHIFT WAS REQUIRED TO MEET MINIMUM MANUFACTURING STUB LENGTH

REMAINING STUB LENGTH IN REPORT IF MUST NOT CUT LAYER IS NOT THE CONNECTION LAYER

BACKDRILL

CONNECTION LAYER

MUST NOT CUT LAYER

TO LAYER

LAYER PAIR

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Enhanced Backdrill Support in Allegro Technology
Backdrill layer setup and analysis

- Backdrill data can be defined in padstacks at the library level

- Padstacks without backdrill data is updated using criteria under padstack parameters tab, all other padstacks remain unchanged

Fabrication vendor can assist you in determining the correct values for pad adjustments and clearances for backdrill

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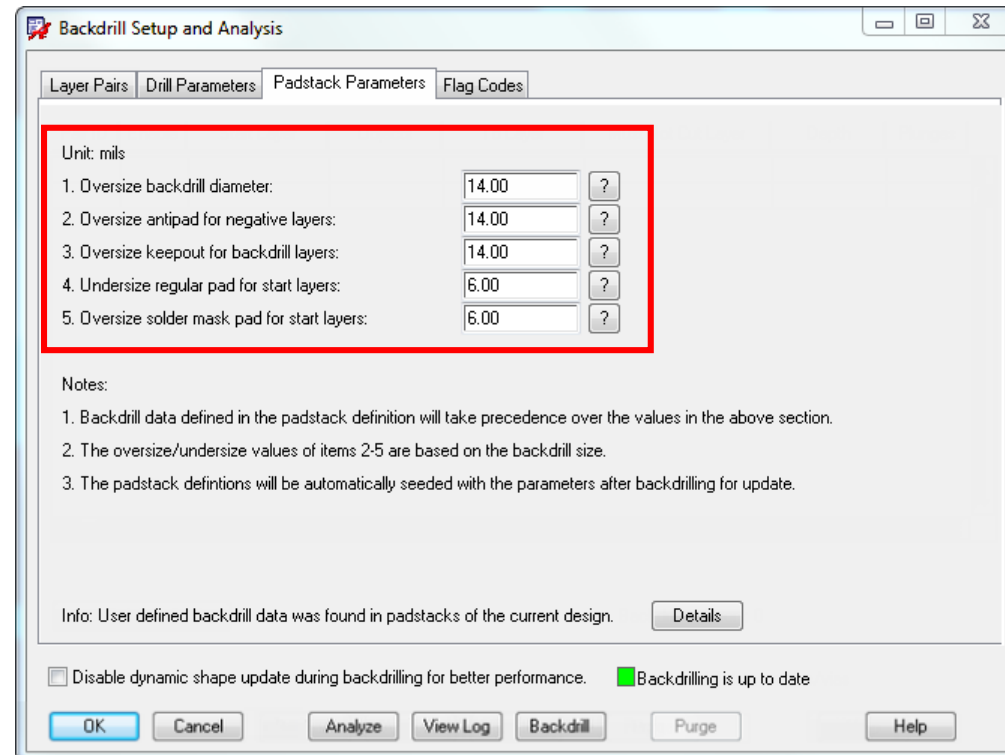
Enhanced Backdrill Support in Allegro Technology
Canvas display and route keepouts

- Backdrill locations clearly identified with special drill labels and hollow circle showing the backdrill diameter

- Route keepouts automatically generated based on clearance defined in padstack

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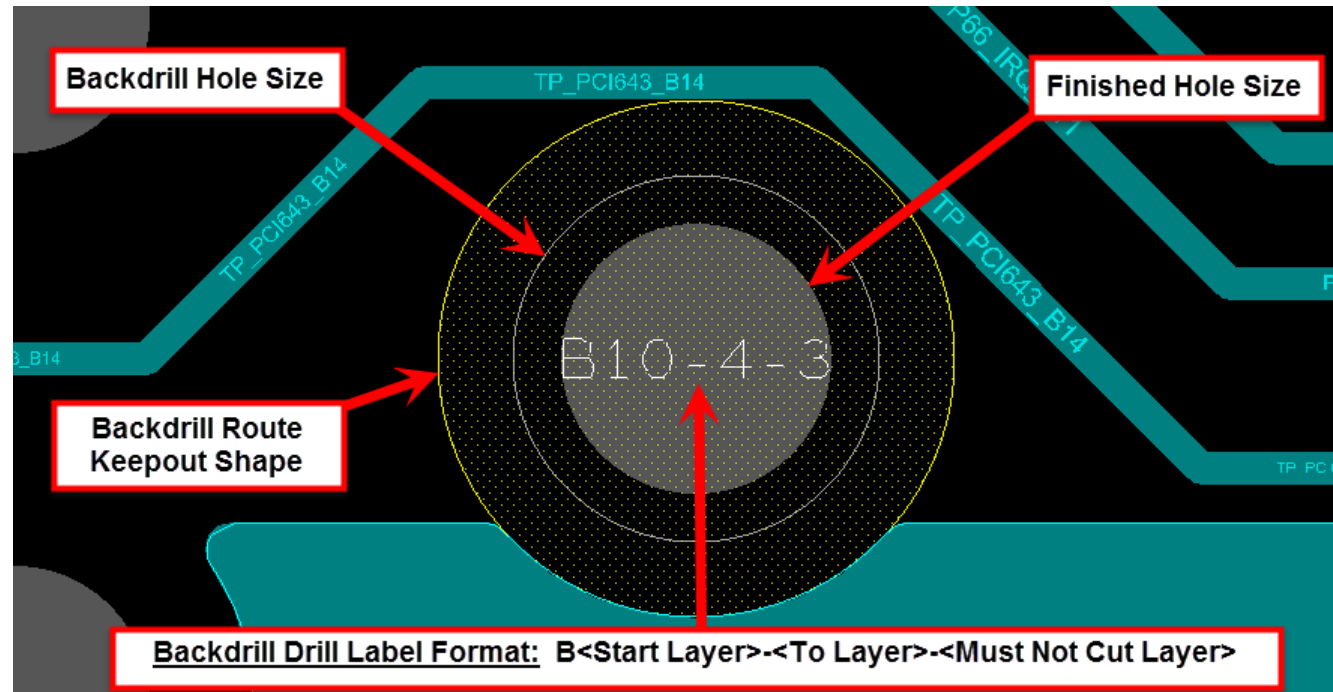
Enhanced Backdrill Support in Allegro Technology
Backdrill drill legends

- Actual backdrill size reported in drill legends based on backdrill data in padstack

- No longer necessary for fabrication vendor to adjust based on PTH

- Legend also reports the *must not cut layer*, depth, and manufacturing stub

```
;LEADER: 12
;HEADER:
;CODE  : ASCII
;FILE  : cadence_design-bd-10-9.drl for backdrilling ... from layer BOTTOM to layer LAYER_9_P
;DESIGN: cadence_design.brd
;MUST-NOT-CUT-LAYER = LAYER_8,  MAX_DRILL_DEPTH = 19.30 MILS,  MFG_STUB_LENGTH = 0.00 MILS
;    BackdrillSize 1. = 28.000000 Tolerance = +0.000000/-0.000000 NON_PLATED MILS Quantity = 5
;    BackdrillSize 2. = 52.000000 Tolerance = +0.000000/-0.000000 NON_PLATED MILS Quantity = 48
;    BackdrillSize 3. = 54.000000 Tolerance = +0.000000/-0.000000 NON_PLATED MILS Quantity = 41
%
G90
X0196600Y0063000
X0191600Y0058000
X0181600Y0053000
X0191800Y0052800
X0181600Y0047800
M00
X0364000Y0418000
X0344000Y0308000
```

BACKDRILL: BOTTOM to LAYER_9_P					
ALL UNITS ARE IN MILS					
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
Ⓐ	28.0	LAYER_8	19.3	-	5
Ⓑ	52.0	LAYER_8	19.3	-	48
Ⓒ	54.0	LAYER_8	19.3	-	41

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE
            SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

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Enhanced Backdrill Support in Allegro Technology
Cross-section detail with backdrill spans
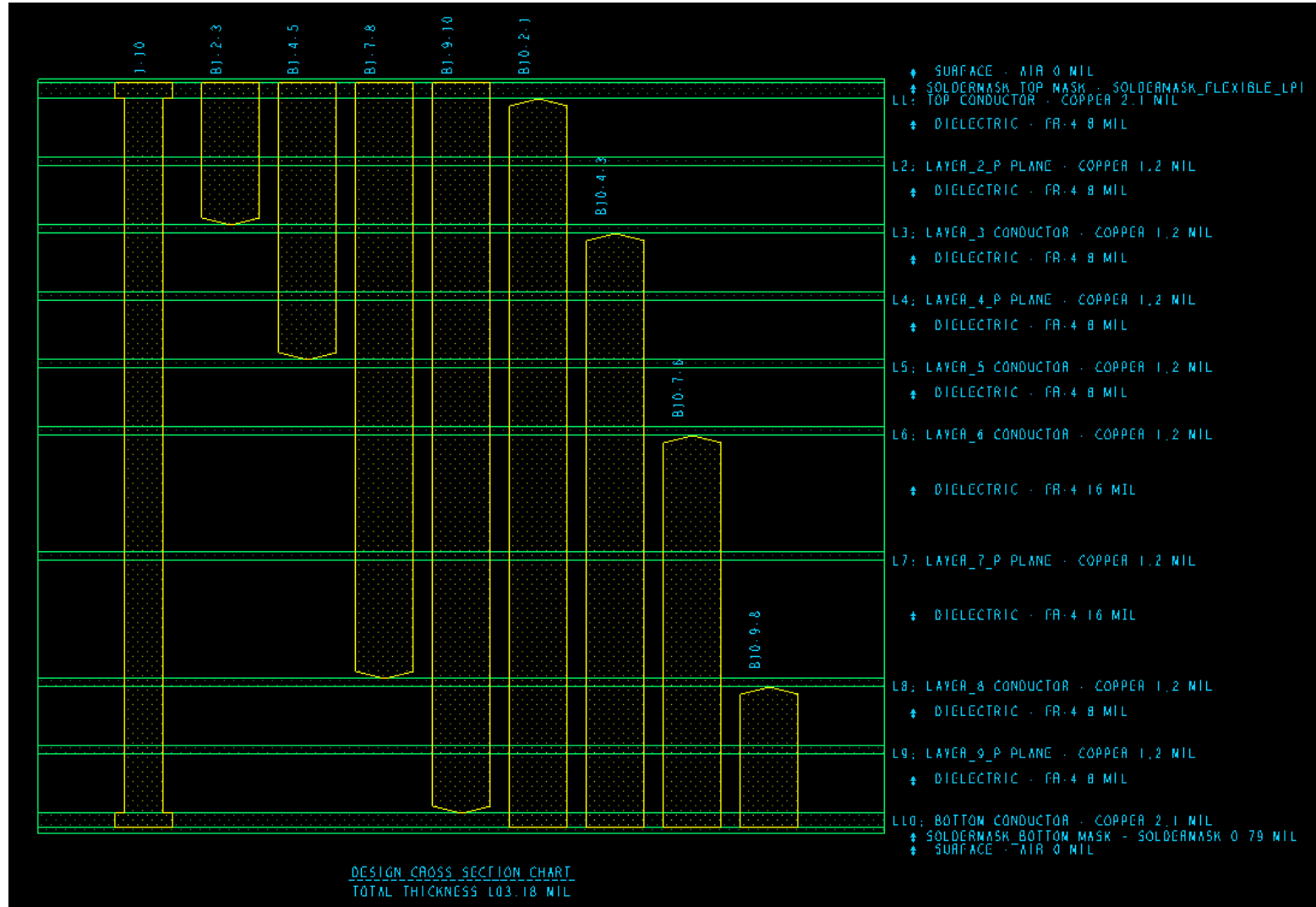
Enhanced Backdrill Support in Allegro Technology
Test points and manufacturing output

- ## Test prep backdrill awareness
  - Adding test point manually or automatically will respect existing backdrill sites and will not update padstack or attempt to mark them as test point
  - Existing test point sites will be skipped during backdrilling and marked with a T figure flag code indicating they are potential backdrill candidates that were not backdrilled

- ## IPC-D-356
  - Output will include any backdrill data with an option to ignore the backdrill data during output

- ## IPC-2581
  - Revised to included all backdrill data in export for complete fabrication package

- ## NC drill data
  - Automatically generates all required backdrill data files, separated by depth and PCB side

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Managing Backdrilling from Library until Handoff to Manufacturing
Session in review

- Brief overview of some signal integrity reasons why backdrill may be required on your high-speed designs

- Provided alternatives to introducing the backdrill process and understanding its limitations

- Discussed design practices in support of backdrilling and developing a complete data package to streamline the release to manufacturing

- Reviewed enhanced backdrill functionality in Allegro PCB Designer 17.2-2016 to support backdrilling

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YOUR FEEDBACK IS IMPORTANT! DON'T FORGET YOUR SPEAKER EVALUATION.

PLEASE REMEMBER TO RETURN THE EVALUATION FORMS TO THE PRESENTER, TO THE REGISTRATION DESK OR TO THE DROP BOX IN THE LOBBY.

THANK YOU,

PCB WEST SHOW MANAGEMENT