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How a Team-Based Approach to PCB Power Integrity Analysis Yields Better Results

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Assuring power integrity of a PCB requires the contributions of multiple design team members. Traditionally, such an effort has involved a time-consuming process for a back-end-focused expert at the front end of a design. This paper examines a collaborative team-based approach that makes more efficient use of resources and provides more impact at critical points in the design process.

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Introduction

Consider the proverb, "It takes a village to raise a child." Similarly, multiple design team members participate in assuring PCB power integrity (PI) as a design moves from the early concept phase to becoming a mature product. On the front end, there's the electrical design engineer who is responsible for the schematic. On the back end, the layout designer handles physical implementation. Typically, a PI analysis expert is responsible for overall PCB PI and steps in early on to guide the contributions of others. How quickly a team can assure PCB PI relates to the effectiveness of that team.

In this paper, we will take a look at currently popular analysis approaches to PCB PI. We will also introduce a team-based approach to PCB PI that yields advantages in resource utilization and analysis results.

Common Power Integrity Analysis Methods

There are two distinct facets of PCB PI: DC and AC. DC PI guarantees that adequate DC voltage is delivered to all active devices mounted on a PCB (often using IR drop analysis). This helps to assure that constraints are met for current density in planar metals and total current of vias and also that temperature constraints are met for metals and substrate materials. AC PI concerns the delivery of AC current to mounted devices to support their switching activity while meeting constraints for transient noise voltage levels within the power delivery network (PDN). The PDN noise margin (variation from nominal voltage) is a sum of both DC IR drop and AC noise.

DC PI is governed by resistance of the metals and the current pulled from the PDN by each mounted device. Engineers have, for many years, applied resistive network models for approximate DC PI analysis. Now that computer speeds are faster and larger addressable memory is available, the industry is seeing much more application of layout-driven detailed numerical analysis techniques for DC PI. Approximation occurs less, accuracy is higher, and automation of

whole-design analysis and post-processing results are commonly available commercially. In fact, DC PI analysis for PCB designs has become a "signoff" requirement for many OEMs. See Figure 1 (left) for typical results for current density.

Since metal conductivity is temperature-dependent, DC IR drop is a nonlinear analysis. IR drop results can vary by more than 20% when temperature effects are considered, according to case studies for high-power designs. There is, however, a way to accurately characterize PCB IR drop while assuring that the PDN noise margin isn't wasted. Using a DC analysis tool that provides capabilities such as electrical/thermal co-simulation, perform a linear electrical analysis at ambient temperature; take the resulting power loss and apply it to perform a linear thermal analysis. Then, perform another linear electrical analysis with consideration of the localized temperature-dependent conductivity. This process converges in just a few iterations to yield a desired result. See Figure 1 for an illustration of this solution, as implemented in the Cadence® Sigrity™ PowerDC™ DC analysis tool.

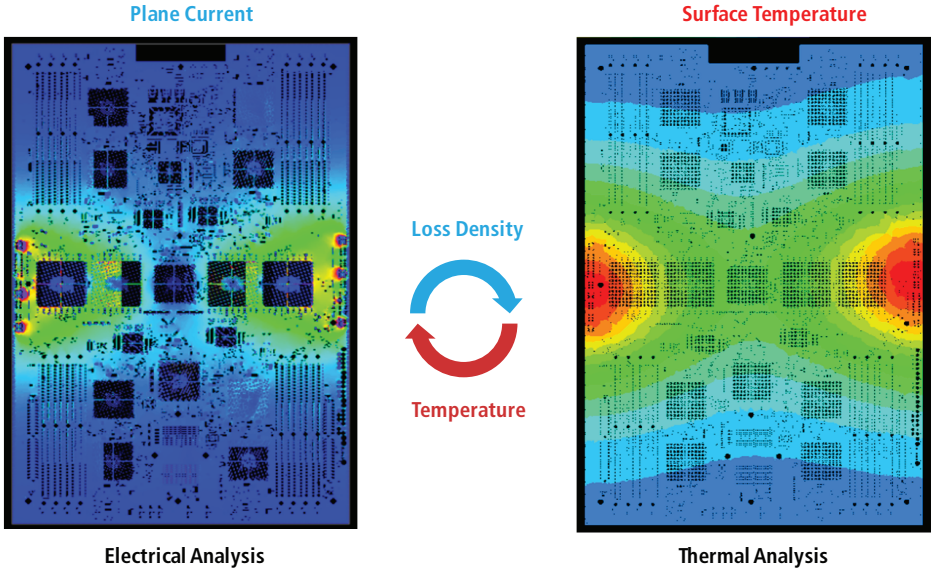

Figure 1: Current density (left) and temperature distribution (right) for a PCB design due to DC power delivery as two linear solutions are iteratively linked to address nonlinear electro-thermal analysis.

AC PI is governed by voltage regulator modules, loop inductances, decoupling capacitors (decaps), and plane capacitance. AC PI effects tend to be global in nature due to plane resonances, plane-to-plane coupling, and shared reference planes. As such, this calls for full-board analysis, as well as more resource-intensive analysis algorithms. A hybrid of circuit theory and electromagnetic (EM) analyses is the most commonly applied AC PI analysis for PCBs. This type of analysis is available in the frequency domain to extract S-parameters, using a tool such as the Cadence Sigrity PowerSI® frequency-domain electrical analysis solution. It's also available in the time domain to directly generate transient waveforms, using a tool such as the Cadence Sigrity SPEED2000™ time-domain analysis solution. With the proper tools, an engineer can, in tens of minutes, accurately characterize the PDN behavior of even the largest and most complex PCBs from DC to multi-gigahertz using single- to low double-digit gigabytes of memory.

Transient PI analysis may seem attractive because it directly yields noise waveforms; however, in reality, it is less commonly applied than frequency-domain impedance analysis. "Target impedance" profiles are applied as PI constraints. Lower impedance corresponds to lower transient noise. Without direct vendor specification, reasonable target impedance may be estimated based on device specifications for voltage ripple and AC switching current. See Figure 2 for a comparison of frequency-domain and time-domain results. In this comparison, the Cadence Sigrity OptimizePI™ tool was used to significantly reduce an impedance peak near 800MHz by applying an alternate set of decaps to mount for a DIMM module. This solution reduced peak-to-peak PDN noise for the optimized design by 12% and the component and manufacturing cost of the decap implementation by 21%.

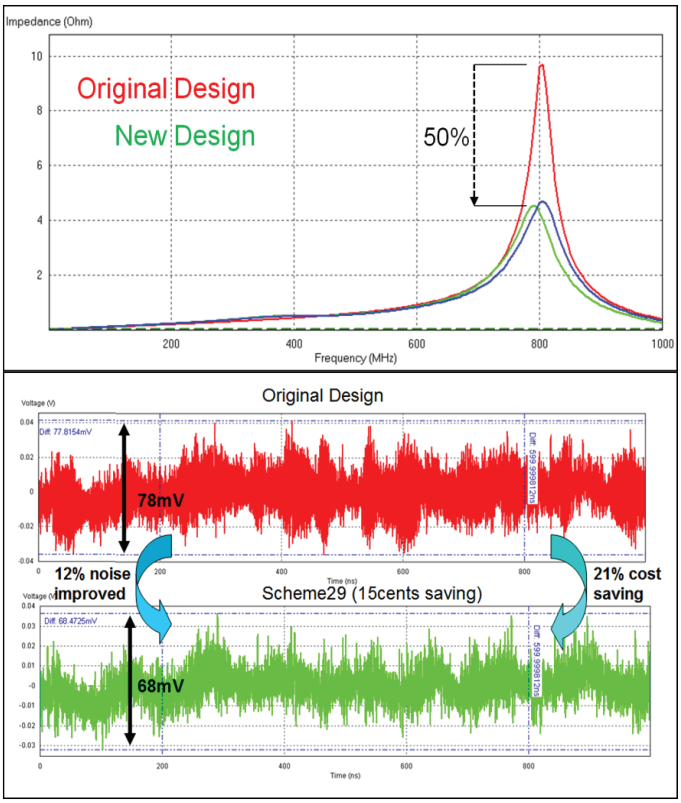

Figure 2: Impedance profile and transient PDN noise of a DIMM before and after the decap implementation was optimized.

Applying a Team-Based Approach to Power Integrity Analysis

Traditionally, PI experts have performed pre-layout decap selections and initial IR drop analyses. This is a substantial time investment at the front end of a design for a back-end-focused expert. By applying a more collaborative approach, a design team can make better use of its resources and expertise, and generate more impactful results. A team can set up simple analyses that yield actionable results and that can be performed by other members of the PI team. This PCB PI team ideally consists of three key members: design engineer, layout designer, and PI analysis expert, as shown in Figure 3.

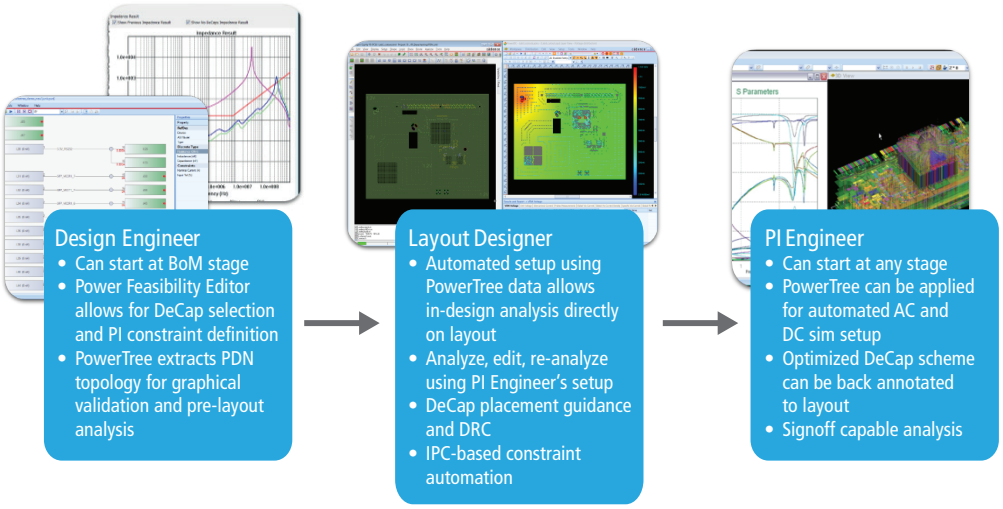

Figure 3: Roles and responsibilities of the PCB PI design team.

There is now a tool available on the market that supports team-based PCB PI analysis. The Cadence Allegro® Sigrity PI solution is the industry's first front-to-back, constraint-based PI approach for PCB and IC package designs. This tool differs from other solutions in the way that it accesses existing analysis algorithms and how the analysis results are applied. In addition, the tool also provides PI-focused infrastructure support of non-analysis tasks. As a result, design engineers and layout designers can contribute earlier and more effectively to PCB PI. The DC and AC PI analysis capabilities described in the previous section are available in the associated Power Integrity Signoff and Optimization Option.

The complexity of today's PDN means that it often spans a significant number of pages in the schematic and encompasses a dozen or more power rails. As a result, many design teams painstakingly regenerate the PDN or portions of it in some other format such as a spreadsheet to better visualize the PDN and to assure all of the unnamed or arbitrarily named nets, like those connecting filter circuitry, are included in any layout-based simulation downstream. While these methods offer some advantages in the area of visualization, there is downside in terms of time and effort and there is limited data reuse or ability to actually aid in simulation setup.

Figure 4 shows a topology of the PDN generated with the Cadence Allegro PowerTree™ tool. This utility can be employed by any engineer in the design team and uses just the netlist information available in the schematic. As an integrated piece of Allegro Sigrity PI, the PowerTree technology goes well beyond the simple task of visual validation of the PDN.

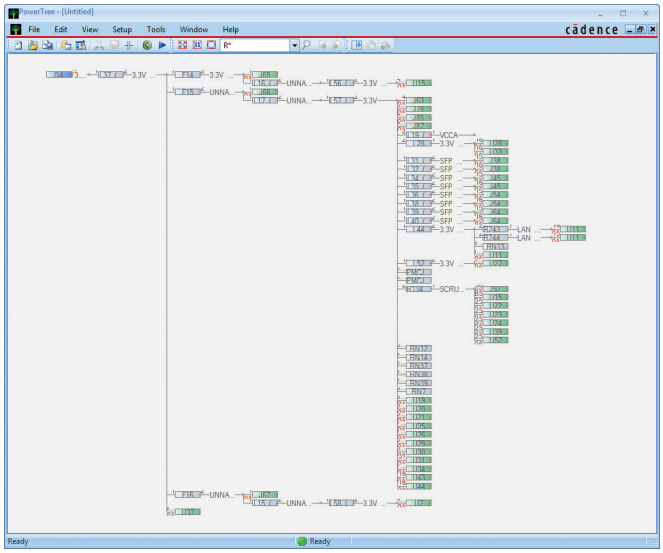

Figure 4: PDN topology generated in the PowerTree tool

The PowerTree tool can generate a tree very easily, drastically reducing time and effort over manual visualization methods. Additionally, trees can be loaded and compared in a side-by-side configuration with graphical indication of differences as a way to track schematic changes. Further component data can be entered manually or automated with a one-time assignment from Analysis Model Manager (AMM) libraries and all tree data can be reused as needed. Simulation of a tree with only component data is another way of validating the PDN prior to layout for early power estimation. Simulations at this stage can identify potential problems with device selection or models well before these issues would be identified using traditional layout-based PI analysis. Further design cycle time can be saved by applying completed trees in either the Sigrity PowerDC tool or the Sigrity OptimizePI tool. This process of applying a tree effectively automates all of the required PDN simulation setup, and allows push-button analysis.

PCB design engineers are responsible for front-end tasks. They must generate an initial bill of materials (BoM) to set in motion cost feasibility studies and assure electrical design intent by generating circuit schematics. They typically work independently of DC PI concerns. However, to support AC PI, design engineers must add decaps and include them in the BoM and the schematic. Some device vendors provide datasheet guidance for decap selection (type and/or quantity), but many do not. Even with datasheet guidance, it is tedious for design engineers to

assemble and interpret the specifications for each device, instantiate all the unique components, assure they appear logically in the schematic, etc. No mechanism has existed for physical placement guidance to be communicated for back-end application.

With constraint-based design methods, engineers gain a uniform interface for design-intent information and for automating a broad class of tasks across front-to-back flows. PI [electrical] constraint sets (PI CSets) have been added to save all component-level PI information. Design engineers may apply PI CSets to quickly and completely define PI design intent for all mounted components. PI CSets also automate instantiation of components and inclusion in the BoM.

Figure 5 provides an example of a PI CSet in Allegro Sigrity PI. PI CSets contain information for each power rail, including decap component names, quantity of each component, package type, and physical placement guidance.

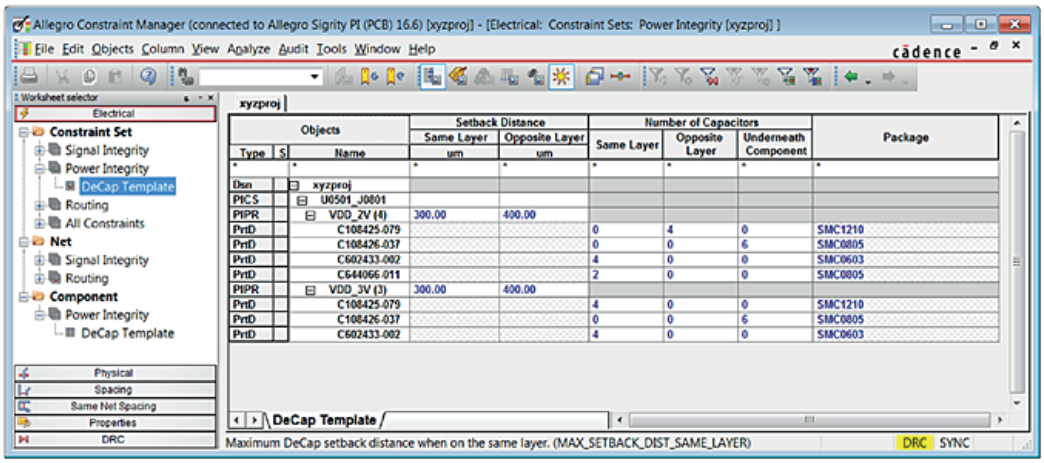

Figure 5: PI constraint set contents viewed from the Constraint Manager

PI Cset creation is automated by the tool's Power Feasibility Editor, which provides a mechanism to enter datasheet decap selection and physical placement guidance. Figure 6 shows a view of the tool's Power Feasibility Editor. In addition to placement guidance, a PI CSet communicates to the layout designer component and power rail association for decaps, helping the designer perform more reliable placement.

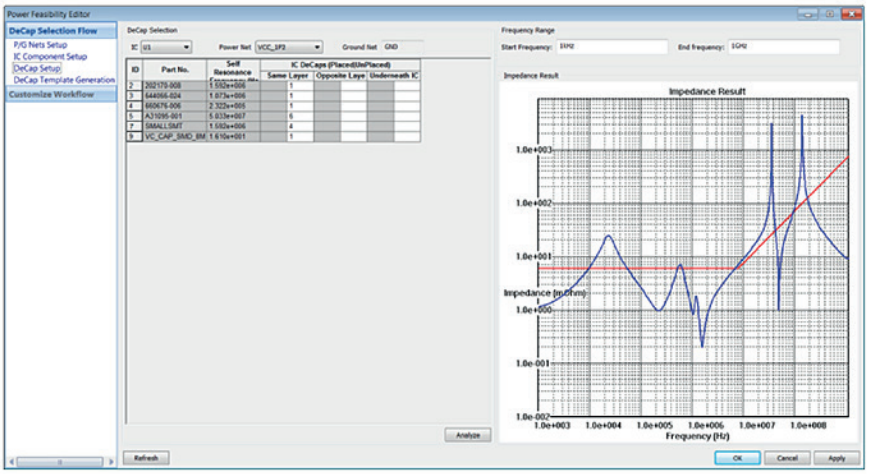

Figure 6: Single-point analysis results in the Power Feasibility Editor

The Power Feasibility Editor also provides access to approximate and detailed pre-layout analysis for selection and placement of decaps. High-level specifications are made to generate target impedance profiles when device vendors do not provide them. An approximate PI analysis called "single-point" is provided for interactive decap selection. For more detailed pre-layout, the tool provides access to the data in the Sigrity OptimizePI tool. The engineer simply clicks a button within the Power Feasibility Editor to generate PI CSets.

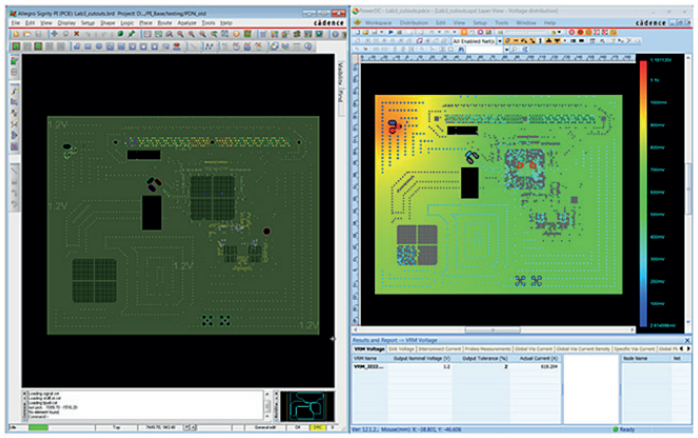

Figure 7: Split-screen view of layout (left) and IR drop analysis results (right)

Unlike design engineers, layout designers are concerned with DC PI issues. Layout designers control metal shapes and vias and these, in turn, control PI behaviors for DC IR drop and current flow. Layout designers can intuitively understand and act upon analysis results for these DC PI effects. Allegro Sigrity PI provides access within the layout environment to the setup and results display for DC IR drop and current constraint analyses. DC analysis is fast, though not conducted in real time in order to enable dynamic updating of analysis results as layout updates are made.

The tool provides several use model options for the layout designer. These use-model options all offer superior integration to the "over-the-wall" approach where a design is passed to the PI expert for analysis and, in turn, some documented form of design changes are tossed back. This antiquated process often involves wait time for each to complete a task before another analyze-edit cycle can be completed. With Allegro Sigrity PI, the layout designer is empowered to leverage setup data in the form of a PowerTree topology or to point directly to the same setup workspace utilized by the PI expert. Prior to this data being available, constraints can be automatically derived from the integrated IPC calculations and a user-provided acceptable temperature rise. Layout designers also have the option of importing DRC markers from the PI analysis or cross-probing from the PI analysis report to violations in the design. Regardless of the selected use model for setup or feedback, the layout designer can independently edit and re-analyze as many times as needed without impacting the PI expert.

The last use-model option is a split-screen view, as shown in Figure 7, to support a fixed view of analysis results as layout designers dynamically make updates to address IR drop or current constraint issues. The two views are synchronized for operations that affect the display, such as layer changes, zoom, and pan. Layout designers can apply this split-screen view of DC analysis results as they craft an initial layout, before the PI analysis expert gets involved. As a more effective method to communicate where PI issues exist in the design, the split-screen view can also be applied with detailed analysis results performed separately by PI analysis experts. In fact, to more quickly verify improved PI performance, the layout designer can launch the same detailed analysis performed by the PI analyst.

Layout designers strongly influence AC PI success with their placement of decaps. Decaps placed close to a device generally benefit PI, but restrict routing channels due to decap mounting vias. Decaps placed too far from a device will be ineffective at providing switching current to the device and will negatively affect PI. Present design methods do not typically provide decap placement guidance, including information as simple as which device is associated with a decap. By conveying design intent, previously described PI CSets enable more effective placement of decaps by layout designers. The associated device and power rail and placement guidance are all specified in the PI CSet.

A decap placement mode is implemented to support layout designers, as shown in Figure 8. Simply select a mounted component and a power rail, and then cycle through a point-and-click placement process. The selected device is highlighted and three optional visual placement guidance displays are available: device to decap distance for top layer, device to decap distance for bottom layer, and decap effective radius. The first two are defined in the PI CSet and are conceptually familiar. The decap effective radius is the maximum distance at which the decap will be maximally effective. It is a function of the stack-up and decap mounting parasitics as well as the decap value and its intrinsic parasitics. It is dynamically computed as the cursor moves due to local availability of metal shapes on the associated power and ground layers.

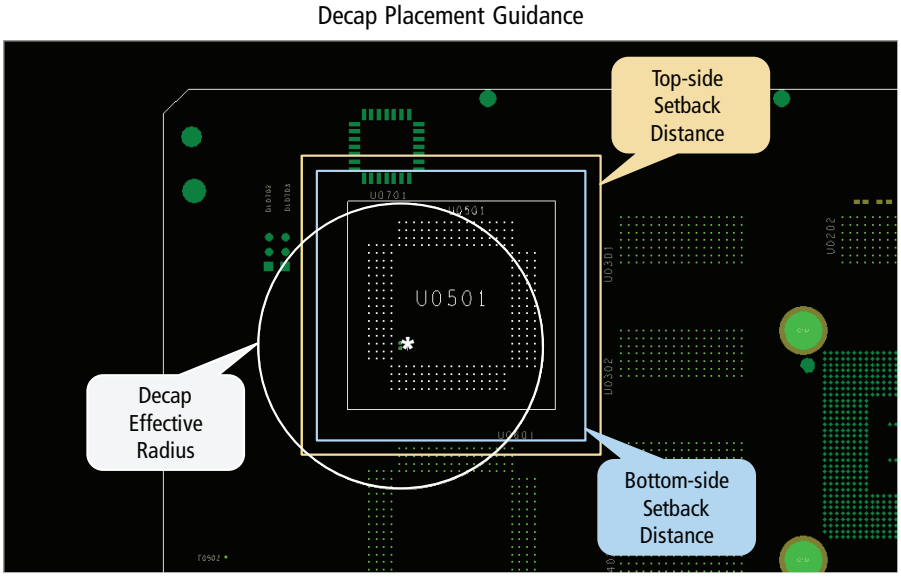

Figure 8: Layout view during decap placement for device U0501 with top (yellow) and bottom (blue) setback distances and decap effective radius (white circle) displayed

Once decap placement is complete, there is still some AC post-layout verification that can be performed. Vendors today are more often supplying target impedance profiles for specific devices. These same impedance profiles can be captured as AMM models and applied during PowerTree capture. Layout designers can then run a simple analysis in the Sigrity OptimizePI tool to verify these impedance profiles, leveraging the setup captured with the PowerTree tool and making any decap placement adjustments. If a full optimization is run by the PI analysis expert, the Sigrity OptimizePI tool can back annotate any decap changes contained in the selected scheme to the layout. This automated process assures that all changes can be implemented in the layout and conveyed back to the design engineer to enable automated update of the schematic, BoM, and PI CSets.

Summary

While current PCB PI analysis tools are continuing to serve the design community well, they are even more effective when combined with a front-to-back, constraint-based approach. Under this type of methodology, each design team member can more efficiently accomplish his or her individual tasks and communicate design intent information to colleagues for increased efficiency of the overall PCB design flow. This approach provides access to actionable analysis results where they are most impactful. It also leverages earlier defined analysis setup information for the PI expert, and eases communication of design changes from his or her back-end role to front-end colleagues.

For Further Information

To learn more about the Cadence Allegro Sigrity PI solution, visit www.cadence.com/go/allegro-sigrity-pi-base.

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