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Save Time and Minimize Errors by Automating Co-Design and Co-Analysis of Chips, PCBs, and Packages

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Given the complexity of today's chips, packages, and PCBs, designing each in isolation is no longer judicious. Cross-domain co-design and co-analysis are key to ensuring optimal performance, cost reduction, and faster time to market. Such capabilities are provided by the Cadence® Virtuoso® System Design Platform, which integrates IC design—including multiple heterogeneous die—into the Allegro® and Sigrity™ packaging and PCB design domains. This technology provides a seamless and automated design flow between IC, package, and PCB design that can accelerate the overall design process and minimize errors.

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Introduction

The increasing complexity in today's IC packages and PCBs can have a huge impact on the performance and functionality of the IC. In addition, higher densities, lower power, and tighter cost margins with a shorter time to market all need to be taken into account when designing an IC along with its package and maybe even the PCB. It's no wonder that chip/package/PCB co-design and co-analysis has now become the norm. However, there hasn't been an automated or efficient process for designing concurrently across all three domains. What designers need is a formal and automated co-design flow to help minimize the potential for human error. This paper outlines a new methodology that provides such a solution.

How IC Packaging and PCB Have Evolved

Traditionally, IC packaging has provided some modest, yet critical, functions: protecting the chip, redistributing I/Os to pitches more suitable for the PCB, and making it easier to test the chip (compared to a wafer) before implementation at the system level. As the electronics industry looks to continue to extend Moore's Law, IC packaging seems poised to take on a larger, more significant role.

As Moore's Law seems to be nearing its end, many designers are looking to packaging as the ideal platform for today's "More than Moore" trend of heterogeneous design assembly. Multi-chip modules (MCMs) and system-in-package (SiP) design technologies have been used for decades to integrate multiple ICs from differing technologies and process nodes. It seems like the timing is perfect for multi-die packaging to really take off.

That said, new semiconductor technologies like through-silicon via (TSV) are making silicon interposers a more viable option for multi-die heterogeneous integration. And maybe the most exciting new packaging trend, fan-out wafer level packaging (FOWLP)—is this the platform of the future for heterogeneous integration? Only time will tell.

In addition, the PCBs that these devices sit on have much more complex form factors and flexible/bendable attributes, enabling a variety of small, lightweight products such as wearable, mobile, military, and medical devices.

To achieve optimal results, early planning, assembly, and optimization of the complete system made up of multiple ICs, targeting multiple-package technologies fitting into complex PCB form-factors is now mandatory for today's leading-edge products.

Displacing a Manual, Error-Prone Process

Traditionally, the flow between chip, package, and PCB has been a manual one, and therefore is time consuming and error prone, particularly in designs with thousands of pins. Designers have had to manually hook up pins on the package based on an electrical model of the IC. Different designers working on different parts of the system—the IC itself, the PCB, and the packaging—have typically designed with tools meant for each particular substrate. However, as we've noted, designing each part in isolation doesn't yield optimal results. An automated means to co-design and co-analyze across the different domains saves time and effort and results in higher performing, cost competitive systems.

Cadence provides such capabilities through its Virtuoso System Design Platform, which integrates IC design into the Allegro and Sigrity packaging/PCB design domains. The platform is ideal for designs that integrate multiple heterogeneous ICs, including RF, analog, and digital devices. Currently, the platform supports two primary flows: implementation and analysis.

Implementation Flow

In the implementation flow, the Virtuoso System Design Platform (shown in Figure 1) captures and manages system-/package-level devices and connectivity from the top level in the Virtuoso Schematic Editor. In other words, the package-/module-level design can be captured in the same environment many IC designers are already using today to create the schematic for their IC layout. This module-level schematic can be used to accurately perform layout vs. schematic (LVS) checking between the Virtuoso (IC) and Allegro (package/PCB) domains.

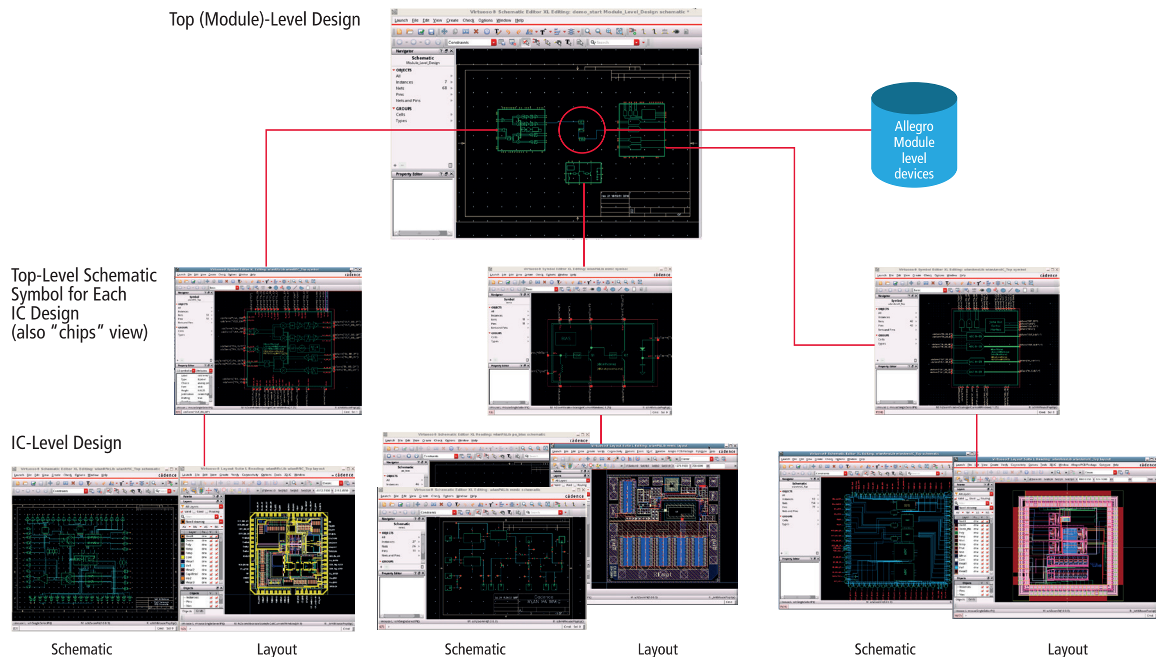

Figure 1: The Virtuoso System Design Platform automates co-design and co-analysis of ICs, packages, and PCBs

Historically, different schematic capture tools were used to support the cross-domain implementation process, but these tools have come with many limitations. Now, using this platform, designers can capture the module-level design from inside the Virtuoso environment, eliminating an often disjointed step in the handoff between IC and package design. The solution automatically creates schematic symbols for the module-level Virtuoso schematic, generating the correct hierarchy to support multiple pins with the same name. It also provides automated creation of library footprint symbols for the Allegro layout environment. Users can also apply shrink factor and scribe lane dimensions to create an accurate manufactured representation of the IC. After this view of the IC layout has been generated and the die abstract imported into Allegro layout, pin positions can be optimized for routing and/or wire bonding. These changes can used to automatically update the IC layout in the Virtuoso Layout Suite.

Analysis Flow

In the analysis flow, the Virtuoso System Design Platform imports system-level connectivity and layout parasitic data into the Virtuoso Schematic Editor for system-aware IC design. It provides intelligent n-port S-parameter models (see Figure 2) to streamline testbench-ready schematic creation (shown in Figure 3). Historically, Virtuoso users designing analog devices encountered a broken flow when they wanted to include system-level connectivity and parasitics data based on the layout. The platform allows users to stay in the Virtuoso Schematic Editor, point to data in either the Allegro or Sigrity environment, and use this data to automatically build the schematic with all of the PCB- and package-level connectivity and parasitic models based on package and PCB layout. As part of the analysis flow, the platform enables circuit simulation with the Virtuoso Analog Design Environment, providing automatic testbench schematic generation (with system-level layout parasitic data) and streamlined binding of the schematic symbols to the IC schematic.

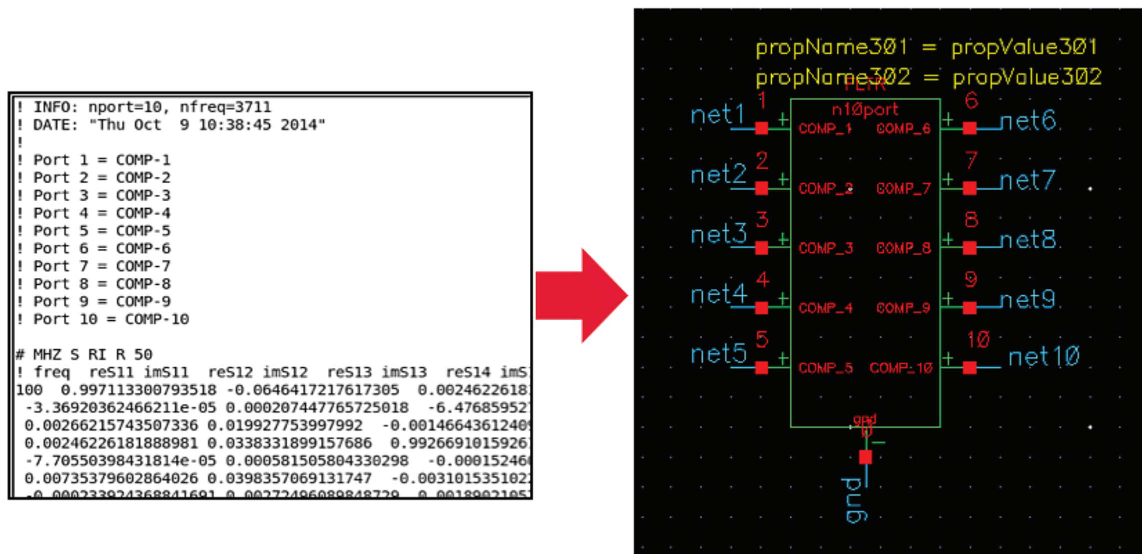

Figure 2: Sigrity environment-generated S-parameter models automate the process of manually hooking up n-port devices in the Virtuoso Schematic Editor XL

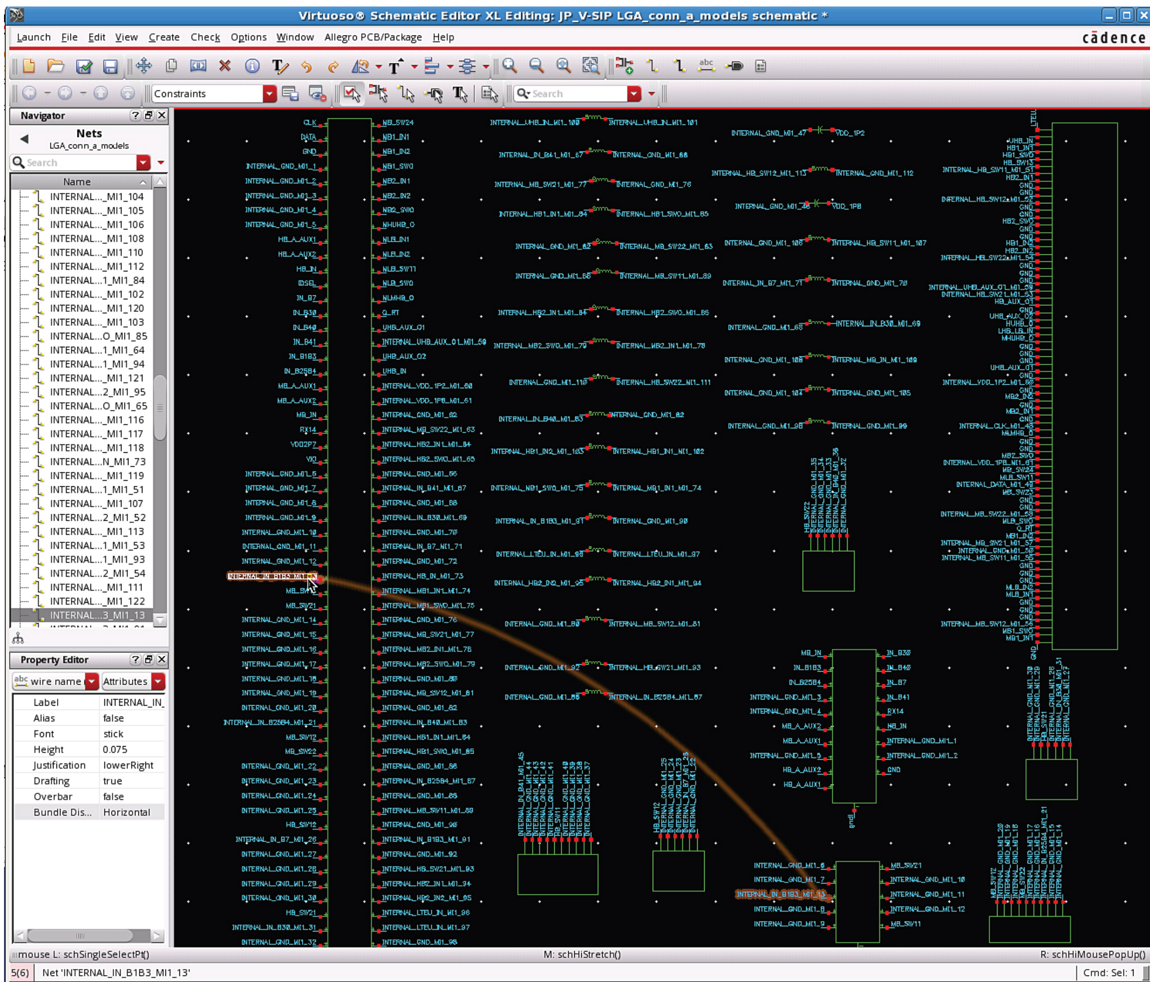

Figure 3: A system-level layout and parasitic-aware schematic, automatically generated in the Virtuoso Schematic Editor XL from Allegro and Sigrity system-level layout data

The Virtuoso System Design Platform can save time and remove the potential for human error, replacing the manual effort required to insert package/PCB S-parameter or Spice models through manual abutment of nets followed by manual stitching. For example, in an 8-pin model, the platform could save about a half hour. In a 120-pin model, that time savings could extend to a day. Without the capabilities provided by the platform, errors may not be detected until the design undergoes circuit simulation, or until it is built. The platform also automates how parts are mapped, which eliminates guesswork, and it automates the process of library development, which also saves time and minimizes error. For example, the platform tracks devices that are embedded in an electrical model during package/PCB extraction by EM-solver. The platform imports such an electrical model and places it inside the Virtuoso Schematic Editor by inserting it in the simulation schematic being created from layout connectivity and correspondingly removing the devices that were already embedded in the electrical model to avoid double counting. Other tools don't provide this type of tracking capability.

With a single schematic editor, users can now design both their package and their IC substrate. Traditionally for this process, designers have used different electronic design automation (EDA) tools that don't necessarily talk to each other. With the platform, the user can now move parts across different fabrics and assess the outcome, performing "what if" analysis to optimize interconnect routing, how the die in an IC will appear in the package, and so on. Figure 4 shows examples of RF module/SiP designs supported by the platform.

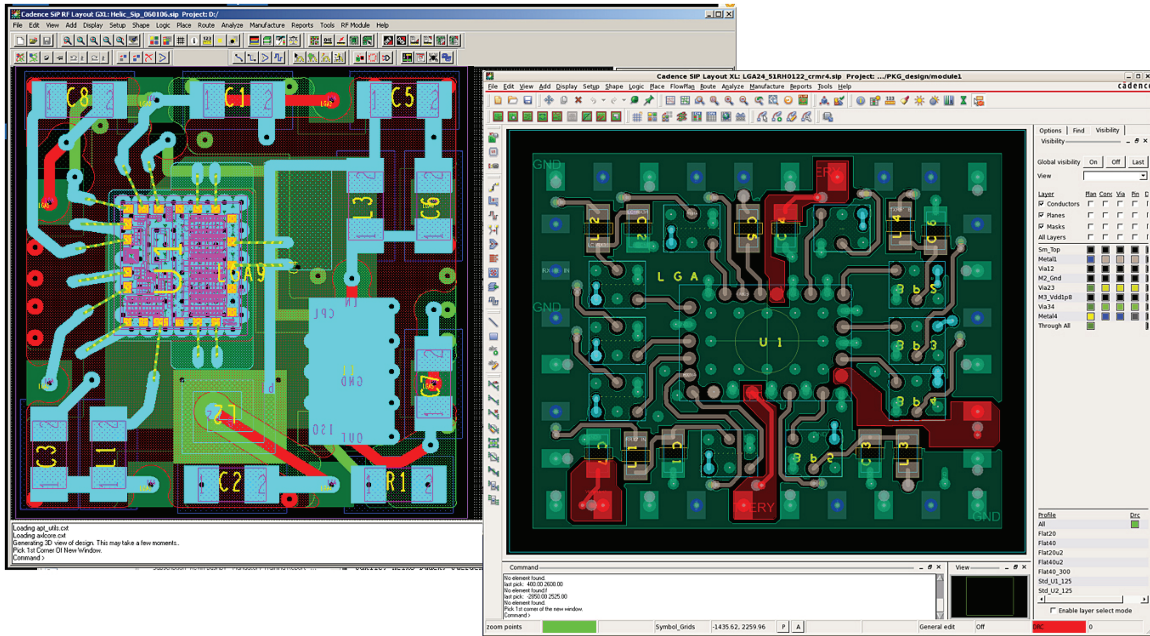

Figure 4: Design examples supported by the Virtuoso System Design Platform

Summary

Ten years ago, IC packaging was much simpler, so empirical models sufficed. Today's multi-chip models require electrical models. Back then, IC designers didn't have to worry much about the package or the PCB. Today, particularly with analog and RF designs, if an IC designer doesn't account for what is happening on the PCB or package, chances are that the chip won't work. By streamlining and automating the flow between the chip, package, and PCB, the Virtuoso System Design Platform provides IC designers with assurance that the chip they are designing will work once placed in the package and then on the PCB, before building out the design.

Further Information

To learn more about the Virtuoso System Design Platform, visit www.cadence.com/go/virtuososdp

To learn more about the Allegro and Sigrity design environments, visit https://www.cadence.com/content/cadence-www/global/en_US/home/tools/pcb-design-and-analysis.html

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