

Virtuoso System Design Platform

Unified “system-aware” platform for IC and package design

The Cadence® Virtuoso® System Design Platform is a holistic, system-based solution that provides the functionality to drive simulation and LVS-clean layout of ICs and packages from a single schematic. There are two key flows: implementation and analysis.

The implementation flow is used to create an IC package schematic in Virtuoso Schematic Editor and then transfer the schematic data to Cadence SiP Layout to layout the physical design. In addition, this flow offers the capability to generate and verify library parts, output a bill of materials (BOM), and perform layout versus schematic (LVS) checking.

The analysis flow is used to extract and simulate any portion of the system (IC-package-PCB) regardless of the layout design status. Moreover, this flow offers the capability to automatically generate schematics for the PCB and IC package layouts, bind the instances of the IC package to the IC schematic or models, and build testbenches to simulate the system using the Virtuoso ADE Product Suite plus Spectre® Multi-Mode Simulation interface. Cadence Sigriety™ models extracted from the PCB and IC package layouts get automatically stitched into the generated schematic.

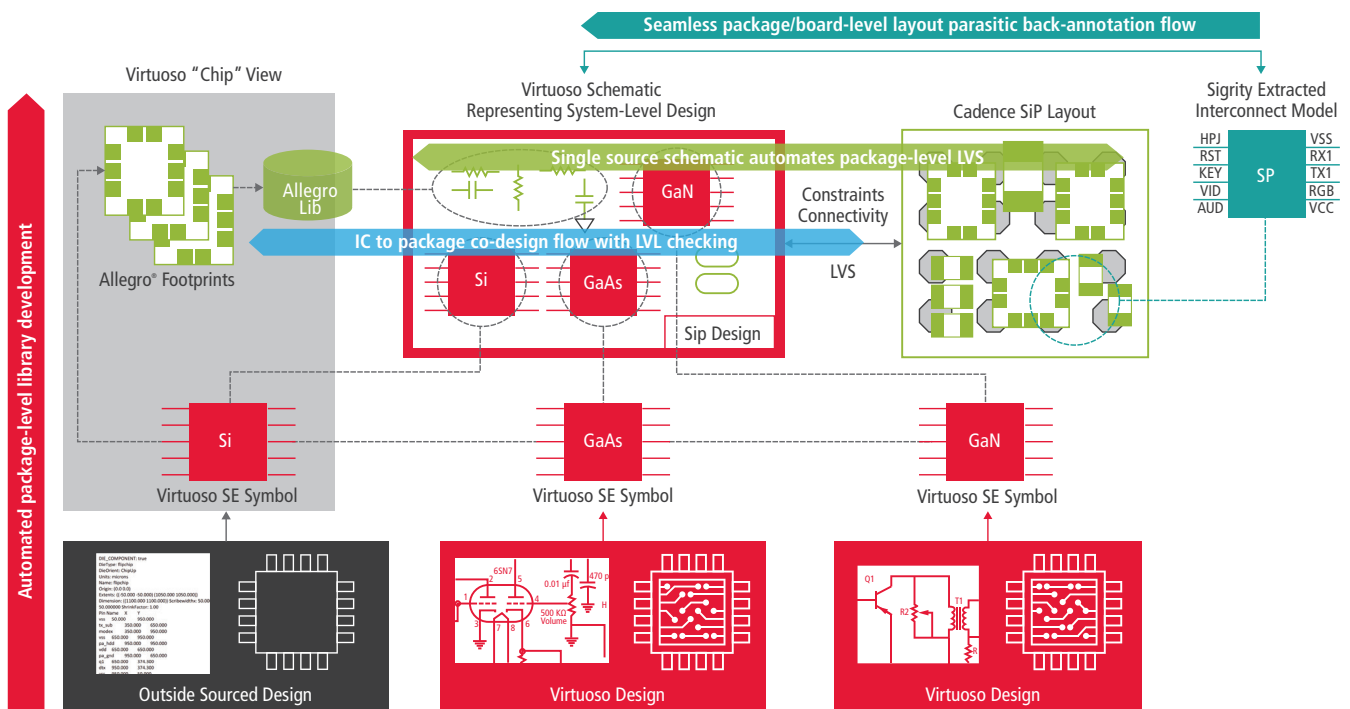


Figure 1: Virtuoso System Design Platform Flow

Introduction

The task of designing a chip that meets all product expectations once placed into a package and then onto a PCB is very challenging. With the recent growth in heterogeneous integration, now consider designing multiple chips, across multiple technologies, that integrate onto a single package and then are integrated onto a PCB. For even the most experienced designers, this can be a frightening proposition.

identify and eliminate such errors at an early design stage and long before tapeout, it is essential to have a familiar design and simulation environment that auto-enables the IC designer to simulate the IC in context of the entire PCB and package system and its parasitics. While such an environment exists for simulating I/O to I/O interconnects for digital ICs, the Virtuoso System Design Platform is the first seamless flow of its kind that allows simulation of the analog/RF IC in context of a complete PCB/package circuit

easily co-design between the die and the package to achieve better package-level routing and/or wire bonding.

The Virtuoso System Design Platform analysis flow allows the IC designer to import a PCB and package layout with its corresponding parasitic models, represented by S-parameters or SPICE, to the IC design environment. The flow reads the PCB or package connectivity and creates a schematic with parasitic models stitched-in. The schematic becomes ready to simulate in context of the PCB or package system.

The Virtuoso System Design Platform environment helps to integrate and simulate the IC in context of all such package/PCB interconnects and external components. This assumes greater importance because the IC, package, and PCB are typically designed by different teams using different design tools across geographic locations, all independent of the others and at different stages of the design cycle. The Virtuoso System Design Platform brings the package and PCB-level layout parasitics into a common schematic, enabling cross-domain simulation of the complete system. This helps designers identify critical performance deviations before tapeout. Communication of required modifications can then be driven directly to package/PCB teams.

An important feature here is to intelligently stitch the parasitics models into the simulation schematic. If the models also contain discrete devices, they should be auto-filtered when the simulation schematic is created so that they are not double-counted in the simulation.

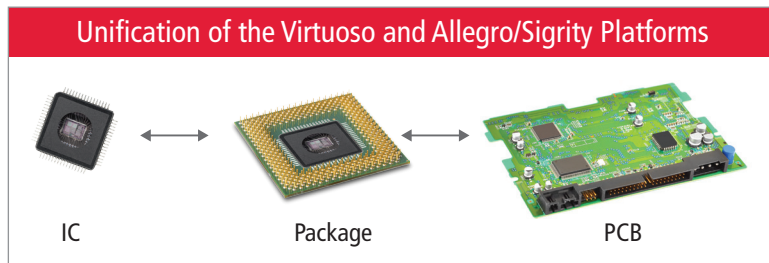


Figure 2: How IC, package, and PCB relate

Today, designing at the “system-level” (IC-package-PCB) involves a lot of educated guesswork regarding the downstream effects of the package/PCB on the performance and reliability of your chip(s). The Virtuoso System Design Platform takes this guesswork out of designing chips accounting for system-level effects.

Traditionally, the analog/RF IC designer would only simulate standalone ICs without considering the effects of the package and PCB. The package contains a single or multiple ICs and interconnects. It also probably contains discrete components required by the ICs to function. Similarly, the PCB contains several packages and interconnects and discrete components. It is important to simulate the entire system together to capture the performance at high frequencies. Because the IC designer and the package designer use different schematic entry tools, the IC designer must re-capture the package system schematic as a testbench around the IC schematic to do combined system simulations. Earlier, such system analysis had been largely a manual effort with error-prone stitching of package models to the rest of the system schematic. To

inclusive of parasitics. This flow empowers the IC designer and minimizes design iterations.

The Virtuoso System Design Platform provides an IC-centric solution with both a top-down implementation flow and bottom-up analysis-centric flow. The analysis-based flow helps bring in the complete simulation environment, requiring minimal knowledge in PCB or package and electromagnetic simulation domains. A colossal improvement in productivity is predicted with such an integrated solution.

The Virtuoso System Design Platform implementation flow provides the capability to drive IC and package layout through a single schematic editor. By having the same schematic editor (Virtuoso Schematic Editor), the IC designer is in a much better position to do system-level design in a common environment with pre-layout system simulations (IC and package together) and then drive the layout of the respective domain. This flow also automates much of the package-level library development process by generating die footprints to be used in SiP Layout. Advanced users can

Virtuoso System Design Platform

The Virtuoso System Design Platform flow traces through the following products in the IC, package, PCB, and EM solver domains:

- Virtuoso Schematic Editor: For creating the package schematic
- Virtuoso Layout Suite: For die export
- Cadence SiP Layout XL: For design and layout of multi-die packages
- Sigrity EM solvers: For extracting models of PCB and package
- Spectre Multi-Mode Simulation: For enabling system simulations

There are primarily two flows in the Virtuoso System Design Platform, the implementation and the analysis flow. The implementation flow allows you to design schematics of packages in the Virtuoso Schematic Editor before pushing it to a package layout editor. It further allows you to export die footprints and symbols from the Virtuoso Layout Suite and use them to construct a package schematic. The bidirectional flow of data dynamically propagates edits in the schematic to SiP Layout and conversely. Generating a BOM, visualizing design differences in an intuitive manner, and looking at layout reports constitute some of the other key features of this flow.

Once your package or PCB is designed using the implementation flow described above, the analysis flow lets you import PCB and package layout in the Virtuoso environment as a schematic along with the automatically stitched parasitic models of the components and traces early in the design cycle, and carry out a parasitic-aware system-level simulation. You can simulate such a system, identify critical performance metric deviation early, and communicate required modifications to the package and PCB teams.

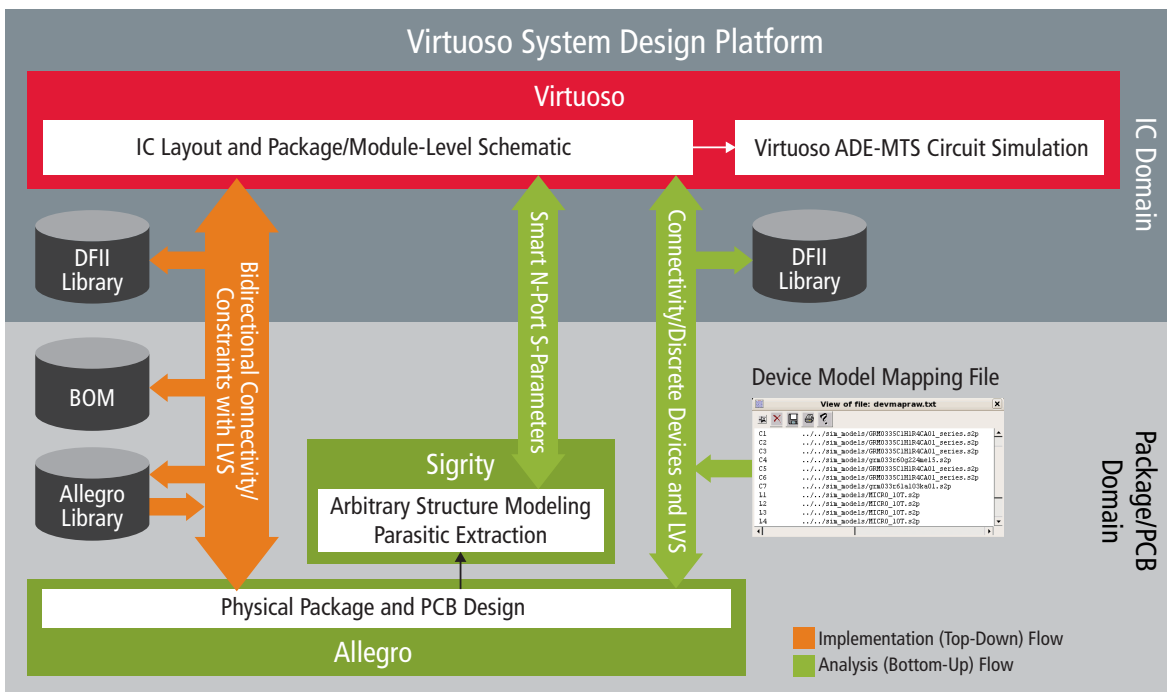


Figure 3: The Virtuoso System Design Platform flow

Benefits

By integrating the Virtuoso, Allegro, Sigrity, and Spectre platforms, the Virtuoso System Design Platform entails the following three key benefits:

- Updates the IC layout and package layout design using the Virtuoso Schematic Editor. Therefore, in addition to the IC layout, you can now design the schematic for a package layout. The Virtuoso Schematic Editor provides a single schematic editor-driven IC and package design.

- Creates a package or PCB parasitic-aware schematic that can be simulated with the Virtuoso Analog Design Environment including multi-technology simulations. This is an essential mechanism to realize complete system-aware simulations.
- Designs IC and package layout through the co-design die abstract flow simultaneously. This minimizes design iterations and cuts down on very-late-stage floorplanning and design feasibility issues.

Features

Die export

The Virtuoso System Design Platform provides a key feature to generate footprint and symbol information from a Virtuoso layout for use in constructing a package schematic and a package layout. This also allows simultaneous co-design of the IC and package layout and helps minimize design iterations.

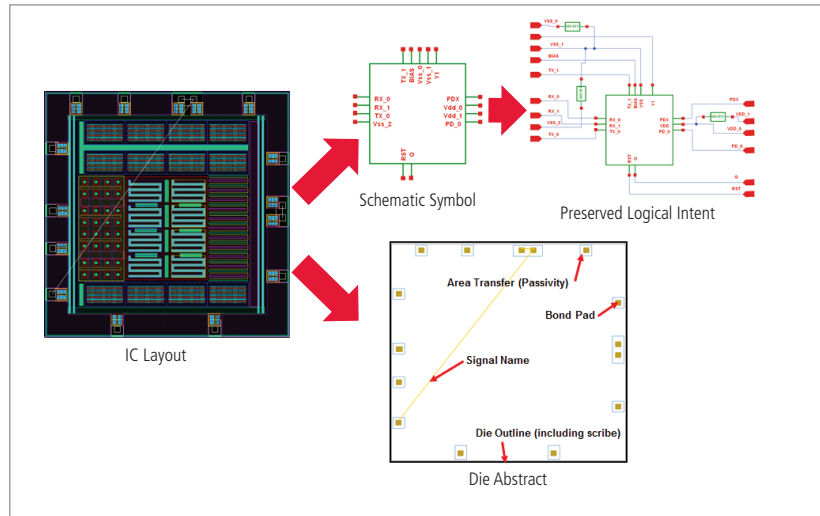


Figure 4: Die abstracts

Creating a project and assigning part table files

While creating a package schematic, it is imperative to efficiently select parts that are supplied by a vendor. The part table file option lets you seamlessly select from as many as a million parts from different vendors and assign them effectively on the instances in your schematic.

Transferring the schematic information to SiP Layout

Once the schematic with all the parts is created, this feature enables the seamless transfer of the schematic information to the SiP Layout editor. Subsequently, you can place all the parts in the SiP Layout editor and start creating routes and complete the finished package.

Editing in the SiP Layout and back-annotating in the Virtuoso Schematic Editor

During a design cycle, it is quite possible that the layout engineer recommends changes that need to be matched in the Virtuoso Schematic Editor. This feature enables transferring information seamlessly to the Virtuoso Schematic Editor and ensures that the schematic and layout are always in sync.

Design-differentiating layout vs. schematic check

Provides a signoff-quality LVS check highlighting nets, components, and similar differences between the layout and the schematic. It also flags design shorts, unplaced components on the layout, and DRC checks. It reports all the differ-

ences in a highly intuitive and graphical manner utilizing the Annotation Browser assistant in the Virtuoso Schematic Editor.

Generating a BOM report

A BOM report lists all the components used in a design along with the part numbers and values of the different properties of each component. This is an extremely important input for an original equipment manufacturer (OEM). The Virtuoso System Design Platform provides a user-friendly and highly customizable environment to generate all such reports.

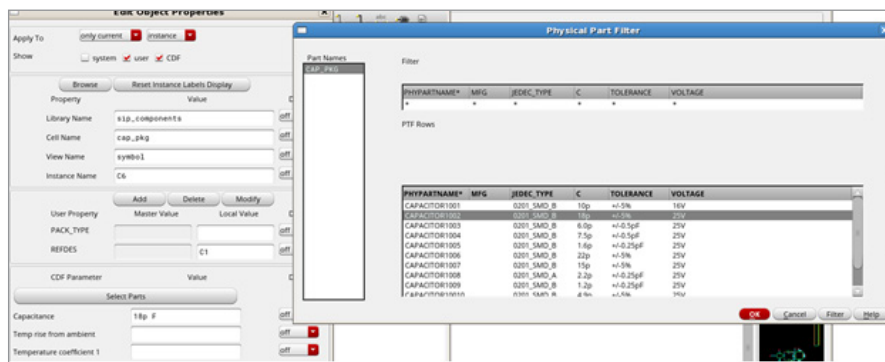


Figure 5: Selecting a package-level part from the part table file in the implementation schematic

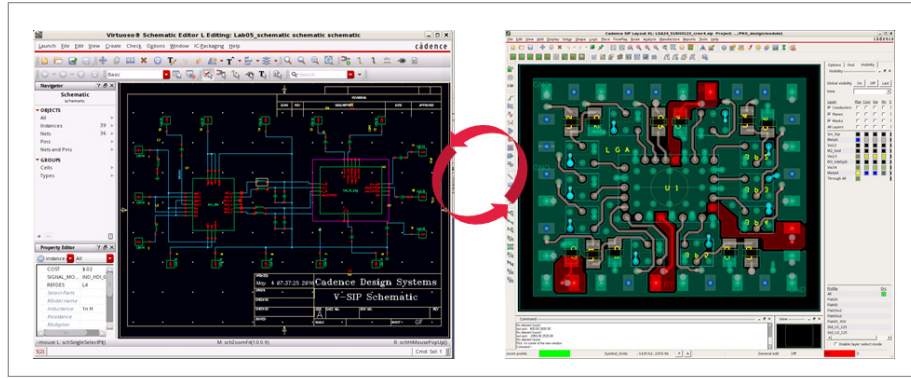


Figure 6: Schematic driving package layout

Analysis Flow Features

You can start utilizing the analysis flow once you have the design of a fully routed package.

Creating a parasitic-aware PCB/package schematic in Virtuoso Schematic Editor

Another key feature enables you to create a PCB or package schematic with S-parameters and SPICE models of the traces and PCB or package components automatically stitched in, all using the Virtuoso Schematic Editor.

It is noteworthy to highlight the analysis flow ability to use a device mapping text file to automatically replace SMDs with their corresponding vendor-specified S-parameters and SPICE models while creating the schematic. Previously, the schematic creation with all the models in place was a manual, tedious, and error-prone process.

Binding the IC footprint to its underlying schematic or sub-circuit model

Once the parasitic-aware schematic is created, the IC is imported as a simple footprint. The next important step is to bind this footprint to the original IC schematic symbol or sub-circuit. This is the same symbol that the IC designer has been using in the top-level IC simulations. The Virtuoso System Design Platform provides an intelligent mapping mechanism to create a 1:1 map between the footprint terminals and the IC symbol terminals. In cases where a schematic or a schematic symbol is not present, it allows binding to a sub-circuit model of the IC.

Automatic creation of testbench symbol for top-level system simulations

Creation of a testbench symbol is an easy, automatic, and seamless feature of testbench generation and is an integral part of the analysis flow. It reduces the design time and creates compact and manageable testbenches for you to start an early evaluation and subsequent fix of the system.

Simulation layout vs. schematic check

The simulation layout versus schematic check feature helps to flag any differences between the created schematic and the layout from which it was originally created. This feature is essential because very often a designer tends to tweak his top-level schematic to arrive at the desired results.

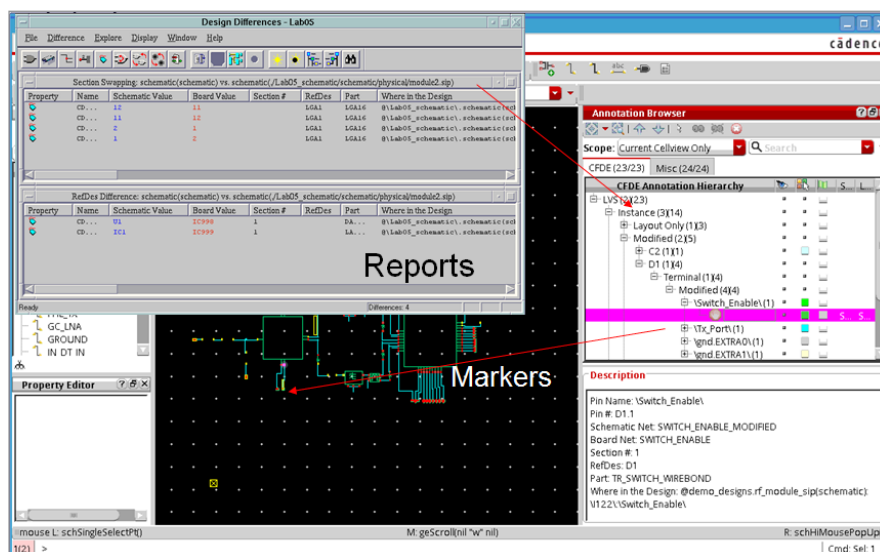


Figure 7: Viewing LVS differences highlighted in the Annotation Browser

Specifications

Third-party support

Allows seamless import of third-party vendor-supplied models of SMDs into the parasitic-aware PCB/package schematic

Design input

- Design libraries including parasitic models (SPICE and S-parameters)
- Virtuoso Layout Suite die
- Allegro PCB/package layout
- Sigrity models representing parasitic models of the traces and components on the PCB/package
- Device models of SMD's SiP layout
- Virtuoso Schematic Editor schematic
- Parasitic-aware simulation schematic
- Footprint of dies designed in Virtuoso Layout Suite

Platform/OS

- Linux for tools based on Virtuoso platform
- Linux, Microsoft Windows for tools based on Allegro and Sigrity technologies

Tools that may be required to run the Virtuoso System Design Platform flow

- Virtuoso Schematic Editor XL
- Virtuoso Layout Editor
- Virtuoso Analog Design Environment
- Spectre Multi-Mode Simulation, Spectre RF Option
- Allegro SiP and PCB layout editor
- Sigrity PowerSI®, Sigrity PowerSI 3D EM Extraction Option, and Sigrity XtractIM™ technology

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