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Cadence SiP Layout WLCSP Option

The majority of ultra-thin fan-out wafer-level chip-scale-packaging (UT-FOWLCSP) designs are the responsibility of the IC packaging design teams of the fabless semiconductor company. However, these designs place demands on the team and the design tools that are not typically encountered with traditional IC packaging methodologies, technologies, and processes. The Cadence® SiP Layout WLCSP Option now provides robust support for the specific design and manufacturing challenges of UT-FOWLCSPs.

Overview

While wafer-level chip-scale packaging (WLCSP) is not a new technology or process, as with all technologies, it evolves. In its latest evolution as UT-FOWLCSP, it is seeing adoption through its promotion by traditional IC foundries as well as leading OSAT vendors, as it provides a number of new advantages that are targeted at the handheld/mobile/wireless/multi-media product market segment.

UT-FOWLCSP technology, based on wafer molding and fine metal processes without substrate, enables the reduced thickness, optimized performance, and lower cost ideal for its initial target market, mobile computing products such as smartphones and tablets. Such devices are evolving at a rapid pace as faster and more powerful multi-core application processors become available. UT-FOWLCSP enables a thinner PoP stack with better routing density, higher operating frequency (f_{MAX}), higher memory bandwidth DRAM, and better heat dissipation than conventional chip-scale packaging methodologies.

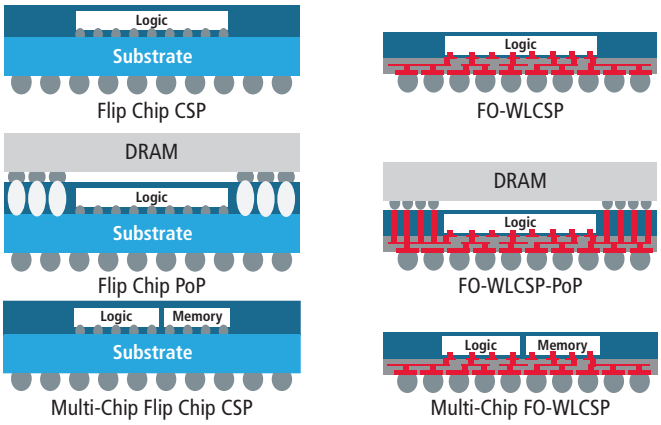

Figure 1: Examples of chip-scale-packaging compared with UT-FOWLCSP

SiP Layout WLCSP Option

The majority of these emerging UT-FOWLCSP designs are the responsibility of the IC packaging design teams of the fabless semiconductor company. However, these designs place demands on the IC packaging designer/team and the IC packaging design tools that are not typically encountered with traditional IC packaging methodologies, technologies, and processes. Through working with leaders in this emerging segment, Cadence has been able to develop the WLCSP Option for SiP Layout, which

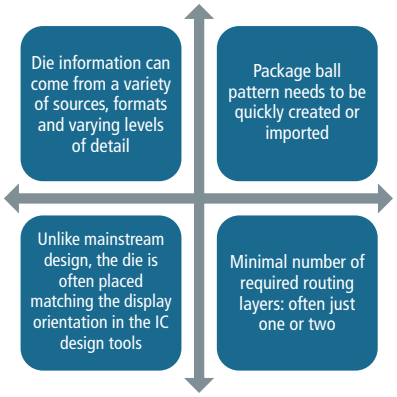

Figure 2: Some typical design challenges unique to UT-FOWLCSP implementations that must be managed by design tools and designers

provides robust support for the specific design and manufacturing challenges of UT-FOWLCSPs.

As the WLCSP Option uses a wafer-level implementation and process, the path to manufacturing is radically different from that of a typical organic IC package manufacturing process. For WLCSP, the manufacturing process is the same as, or very similar, to an IC manufacturing process. At the macro level, the differences and challenges from traditional organic IC package manufacture include:

- A process development kit/rules deck (PDK) must be used, followed by verification signoff
- FOWLCSP-specific interconnect (metal) must follow foundry/fabricator rules and techniques common in IC design and fabrication
- GDSII or Stream is the path to mask creation for the WLCSP manufacture
- PDK-adherence verification/signoff is required before a design/mask enters manufacturing

Features

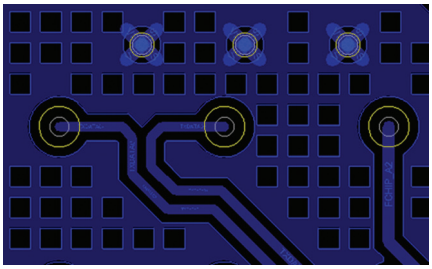

Figure 3: Metal creation and management tools allow the designer to scan, assess, and modify the localized metal density on each layer to meet the foundries' stringent fabrication requirements on both shapes and pads

The SiP Layout WLCSP Option in conjunction with the Cadence Physical Verification System (PVS) enables designers to address these macro-level items. Some of the features specific to the WLCSP Option are:

- Localized, tightly controlled metal-density creation and editing tools to control warpage in ultra-thin packages (500 to 1000µm)
- Metal-density utilities for across-design balancing with meshed metal and meshed pads

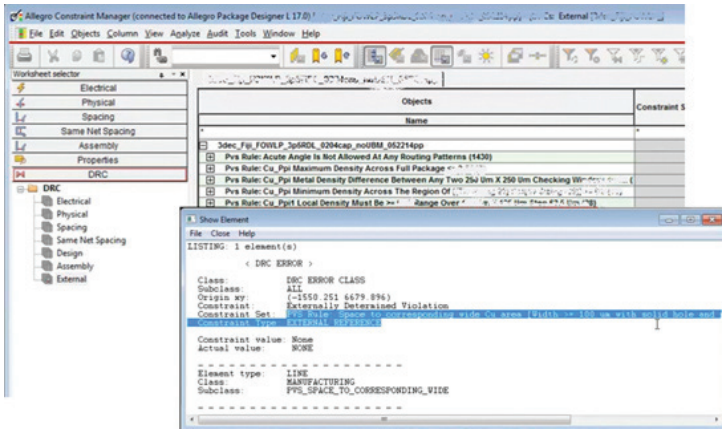

Figure 4: Foundry-supplied PDK/rules-deck-driven PVS verification results are directly displayed with the SiP Editor using the constraint manager

- High-performance GDS2 mask processing
- Direct integration with PVS for design and mask verification and signoff to PDK rules deck
- PVS verification issue highlighting and reporting directly on design canvas and in constraint manager

Platforms

The Cadence SiP Layout WLCSP Option is available with 17.2-2016 and is designed to be used in conjunction with PVS, which must be purchased separately. The SiP Layout WLCSP Option is available in these versions:

- Windows (64 bit)
- Linux (64 bit)

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- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
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