cadence®

Cadence SiP Design

Connectivity-driven co-design and implementation of full systems in package

System-in-package (SiP) implementation presents new hurdles for system architects and designers. Conventional EDA solutions have failed to automate the design processes required for efficient SiP development. By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on PCBs, Cadence® SiP design technology streamlines the integration of multiple high–pin-count chips onto a single substrate.

Cadence SiP Co-Design Technology

Manufacturers of high-performance consumer electronics are turning to system-in-package (SiP) design because it offers a number of significant advantages such as increased functional density, integration of disparate chip technologies, low power, improved signal performance/integrity, and ease of integration into a PCB system. However, this also requires expert engineering talent in widely divergent fields, which historically has limited mainstream adoption.

By streamlining the integration of multiple high–pin-count chips onto a single substrate through a connectivity-driven co-design methodology, Cadence SiP co-design technology allows companies to adopt what were once expert engineering SiP design capabilities for mainstream product development. Cadence SiP solutions seamlessly integrate with Cadence Encounter® technology for die abstract co-design, Cadence Virtuoso® technology for RF module design, and Cadence Allegro® technology for package/board co-design. See Figure 1.

Connectivity-driven SiP co-design

The Cadence connectivity-driven SiP flow focuses on the design challenges of integrating multiple large high–pin-count chips onto a single substrate. This flow targets the major challenges of SiP-level connectivity definition and management, physical concept prototyping of the SiP floorplan, including multi-chip die stacks, and die I/O planning to optimize and minimize substrate connectivity routing and signal integrity challenges. The SiP flow is driven by Encounter and Verilog® connectivity.

Cadence technology for SiP co-design includes four focused products for full SiP implementation:

- Cadence SiP Digital Architect (XL and GXL) for front-end design concept definition and evaluation
- Cadence SiP Layout (XL) for detailed constraint- and rules-driven physical substrate construction and manufacturing preparation
- Cadence SiP Digital SI (XL) for detailed interconnect extraction, modeling, and signal integrity/power delivery analysis

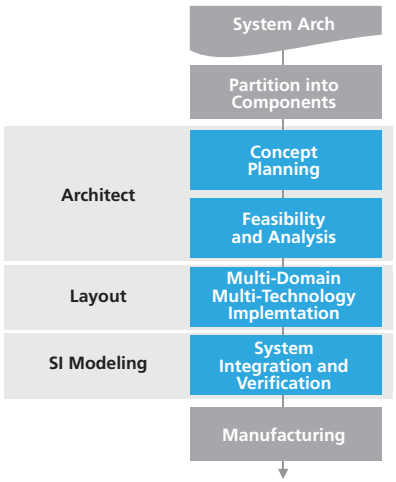

Figure 1: Cadence SiP digital design

- Cadence Chip Integration Option for direct integration with Encounter and Virtuoso IC design tools

Cadence SiP Digital Architect

SiP Digital Architect provides an SiP concept prototyping environment for early design exploration, evaluation, and tradeoff using a connectivity authoring and driven co-design methodology across die abstract, package substrate, and PCB system.

Built around a unique System Connectivity Manager, SiP Digital Architect provides a unique environment to explore and define system connectivity/functionality that is optimized between ICs, SiP package substrate, and the target PCB system through concurrent co design. It allows engineers to perform rapid "what if" feasibility studies to maximize functional density and performance while minimizing power consumption. It fully supports IC-driven or package/board substrate-driven flows with cross-fabric domain engineering change orders (ECOs) and layout versus schematic (LVS) validation. Since its design focus is predominantly digitally based, analog and/or RF mixed-signal design content is imported and managed as a hierarchical sub-block(s).

Benefits

- Allows rapid "what if" feasibility studies to optimize device functional density, performance, and power consumption
- Enables rapid system-level connectivity capture with the ability to bind into alternative physical implementation scenarios to evaluate performance and tradeoffs
- Provides IC I/O padring/array co-design and optimization at IC, substrate, and system levels

Cadence SiP Layout

SiP Layout provides a constraint- and rules-driven layout environment for SiP design. This includes substrate place and route, final connectivity optimization at the IC, substrate, and system levels, manufacturing preparation, full design validation, and tapeout. The environment features integrated IC/package I/O planning capabilities and three dimensional (3D) die stack creation and editing capabilities. In addition, full online design-rule checking (DRC) supports the complex and unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. Multi-layer flip-chip along with radial any-angle routing provide rapid constraint-driven interconnect creation.

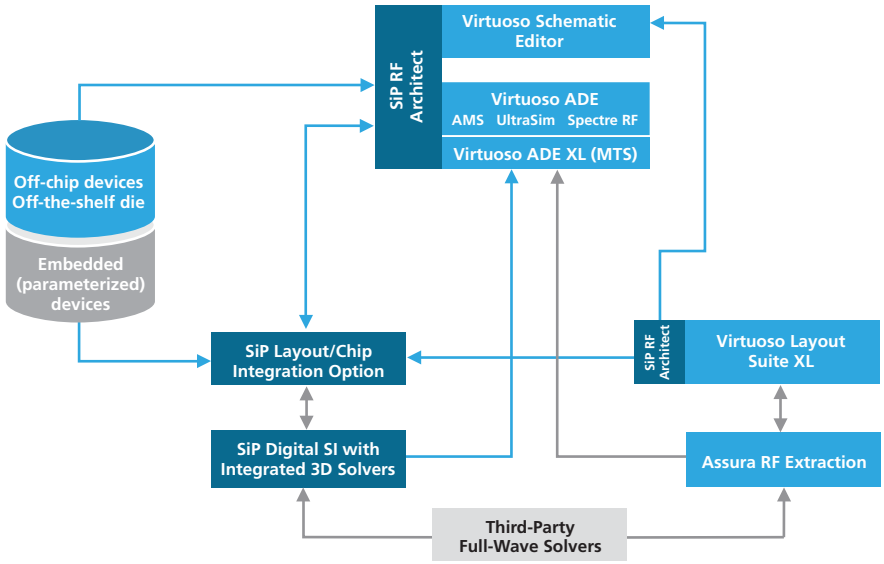

Figure 2: Cadence SiP RF/AMS design

Benefits

- Provides 3D die stack creation/editing capabilities for rapid stack assembly and optimization
- Enables IC I/O pad ring/array co-design and connectivity optimization at IC, substrate, and system levels
- Allows connectivity assignment and optimization between ICs and substrate for minimal layer usage based on signal integrity and routability
- Reduces tedious, time-consuming, and manual breakout editing via flip-chip die autoroute-breakout
- Constraint-driven HDI design with automation-assisted interactive routing speeds implementation and reduces potential errors
- Includes comprehensive substrate DFM capabilities for rapid manufacturing preparation
- Provides 3D design viewer and DRC for accurate full 3D wire bondshell verification, design review debug, and design documentation for assembly and test
- Team-based design partitioning reduces design cycle time and optimizes designer resources

Cadence SiP Digital SI

SiP Digital SI provides an environment for the co-simulation of SiP interconnect, including embedded ICs and the target PCB. By using its embedded integration with a third-party supplied 3D field solver engine combined with a SPICE-based signal integrity simulation environment, engineers can make tradeoffs to minimize cost while maximizing performance of the package module interconnect. To model and simulate complex 3D SiP structures, SiP Digital SI supports S-Parameters and fast, high-capacity simulation (10,000 bits in seconds) to provide a unique combination of fast and accurate multi-gigahertz interconnect analysis.

Benefits

- Provides a highly integrated physical and electrical design and simulation environment
- Pre/post-route interconnect analysis with graphical topology exploration enables rapid what-if performance tuning
- Includes a SPICE-based simulation engine and embedded integration with third-party supplied 3D field solvers
- Enables rapid evaluation of cost versus performance tradeoffs through its virtual prototyping environment

- Reads/writes Cadence Digital SiP Layout files
- Ensures sufficient and efficient power delivery network (PDN) design
- Creates full or partial interconnect 3D parasitic models for backannotation into Virtuoso testbenches (for RF and analog/mixed-signal SiP designs)

Schematic- and circuit simulation-driven SiP RF module design

While SiP design makes it possible to combine RF and analog chips of disparate technology on the same sub-strate, it presents a number of challenges. These include designing and integrating RF/analog chips with substrate-level buried RF passive devices as well as enabling top level pre- and post-layout circuit simulation of the entire SiP design. As seen in figure 2, Cadence SiP RF design technology provides the proven path between analog design and circuit simulation and SiP module layout. It delivers an integrated flow between the Virtuoso Analog Design Environment and SiP physical package layout and signal integrity (SI) extraction technologies. It enables the creation of a single, circuit simulation-capable, top-level SiP RF module schematic that includes the RF/analog ICs and substrate-level passive components (including packaged and embedded parameterized discretes). This schematic drives detailed SiP module layout that includes constraint-driven interconnect routing and full SiP tapeout manufacturing preparation.

Cadence SiP RF design includes four focused technologies for full SiP RF module design and implementation:

- Cadence SiP RF Architect (XL)
- Cadence SiP Layout (XL)
- Cadence Chip Integration Option
- Cadence SiP Digital SI

Cadence SiP RF Architect XL

SiP RF Architect XL provides the integration and flow environment between the Virtuoso Analog Design Environment (and/or Virtuoso Layout Suite) and Cadence SiP Layout with the Chip Integration Option. It enables the creation of a single, circuit simulation-capable, top-level SiP RF module schematic that includes the RF/analog ICs required for the final SiP design. SiP RF Architect XL provides schematic-level pre layout definition and characterization of substrate-level embedded RF passive devices. It also enables two key flows: a bi-directional engineering change order (ECO) and layout versus schematic (LVS) flow between the substrate layout and the Virtuoso Analog Design Environment, and a SiP substrate-level parasitic extraction backannotation flow into pre-defined simulation testbenches. For RF/analog ICs designed with Virtuoso Layout Editor, SiP RF Architect XL can export a design-ready SiP die footprint that includes post-wafer processing geometry adjustments.

Benefits

- Provides a single, top-level Virtuoso schematic- and simulation-driven environment for RF ICs, SiP RF module substrate, and embedded RF passive elements
- Supports bi-directional ECO and LVS flow between RF/AMS IC design team and SiP RF module layout team
- Supports substrate-level RF passive parameterized cell (Pcell) creation via Virtuoso top-level design definition
- Speeds design with direct export of SiP substrate-ready IC die footprints from Virtuoso Layout Editor
- Automates circuit simulation testbench management and parasitic backannotation from Cadence SiP Layout with the Chip Integration Option

Cadence SiP Layout/Chip Integration option

SiP Layout with the Chip Integration Option provides a complete Virtuoso schematic connectivity-driven package substrate layout environment for SiP RF module physical design. It features integrated I/O planning co-design capabilities (for digital ICs) and 3D die-stack creation and editing. It supports all packaging methods including PGA, BGA, micro-BGA, chip scale, flip-chip, and wirebond attach. SiP Layout / Chip Integration Option is based on a co-design process that manages physical, electrical, and manufacturing interfaces between design components—across all associated design fabrics—allowing designers to make tradeoffs and optimize the entire system interconnect. Full online and batch design-rule checking (DRC) supports the complex and unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. SiP Layout/Chip Integration Option also supports multiple cavities, complex shapes, and interactive and automatic wirebonding.

Benefits

- Provides bi-directional ECO and LVS flow between RF design team and SiP RF module layout team
- Supports substrate-level RF passive Pcell creation through Virtuoso top level driven design
- Allows direct import of SiP substrate-ready IC die footprints from Virtuoso Layout Editor
- Speeds die stack assembly and optimization with 3D creation/editing
- Optimizes IC I/O padring/array co-design and connectivity at IC, substrate, and system levels
- Minimizes layer usage by optimizing SI and routability-driven connectivity assignment between ICs and substrate
- Reduces tedious, time-consuming manual breakout editing via flip-chip die autoroute breakout
- Constraint-driven HDI design with automation-assisted interactive routing enables greater design miniaturization, speeds implementation, and reduces potential errors
- Includes comprehensive substrate DFM capabilities for rapid manufacturing preparation
- Includes the Cadence 3D Design Viewer and DRC for accurate, full 3D wire bondability verification, design review debug, and design documentation for assembly and test

Key Features*

**Reference the product capabilities grid at the end of this datasheet to see which features are applicable to each product.*

System Connectivity Manager

The System Connectivity Manager is the "cockpit" or "dashboard" of SiP Digital Architect. It allows the project architect to rapidly author and/or capture the connectivity of the SiP, which includes importing IC die Verilog netlists for chips that comprise the SiP design and interfacing to the PCB footprint symbol of the completed SiP. Embedded LVS routines and ECO management capabilities ensure that the logical SiP definition matches the physical SiP implementation, including any ICs that are partitioned and co-designed as part of the SiP.

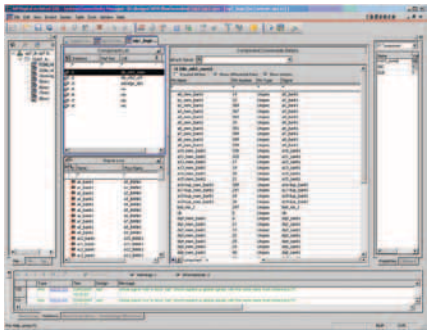

Figure 3: System Connectivity Manager

Virtual system interconnect (VSIC) models

An integrated graphical and topological interconnect modeling and simulation capability enables the creation and exploration of the SI performance of proposed system-level connectivity. Embedded simulation capability provides time and frequency domain interconnect simulation, including industry-standard S-Parameter models. The embedded integration with a third-party supplied full 3D quasi-static field solver further enables the extraction and creation of detailed, accurate geometric IBIS, RLGC, or S-Parameter models of complex 3D interconnect structures.

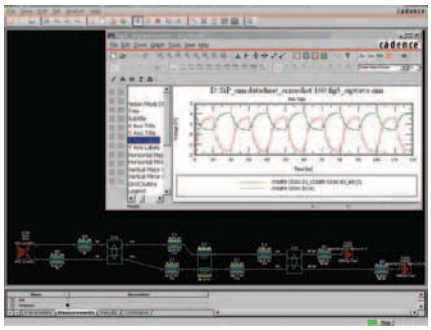

Figure 4: Virtual system interconnect models

Die editor

Distributed IC-package co-design is enabled through the die editor, which provides visibility of the chip I/O pad ring and bump matrix within the context of the SiP substrate editing canvass. Interconnect flight lines are displayed between the I/O and bump. The die editor allows the user to visualize and edit I/O and bump locations. The I/O, bump, and interconnect data is initialized from a die abstract created from Encounter technology.

Optimized I/O and bump assignments are then passed back to the Encounter tool through the die abstract.

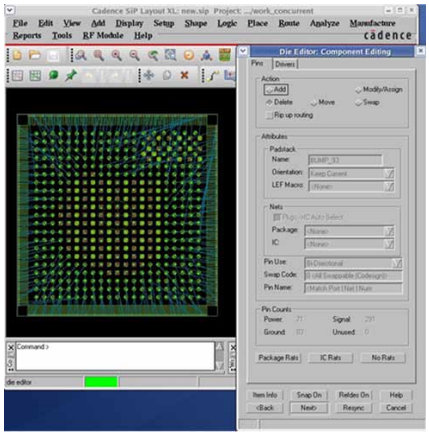

Figure 5: Die editor enables distributed co-design

I/O planner

Concurrent IC-package co-design is enabled through the IC I/O planner, which provides the definition and optimization of the co-design die bump matrix, I/O pad ring/array through connectivity assignment, I/O placement, and redistribution layer (RDL) routing.

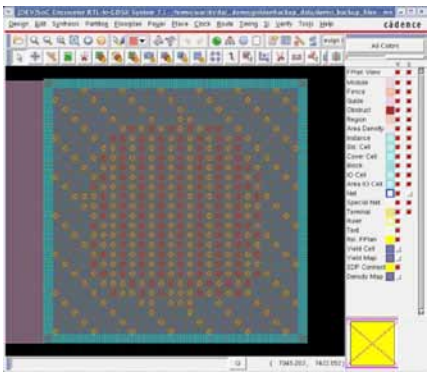

Figure 6: I/O planner

It can create either a die abstract from scratch, or load an abstract from the digital IC design team (LEF/DEF or OA), and then optimize it in the context of the SiP substrate as well as other IC die in the design. The I/O planner is based on Encounter technology, ensuring it is 100 percent compatible with the chip design team's IC tools and provides complete IC technology file compliance.

Note: This feature is not available on Windows (Linux / Unix only).

Substrate floorplanner

The floorplanner allows the physical prototyping and evaluation of various substrate-level SiP implementation concepts. It provides a full rules-driven, connectivity-based capability that ensures a correct-by-construction approach. The die abstracts, discrete components, and connectivity and constraint data is used to build the physical SiP implementation. The SiP architect can then use the graphical, intuitive editing tools to construct and evaluate critical sections of the design.

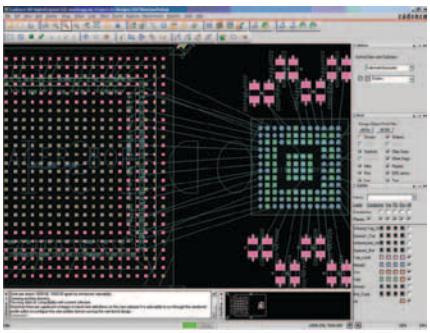

Figure 7: Substrate floorplanner

3D die stack editor

The die stack editor provides a 3D construction environment for assembling complex die stacks that can include spacers, interposers, and die-attach methods such as wirebond and flip-chip.

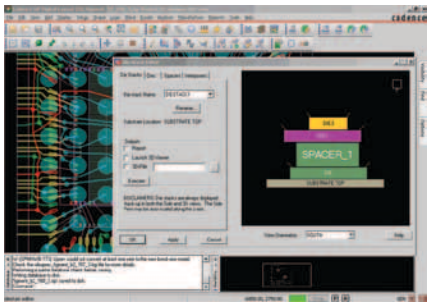

Figure 8: 3D die stack editor

3D Design Viewer

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design, or a selected design subset such as a die stack or complex via array. It also provides a common reference point for cross-team design reviews.

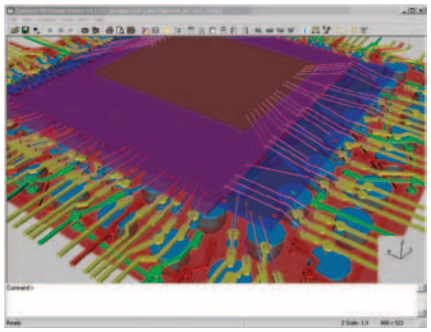

Figure 9: 3D design viewer

Embedded integration with third-party 3D field solvers

Seamless integration with third-party supplied quasi-static and full-wave field solver engines combined with SPICE-based simulation engines—all accessed directly from within the physical SiP design environment—enable modeling and simulation of package interconnect without the time-consuming setup of standalone point tools. Engineers can quickly check tradeoffs to the physical design to ensure that electrical requirements are not compromised. Integration of analysis and design technology also allows analysis tasks that were formerly done by package SI experts to be shared by a broader group within the SiP design community.

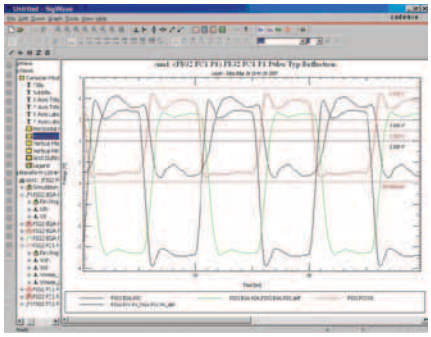

Figure 10: Embedded signal integrity simulation

Package modeling for system-level analysis

Creation of IBIS, RLC, or Cadence DML interconnect models is easily accomplished, either for a selected set of nets or for the entire package. Design teams can then easily reuse these models at the system level to ensure that package effects are properly considered when optimizing PCB cost/performance tradeoffs.

Power delivery network design for low power

An integrated analysis environment enables sufficient, efficient, and stable power delivery network design through the optimization of the package impedance profile and minimizes power supply voltage ripple.

Integrated constraint management

The spreadsheet-based integrated constraint management system provides the definition, application, and management of interconnect constraints and topologies at the physical prototyping and implementation level. Designers can import constraints and apply them to industry-standard bus protocols—such as PCI Express and DDR2—through hierarchical interconnect topology templates that are available from Cadence as well as various IC vendors. (See Figure 11.)

Chip-level IR drop analysis

Integration with Encounter Power System enables the creation of package power and ground RLC models that can be automatically consumed by IC core IR drop analysis (static and dynamic).

Substrate editor

The substrate place-and-route editor allows the package layout designer to physically implement an SiP design based on the final chosen concept, including all levels of manufacturing preparation prior to mask creation. It provides a full rules-driven, connectivity-based capability (driven by SiP RF Architect's integration with the Virtuoso environment) that ensures a correct-by-construction approach backed by a comprehensive design and assembly rule checking environment.

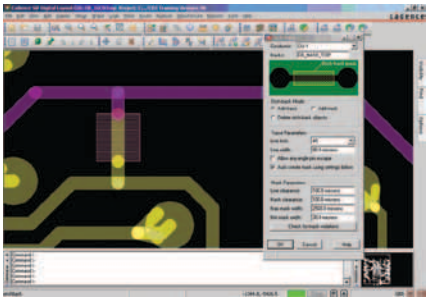

Figure 12: Substrate editor

The die abstracts, discrete components, and connectivity and constraint data are used to build the physical SiP implementation. The package layout

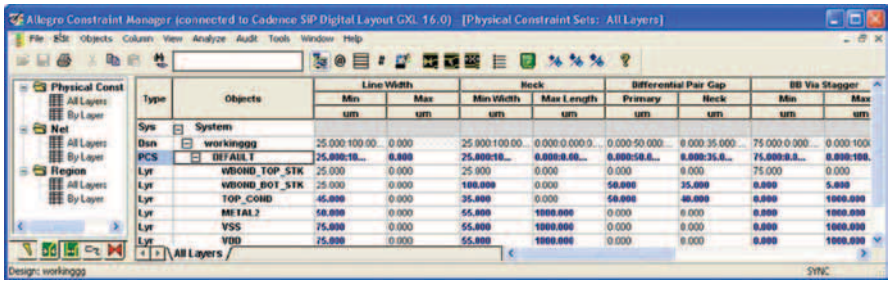

Figure 11: Integrated constraint management

designer can then use intuitive graphical editing tools to implement the design and prepare it for manufacturing. It also supports all packaging methods: PGA, LGA, BGA, micro-BGA, and chip scale, as well as flip-chip and wirebond attach methods. An embedded, push-button, full 3D quasi-static field solver enables the extraction and creation of detailed, accurate geometric RLC or S-Parameter package simulation models for use during PCB design.

Auto/interactive wirebonding

A new, highly productive environment provides fast, powerful, and flexible bondshell creation and editing. Constraint/rules-driven automatic bondfinger array placement can be used with staggered die pads, multiple bond levels, multiple bond rings, and both symmetrical and non-symmetrical designs. For fast initial what-if prototyping of single or multiple die stacks, the "autobond" feature instantly creates a symmetrical bondshell pattern including power and ground rings. Unique push and shove bondfinger editing enables extremely complex bondshells to be developed in minutes, delivering unparalleled capability and productivity. True wireprofile support enables DFM-driven design using manufacturing-verified wire loop data. An included Kulicke & Soffa-verified loop profile library ensures that any wirebond patterns designed meet manufacturing signoff. (See Figure 13.) Wirebond-attached die flags and power/ground rings can be quickly created, edited, and optimized for multiple voltage supplies.

Assembly rule checking (ARC)

A comprehensive assembly and manufacturing rule checker (Figure 14) provides more than 50 SiP-specific checks. Check can be executed as a check-group, individually, or as a custom selection. Check results appear in the Constraint Manager DRC tab and as graphical markers in the design.

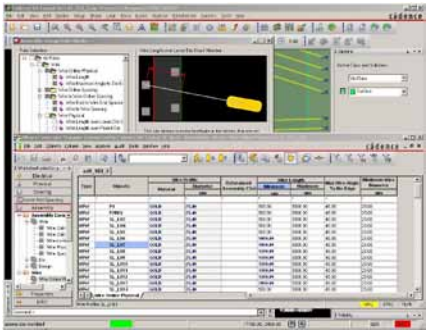

Figure 14: Comprehensive ARC environment

Flow integration with Virtuoso Layout Editor

SiP RF Architect XL provides a single, integrated design flow built around the Virtuoso DFII framework. It also provides a single, system-level, simulation-ready Virtuoso schematic for RF/analog die, SiP substrate, and packaged and embedded passive components. It enables direct export of SiP-level IC die footprints from Virtuoso Layout Editor and schematic-driven SiP substrate-level RF Pcell creation (Figure 15). For post-route circuit simulation, SiP RF Architect XL provides a complete parasitic extraction and backannotation methodology including automatically maintained circuit simulation testbenches for critical signal paths.

Specifications

System requirements

- OpenGL graphics compliance with a minimum 64MB of dedicated graphics memory

Platform/OS

- Windows XP, Vista Enterprise
- Solaris
- Linux

Interfaces

- LEF/DEF 5.1 to 5.7
- OA 2.2
- Verilog

Third-party support

- Apache PakSI-E 3D field solver engine
- CST Studio full-wave solver engine

Figure 13: Auto/interactive wirebonding using Kulicke & Soffa-verified wireprofiles

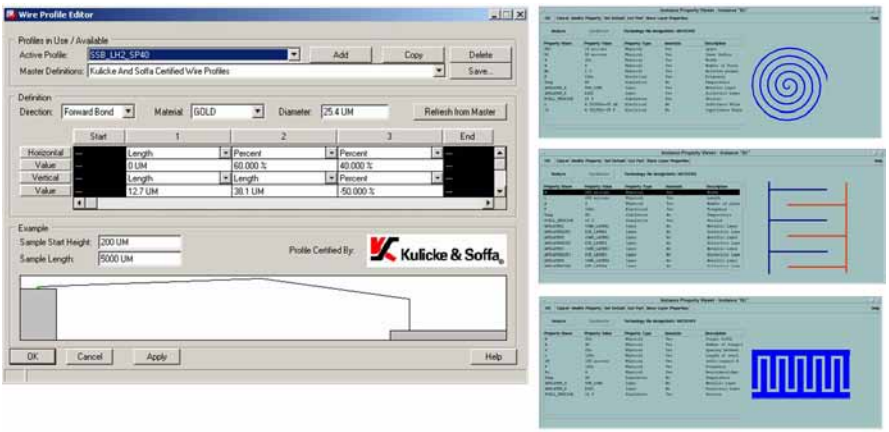

Figure 15: Advanced layout capabilities include true 3D wirebond profiles and Virtuoso technology-driven parameterized Pcell passive components

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

Feature Summary

	SiP Layout*	SiP Layout and Chip Integration Option	SiP Digital Architect	SiP Digital SI**	SiP RF Architect
Front-End Design Creation					
System Connectivity Manager with logical co-design objects			XL/GXL		
Full SiP LVS (substrate and ICs)			XL/GXL		•
Virtuoso Analog Design Environment, schematic/ layout integration and flow					•
Substrate-level embedded RF passive synthesis					•
Parasitic backannotation into system-level testbenches					•
Signal Integrity					
SigXplorer topology editor and simulator (pre-route)			GXL	•	
SigXplorer topology editor and simulator (pre- and post-route)				•	
S-Parameter interconnect modeling and SI simulation			GXL	•	
Source synch and serial interface simulation			GXL	•	
3D PCB full-package simulation model creation			GXL	•	
Embedded integration with a (third-party-supplied) 3D field solver			GXL	•	
Co-planar coupling extraction			GXL	•	
Spectre transistor-level simulation engine			GXL	•	
Channel analysis for high-capacity SI simulation			GXL	•	
Power delivery network (PDN) optimization and verification				•	
Etch back stub effects simulation			GXL	•	
Package/pin delay length report			GXL	•	
Substrate Design					
Constraint Manager (electrical/physical and DRC)	•	•	XL/GXL	•	
Import/export Allegro Package Designer (.mcm) database	•	•	GXL	•	
Interactive (i/a) and automatic component (packaged and bare die) placement	•	•	GXL	i/a only	
Auto/interactive wirebonding including rapid autobond	•	•	GXL		
User-definable wirebond model profiles including XML import	•	•	GXL		

	SiP Layout*	SiP Layout and Chip Integration Option	SiP Digital Architect	SiP Digital SI**	SiP RF Architect
Full and partial design connectivity assignment and optimization (router based, closest match, interactive, and constraint-based)	•	•	GXL		
Interactive and automatic interconnect routing (free angle and multi-layer orthogonal)	•	•	GXL		
On-line soldermask checking	•	•			
Recursive breakout pattern creator (flip-chip and wirebond)	•	•			
Static-style screen rulers		•			
Advanced Design					
Distributed co-design with die editor (using die abstract)	•	•	GXL		
Concurrent co-design with I/O planning co-design editor (using LEF/DEF and OA 2.2)		Unix/Linux only	GXL (Unix/Linux only)		
Hierarchical GDSII output	•	•			
Team-based design (design partitioning)	•	•			
Embedded RF passive creation and editing		•			
3D Design Viewer and 3D wirebond DRC	•	•	GXL	•	
3D die stack editor	•	•	GXL	•	
Support for multiple die stacks	•	•	GXL	•	
Interconnect cline spreading	•	•			
BGA editor	•	•	GXL	•	
Constraint-driven HDI design	•	•	GXL	•	
DFM Preparation/Output					
Die/BGA footprint compare using DEF/OA/.TXT	•	•			
Filled shapes (metal) creation and editing	•	•			
Design documentation (dimensioning, annotation)	•	•			
Assembly rule checking (ARC) system	•	•			
Etch back of plating traces	•	•			
Plating bar generation	•	•			
Manufacturing/documentation export/import capabilities (stream, dxf, AIF)	•	•			
Substrate mask output (Gerber, GDSII)	•	•			
Full design-status reporting capabilities	•	•			
Waived DRCs (creation and reporting)	•	•			
Degassing of filled metal shapes	•	•			
Thieving (metal area balancing)	•	•			

** Note that license for this product also authorizes use of Allegro Package Designer at the XL level (see Allegro Package Designer datasheet)*
*** Note that license for this product also authorizes use of Allegro Package SI at the XL level (see Allegro Package Designer datasheet)*

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com

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