cadence®

# Cadence SiP RF Design

Cadence® SiP RF design technology provides the proven path between Cadence Virtuoso® analog design and circuit simulation and SiP module layout. It enables analog/RF or wireless design teams to create a single, system-level, circuit simulation-ready schematic containing multiple RF/analog chips and SiP substrate including packaged and embedded parameterized discretes. The schematic drives detailed SiP RF module layout that includes constraint-driven interconnect routing and full SiP tapeout manufacturing preparation.

Cadence SiP RF design includes four focused technologies for full SiP RF module design and implementation:

- Cadence RF SiP Methodology Kit
- Cadence SiP RF Architect XL
- Cadence SiP RF Layout GXL
- Cadence SiP Digital SI

## Cadence SiP Design Technology

Manufacturers of high-performance consumer electronics are turning to system-in-package (SiP) design because it provides a number of advantages over SoC design. In addition to lowering cost, reducing power consumption, and increasing performance, SiP design offers the flexibility to mix RF and high-speed digital circuitry in the same package. However, these advances require expert engineering talent in widely divergent fields—and conventional solutions have failed to automate the design processes required for efficient SiP development.

By enabling and integrating design concept exploration, capture, construction, optimization, and validation of complex multi-chip and discrete substrate assemblies on printed circuit boards (PCBs), Cadence SiP design technology streamlines the process of combining multiple high-pin-count chips on a single substrate. This approach allows companies to adopt the most advanced SiP design capabilities for mainstream product development.

Cadence SiP design technology integrates seamlessly with Cadence Encounter® technology for die abstract co-design, Cadence Virtuoso® technology for RF module design, and Cadence Allegro® technology for package/board co-design. (See Figure 1.)

## Schematic- and Circuit-simulation–Driven SiP RF Module Design

While SiP design makes it possible to combine RF and analog chips of disparate technology on the same substrate, it presents a number of challenges. These include designing and integrating RF/analog chips with substrate-level buried RF passive devices as well as enabling top-level pre- and post-layout circuit simulation of the entire SiP design.

Cadence SiP RF design technology provides an integrated flow between the Virtuoso Analog Design Environment and SiP physical package layout and signal integrity (SI) extraction technologies. It enables the creation of a single, circuit-simulation–capable, top-level SiP RF module schematic that includes the

RF/analog ICs and substrate-level passive components required for the final SiP design. Cadence SiP RF design includes four focused technologies for full SiP RF module design and implementation:

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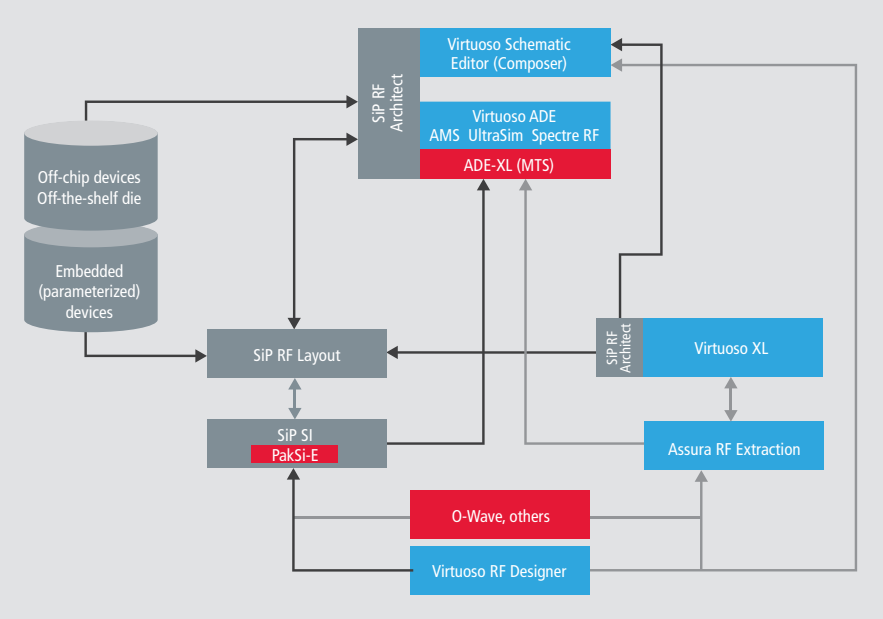


*Figure 1: Cadence SiP Design Technology*

# Cadence RF SiP Methodology Kit

The Cadence RF SiP Methodology Kit leverages Cadence SiP RF design technology and adds verified advanced methodologies with a full segment representative design. By increasing design productivity and quality, the Kit enables wireless design teams to have predictable design schedules and helps them achieve first-pass success. The Kit also provides an excellent training vehicle for fast ramp-up. (See Figure 2.)

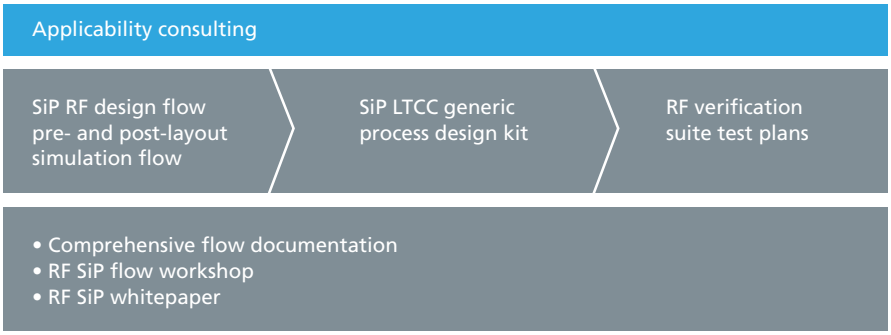


*Figure 2: Cadence RF SiP Methodology Kit*

# Cadence SiP RF Architect XL

Cadence SiP Digital SICadence SiP RF Architect XL provides the integration and flow environment between the Virtuoso Analog Design Environment (and/or Virtuoso Layout Editor) and Cadence SiP RF Layout GXL. It enables the creation of a single, circuit-simulation–capable, top-level SiP RF module schematic that includes the RF/analog ICs required for the final SiP design. SiP RF Architect XL provides schematic-level pre-layout definition and characterization of substrate-level embedded RF passive devices. It also enables two key flows: a bi-directional engineering change order (ECO) and layout versus schematic (LVS) flow between the substrate layout and the Virtuoso Analog Design Environment, and a SiP substrate-level parasitic extraction backannotation flow into pre-defined simulation testbenches. For RF/analog ICs designed with Virtuoso Layout Editor, SiP RF Architect XL can export a design-ready SiP die footprint that includes post-wafer processing geometry adjustments.

## Benefits

- Provides a single, top-level Virtuoso schematic- and simulation-driven environment for RF ICs, SiP RF module substrate, and embedded RF passive elements
- Supports bi-directional ECO and LVS flow between RF/AMS IC design team and SiP RF module layout team
- Supports substrate-level RF passive parameterized cell (P-cell) creation via Virtuoso top-level design definition
- Speeds design with direct export of SiP substrate-ready IC die footprints from Virtuoso Layout Editor
- Automates circuit simulation testbench management and parasitic backannotation from Cadence SiP RF Layout GXL
- Direct integration with Virtuoso RF Designer full wave field solver speeds design verification through direct package interconnect extraction
- Provides rapid adoption path via the Cadence RF SiP Methodology Kit for wireless application implementation

# Cadence SiP RF Layout GXL

Provides rapid adoption path via the Cadence RF SiP Methodology Kit for wireless application implementationCadence SiP RF Layout GXL provides a complete Virtuoso schematic connectivity-driven package substrate layout environment for SiP RF module physical design. It features integrated I/O planning co-design capabilities (for digital ICs) and 3D die-stack creation and editing. It supports all packaging methods including PGA, BGA, micro-BGA, chip scale, flip-chip, and wirebond attach. SiP RF Layout GXL is based on a co-design process that manages physical, electrical, and manufacturing interfaces between design components—across all associated design fabrics—allowing designers to make tradeoffs and optimize the entire system interconnect. Full online and batch design-rule checking (DRC) supports the complex and unique requirements of all combinations of laminate, ceramic, and deposited substrate technologies. SiP RF Layout GXL also supports multiple cavities, complex shapes, and interactive and automatic wirebonding.

## Benefits

- Provides bi-directional ECO and LVS flow between RF design team and SiP RF module layout team
- Supports substrate-level RF passive P-cell creation through Virtuoso top-level driven design
- Allows direct import of SiP substrate-ready IC die footprints from Virtuoso Layout Editor
- Speeds die stack assembly and optimization with 3D creation/editing
- Optimizes IC I/O padring/array co-design and connectivity at IC, substrate, and system levels
- Minimizes layer usage by optimizing SI and routability-driven connectivity assignment between ICs and substrate
- Reduces tedious, time-consuming manual breakout editing via flip-chip die autoroute-breakout
- Constraint-driven HDI design with automation-assisted interactive routing enables greater design miniaturization, speeds implementation, and reduces potential errors
- Includes comprehensive substrate DFM capabilities for rapid design manufacturing preparation
- Includes the Cadence 3D Design Viewer and DRC for accurate, full 3D wire bondability verification, design review debug, and design documentation for assembly and test

# Cadence SiP Digital SI

Cadence SiP Digital SI provides an environment for the co-simulation of SiP interconnect including embedded ICs and the target PCB. By using its integrated SI, parasitic extraction, and embedded integration with third-party 3D field solvers, engineers can make tradeoffs to minimize cost while maximizing performance of the package module interconnect. To model and simulate complex 3D SiP structures, SiP Digital SI includes embedded integration with third-party 3D field solvers, integrated S-Parameter support, and fast, high-capacity simulation (10,000 bits in seconds) to provide a unique combination of fast and accurate multi-gigahertz interconnect analysis.

## Benefits

- Provides a highly integrated physical and electrical design environment
- Enables rapid what-if performance tuning via pre- and post-route interconnect analysis with graphical topology exploration
- Ensures sufficient and efficient power delivery network (PDN) design
- Includes a SPICE-based simulation engine and embedded integration with a third-party supplied 3D field solver
- Creates full or partial interconnect 3D parasitic models for backannotation into Virtuoso testbenches
- Quickly evaluates cost versus performance tradeoffs through its virtual prototyping environment

## Features*

### Flow integration between Virtuoso Layout Editor and SiP RF Layout GXL

SiP RF Architect XL provides a single integrated design flow built around the Virtuoso DFII framework. It also provides a single, system-level, simulation-ready Virtuoso schematic for RF/analog die, SiP substrate, and packaged and embedded passive components. It enables direct export of SiP-level IC die footprints from Virtuoso Layout Editor and schematic-driven SiP substrate-level RF P-cell creation. For post-route circuit simulation, SiP RF Architect XL provides a complete parasitic extraction (including use of Virtuoso RF Designer for inductors) and backannotation methodology including automatically maintained circuit simulation testbenches for critical signal paths. (See Figure 3.)

### Integrated Constraint Management

The spreadsheet-based integrated constraint management system defines, applies, and manages interconnect constraints and topologies at the physical prototyping and implementation level. Designers can import constraints and apply them to industry-standard bus protocols such as PCI Express and DDR2/DDR3 through hierarchical interconnect topology templates available from Cadence as well as various IC vendors. (See Figure 4.)

### I/O planner (for digital IC die co-design)

The IC die abstract I/O planner defines and optimizes co-design die bump matrixes, I/O padring/array through connectivity assignment, I/O placement, and redistribution layer (RDL) routing. It can either create a die abstract from scratch or load an abstract from the digital IC design team (LEF/DEF or OpenAccess), and then optimize it in the context of the SiP substrate as well as other IC die in the design. The I/O planner is based on proven Encounter technology ensuring it is 100% compatible and compliant with the IC design teams technology file. (See Figure 5.)

### Substrate editor

The substrate place-and-route editor allows the package layout designer to physically implement the SiP design based on the final chosen concept. It provides a full rules-driven, connectivity-based capability (driven by SiP RF Architect XL's integration with the Virtuoso environment) for top-level SiP netlist definition, ensuring a correct-by-construction approach. The die abstracts, discrete components, and connectivity and constraint data are used to implement the physical SiP. Substrate-level passive structures (inductors, capacitors,

**Reference the product capabilities grid at the end of this datasheet to see what features are applicable to what product.*

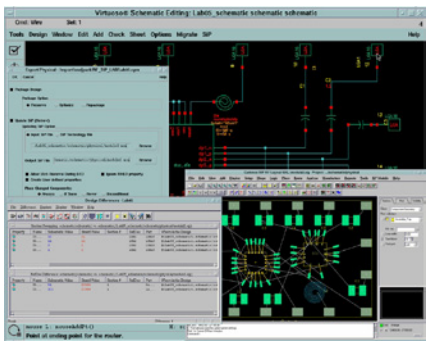

*Figure 3: Flow integration between Virtuoso software and SiP RF Layout GXL*

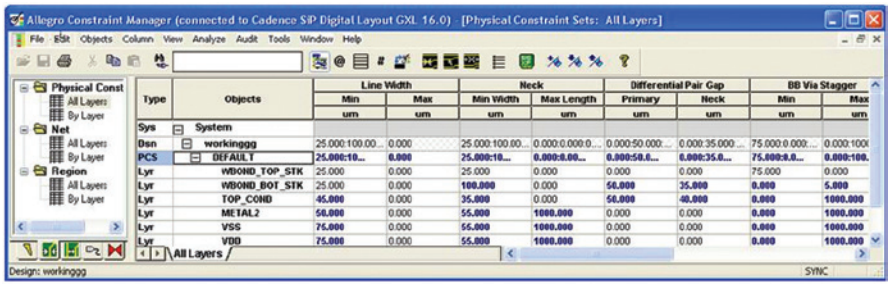


*Figure 4: Integrated Constraint Management*

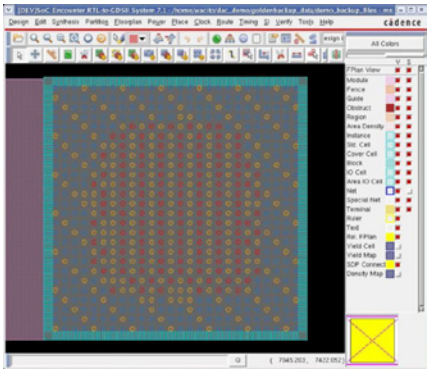

*Figure 5: I/O planner*

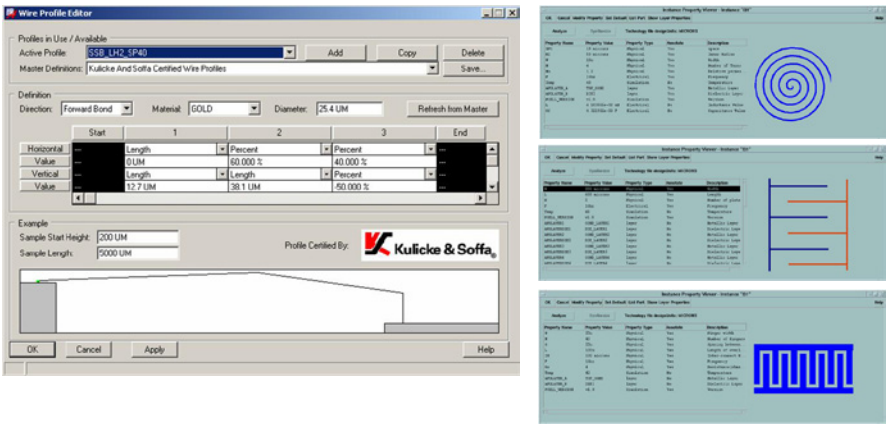


*Figure 6: Advanced layout capabilities include true 3D wirebond profiles and Virtuoso technology-driven parameterized "p-cell" passive components*

transmission lines, etc.) defined during connectivity capture and circuit simulation are synthesized into physical metal structures as intelligent programmable cells. The package layout designer can then use the graphical, intuitive editing tools to implement the design and prepare it for manufacturing. The substrate editor supports all packaging methods, including PGA, LGA, BGA, micro-BGA, and chip scale, as well as flip-chip and wirebond attach methods. (See Figure 6.)

## Assembly rule checking

A comprehensive assembly and manufacturing rule checker provides more than 50 SiP-specific checks. Check can be executed as a check-group, or individually, or as a custom selection. Check results appear in the constraint manager DRC tab and as graphical markers in the design. (See Figure 7.)

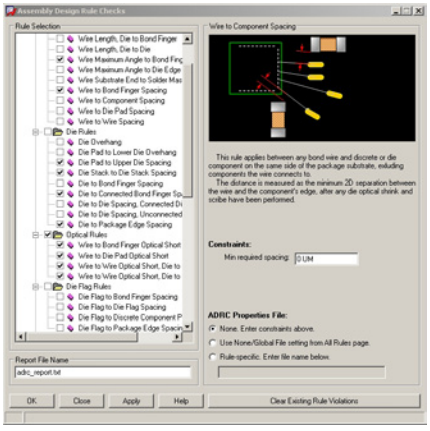

*Figure 7: Advanced Assembly Rule Checking enables DFM ready verification*

## 3D die stack editor

The die stack editor provides a 3D construction environment for assembling complex die stacks. Die stacks are instantiated on the 2D substrate design as hierarchical design objects. (See Figure 8.)

## High density interconnect (HDI) design

HDI or build-up layer technology is pervasive in almost all IC Package design using routable organic substrates and fine pitch flipchip devices. SiP RF Layout has comprehensive constraint-driven HDI design capabilities linked to automation assisted interactive design. Comprehensive microvia class rules linked to auto-assisted via array creation and editing capabilities enable the designer to achieve desired design and productivity goals.

## Auto/interactive wirebonding

A new, highly productive environment provides fast, powerful, and flexible bondshell creation and editing. Constraint/rules-driven automatic bondfinger array placement can be used with staggered die pads, multiple bond levels, multiple bond rings, and both symmetrical and non-symmetrical designs. For fast initial what-if prototyping of single or multiple die stacks, the "autobond" feature instantly creates a symmetrical bondshell pattern including

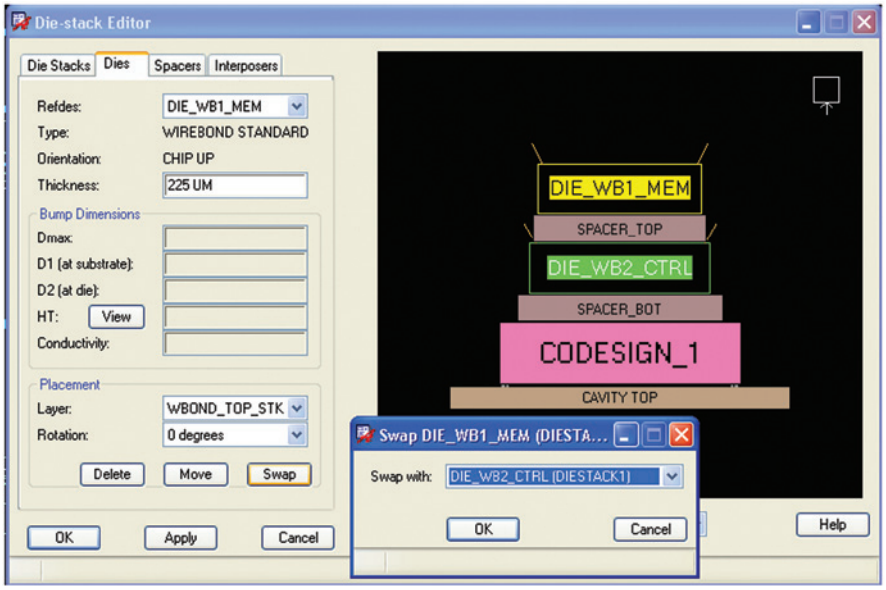


*Figure 8: 3D Die Stack Editor*

power/ground rings. Unique push-and-shove bondfinger editing enables extremely complex bondshells to be developed in minutes, delivering unparalleled capability and productivity. All of this is supported by extensive wirebond rules and constraints that provide real-time design feedback. Wirebond-attached die flags and power/ground rings can be quickly created, edited, and optimized for multiple voltage supplies. (See Figure 9.)

### 3D Design Viewer

The Cadence 3D Design Viewer is a full, solid model 3D viewer and 3D wirebond DRC solution for complex IC package designs. It allows users to visualize and investigate an entire design or a selected design subset, such as a die stack or complex via array. It also provides a common reference point for cross-team design reviews. (See Figure 10.)

### Virtual System Interconnect (VSIC) models

An integrated graphical and topological interconnect modeling and simulation capability allows designers to create and explore the SI performance of proposed system-level connectivity. Embedded simulation capability provides time and frequency domain interconnect simulation, including industry-standard S-Parameter models. An integrated (third-party supplied) 3D quasi-static field solver extracts and creates detailed, accurate geometric IBIS, RLGC, or S-Parameter models of complex 3D interconnect structures. (See Figure 11.)

### Embedded integration with third-party field solver

Seamless embedded integration with a third-party supplied 3D field solver linked to SPICE-based simulation engines within the physical SiP design environment enable modeling and simulation of package interconnect, without the time-consuming setup of standalone point tools. Engineers can quickly check tradeoffs to the physical design to ensure

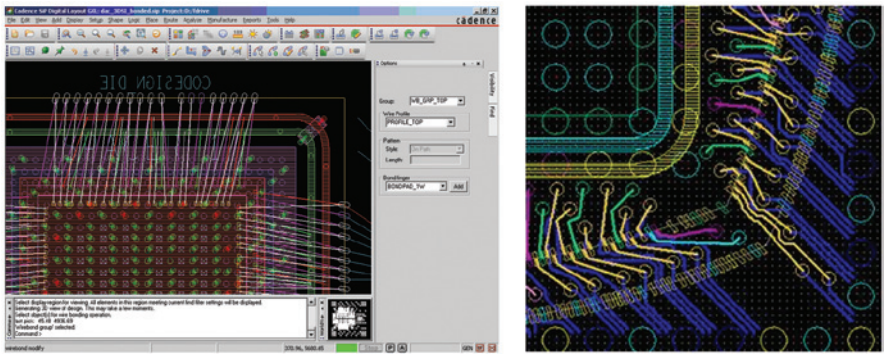

*Figure 9: Powerful auto/interactive wirebonding and bondshell breakout routing*

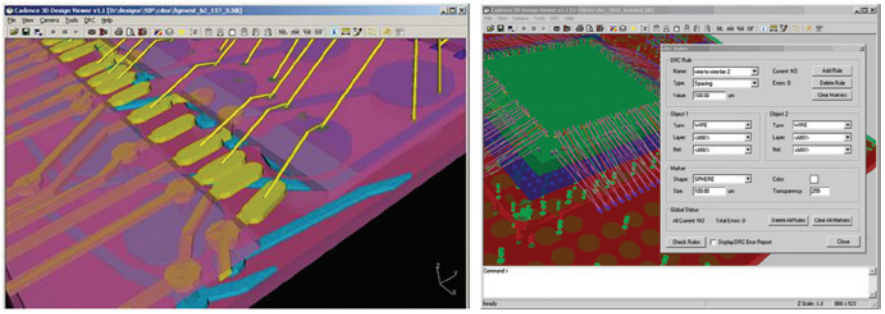

*Figure 10: 3D Design Viewer and 3D DRC*

that electrical requirements are not compromised. Extracted parasitic models can be backannotated into the top-level Virtuoso SiP schematic and testbenches for post-route circuit simulation.

### Package modeling for system-level analysis

Creation of IBIS, RLC, or Cadence DML interconnect models is easily accomplished, either for a selected set of nets or for the entire package. Design teams can then easily re-use these models at the system level to ensure that package effects are properly considered when optimizing PCB cost/performance tradeoffs.

### Integration with chip-level IR drop analysis

Creation of package power and ground RLC models that can be automatically consumed by IC core IR drop analysis (static and dynamic) is accomplished using Cadence VoltageStorm® power analysis. (See Figure 12.)

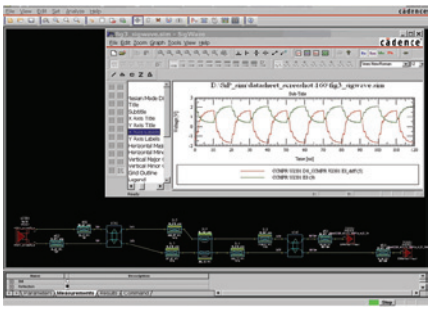

*Figure 11: Virtual system interconnect models*

## Specifications

### System requirements

- OpenGL graphics compliance with a minimum of 64MB of dedicated memory

### Platform/OS

- Windows XP, Vista Enterprise
- Solaris
- Linux

### Interfaces

- LEF/DEF 5.1 to 5.7
- OA 2.2
- Verilog® language

### Virtuoso compatibility

- 5.x for CDBA and 6.1.1 for OA

### Third-party support

- Agilent RFDE (ADS and MoMentum) for pre- and post-layout extraction and simulation
- Embedded PakSI-E 3D field solver engine from Apache-DA

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom

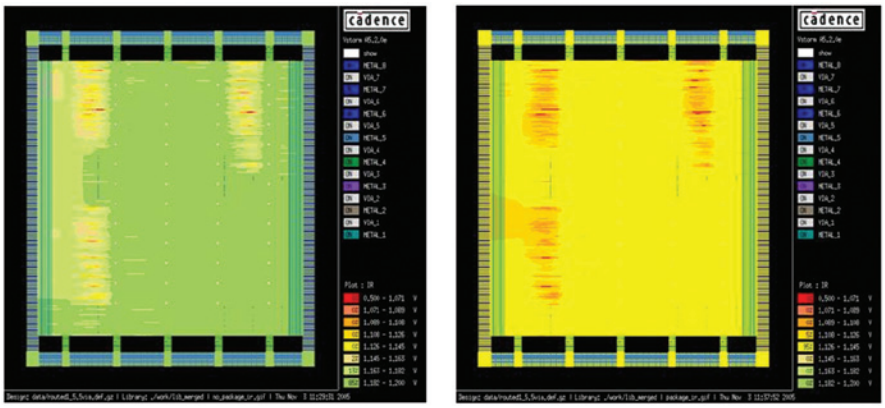

*Figure 12: Integration with VoltageStorm for chip-level IR drop analysis including the package*

- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

## Product Features

| | SiP Digital Architect GXL | SiP Digital Architect XL | SiP Digital Layout GXL | SiP Digital SI XL | SiP RF Architect XL | SiP RF Layout GXL |
|---|---|---|---|---|---|---|
| **Front-End Design Creation Features** | | | | | | |
| Virtuoso Analog Design Environment, schematic/ layout integration and flow | | | | | • | |
| Substrate-level embedded RF passive synthesis | | | | | • | |
| System Connectivity Manager with logical co-design objects | • | • | | | | |
| Full SiP LVS (substrate and ICs) | • | • | | | • | |
| Parasitic back annotation into system-level test benches | | | | | • | |
| **Signal Integrity Features** | | | | | | |
| SigXplorer topology editor and simulator (pre-route capabilities) | • | | | • | | |
| SigXplorer topology editor and simulator (pre- and post-route capabilities) | | | | • | | |
| S-Parameter interconnect modeling and SI simulation | • | | | • | | |
| Source synch and serial interface simulation | • | | | • | | |
| 3D PCB full-package simulation model creation | • | | • | • | | • |

## Product Features (continued)

| | SiP Digital Architect GXL | SiP Digital Architect XL | SiP Digital Layout GXL | SiP Digital SI XL | SiP RF Architect XL | SiP RF Layout GXL |
|---|---|---|---|---|---|---|
| Embedded integration with a (third-party supplied) 3D field solver | • | | | • | | |
| Co-planar coupling extraction | • | | | • | | |
| Spectre transistor-level simulation engine | • | | | • | | |
| Channel analysis for high-capacity SI simulation | • | | | • | | |
| Power Delivery Network (PDN) optimization & verification | | | | • | | |
| Etch back stub effects simulation | • | | | • | | |
| Package/pin delay length report | • | | • | • | | • |
| **Substrate Design Features** | | | | | | |
| Import/export APD (.mcm) database | • | | • | | | • |
| Auto/interactive wirebonding including rapid autobond | • | | • | • | | • |
| User-definable wirebond model profiles including XML import | • | | • | • | | • |
| Full and partial design connectivity assignment and optimization (router-based, closest match, interactive and constraint-based) | • | | • | • | | • |
| Interactive and automatic interconnect routing (free angle and multi-layer orthogonal) | • | | • | • | | • |
| On-line soldermask checking | | | • | | | • |
| Recursive breakout pattern creator (flip-chip and wirebond) | • | | • | | | • |
| Static-style screen rulers | | | | | | • |
| **Advanced Design Features** | | | | | | |
| I/O planning co-design editor (using LEF/DEF and OA 2.2) | • | | • | | | • |
| Hierarchical GDSII output | | | • | | | • |
| Team-based design (Design partitioning) | | | • | • | | • |
| Embedded RF passive creation and editing | | | | | | • |
| 3D Design Viewer and 3D wirebond DRC | • | | • | • | | • |
| 3D Die Stack Editor | • | | • | | | • |
| Interconnect cline spreading | | | • | | | • |
| BGA editor | • | | • | • | | • |
| Constraint-driven HDI design | • | | • | • | | • |
| **DFM Preparation/Output** | | | | | | |
| Die/BGA footprint compare using DEF/OA/.TXT | • | | • | | | • |
| Filled shapes (metal) creation and editing | | | • | • | | • |
| Design documentation (dimensioning, annotation) | | | • | | | • |
| Assembly Rule Checking (ARC) system | | | • | | | • |
| Etch back of plating traces | | | • | | | • |
| Plating bar generation | | | • | | | • |
| Manufacturing/documentation export/import capabilities (stream, dxf, AIF) | | | • | | | • |
| Substrate mask output (Gerber, GDSII) | | | • | | | • |
| Full design-status reporting capabilities | • | | • | • | | • |
| Waived DRCs (creation and reporting) | • | | • | • | | • |
| Degassing of filled metal shapes | | | • | | | • |
| Thieving (metal area balancing) | | | • | | | • |

cadence®

Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com