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CAE Flow in the Development for the Digital Equipments

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- CAE Flow for PCB Design
- Chip / Package / PCB Modeling

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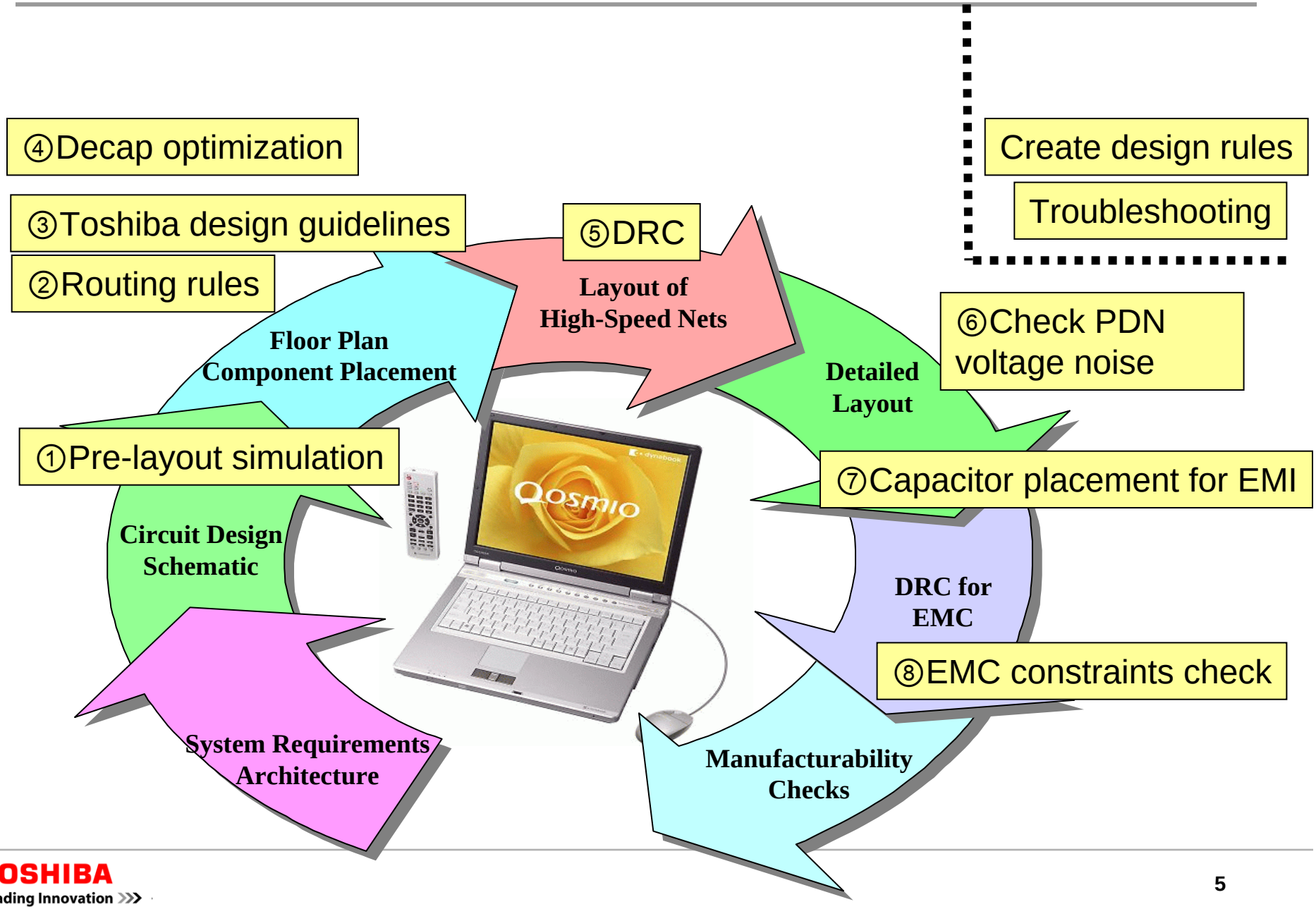
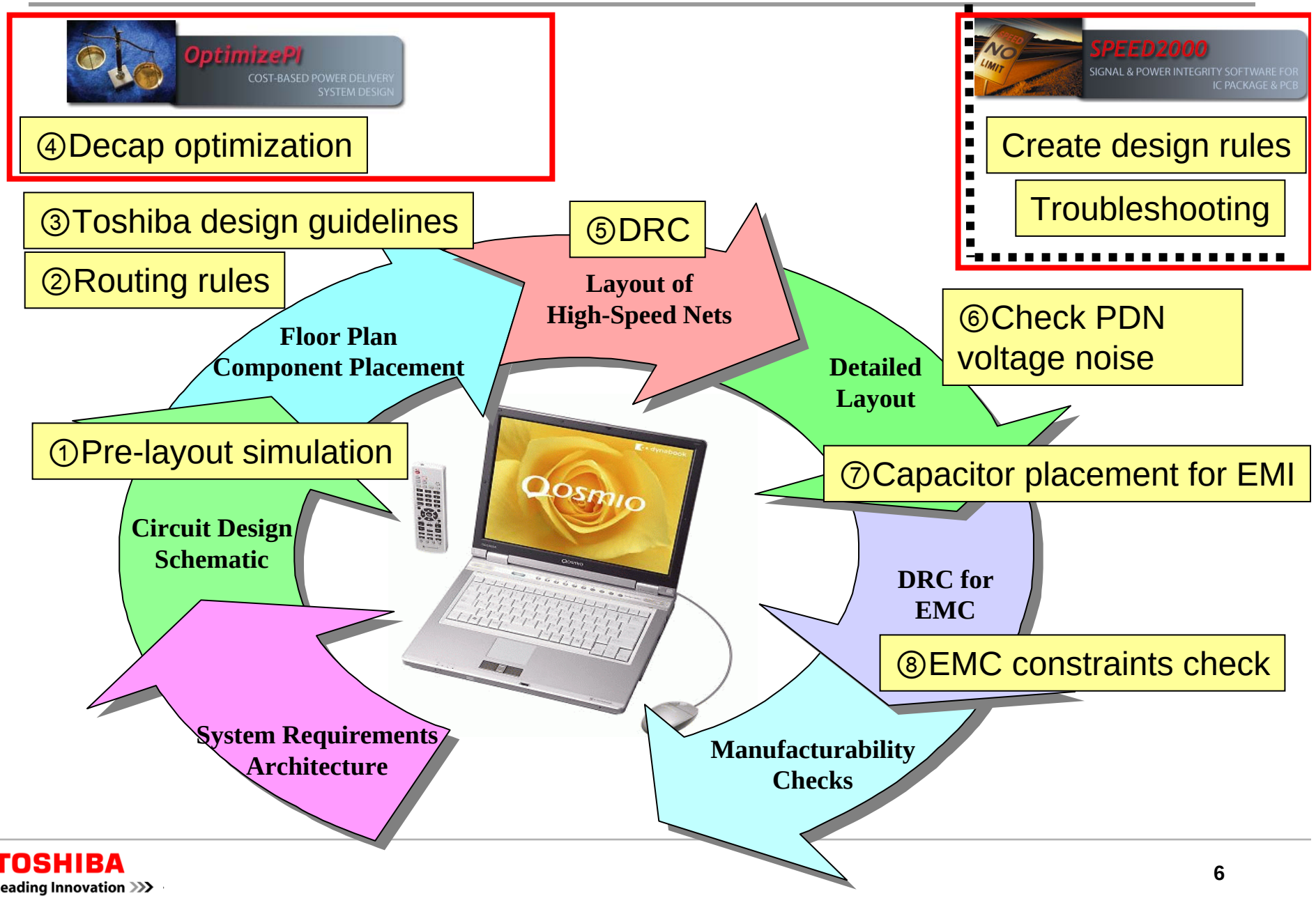
PCB Design Flow

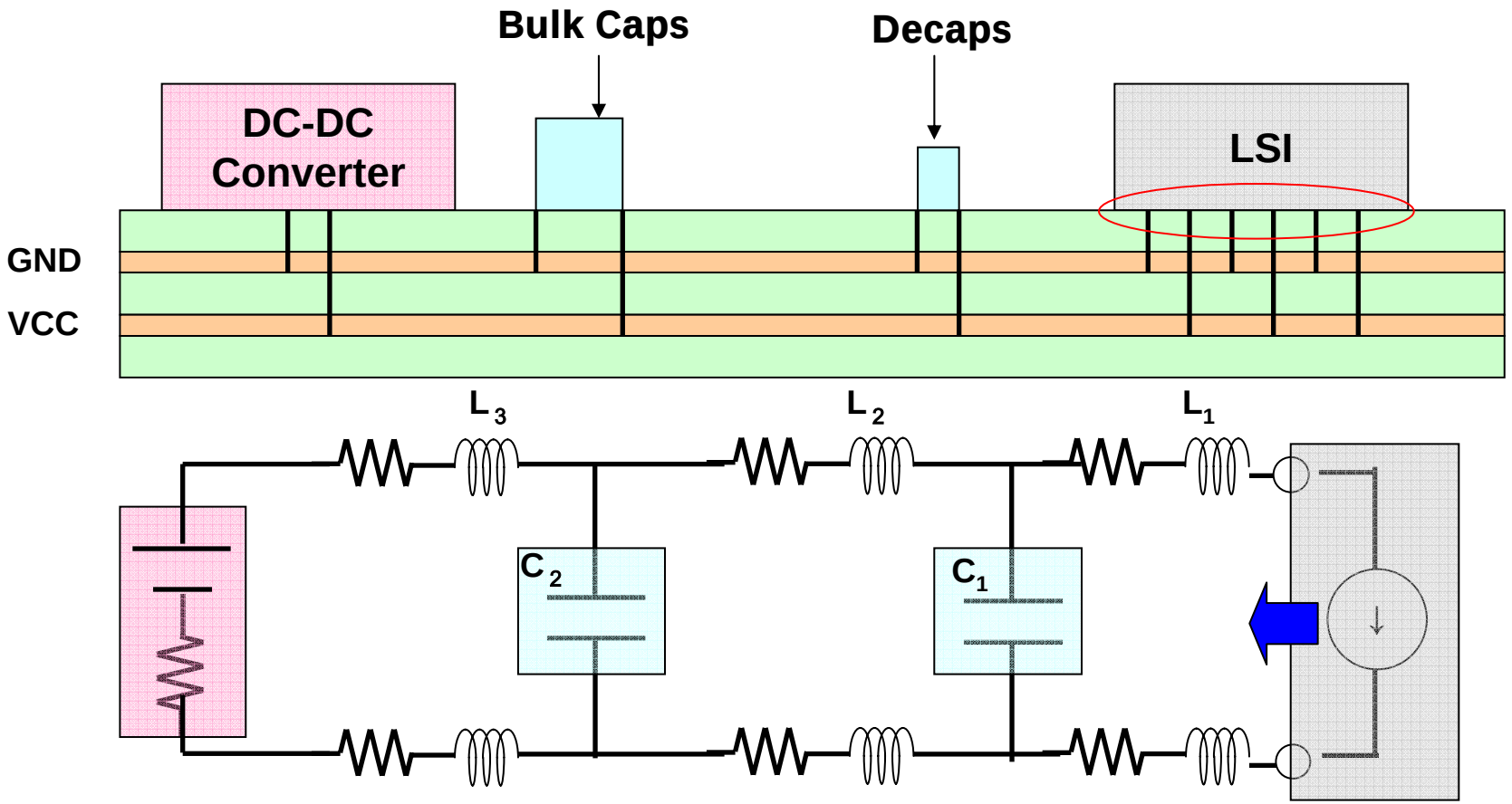
PCB Design Flow



PCB Design Flow



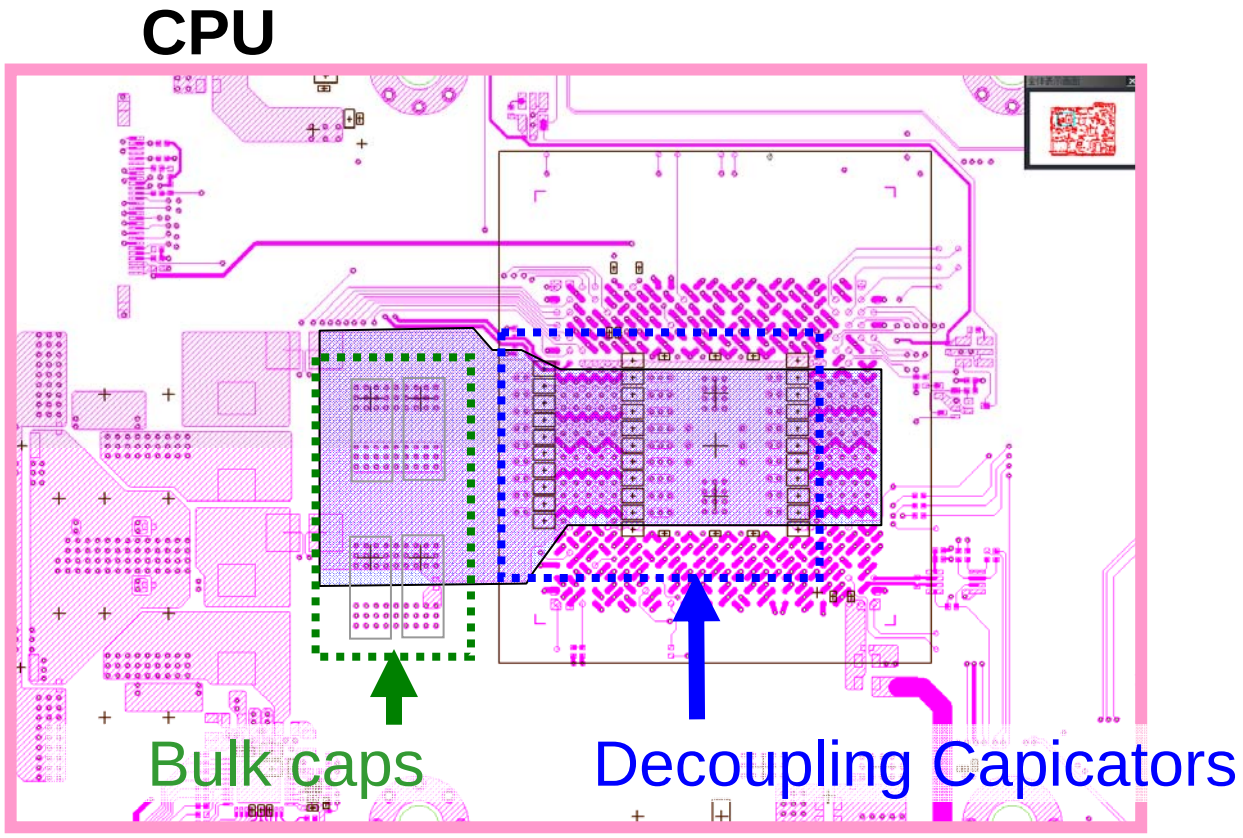
Case Study for Decap Optimization



Observation of PDN impedance

< Typical Methodology (before OptimizePI) >

1. Identify decap placement locations from CPU supplier specifications



2. Pickup possible decap combinations based on Design of Experiment approach (1 hour for this design)

Bulk caps

Decaps

大容量コンデンサ				デカップリングコンデンサ																																	
1	2	3	4	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
A	0	A	A	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B	B	B	0	0	B	0	B
A	A	0	A	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B	B	B	0	0	B	0
0	A	A	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B	B	B	0	0	B
0	0	A	A	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B	B	B	0	0
A	0	0	A	B	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	0	B	B	B	0	B
0	A	0	0	B	B	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B	B	B
A	0	A	0	0	B	B	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B	B
0	A	0	A	0	0	B	B	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B	B	B	0	B
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A	A	A	0	0	B	0	B	0	0	B	B	0	B	B	0	B	0	B	B	0	0	0	B	0	0	0	0	0	B	B	B	0	B	0	0	0	B	B	B
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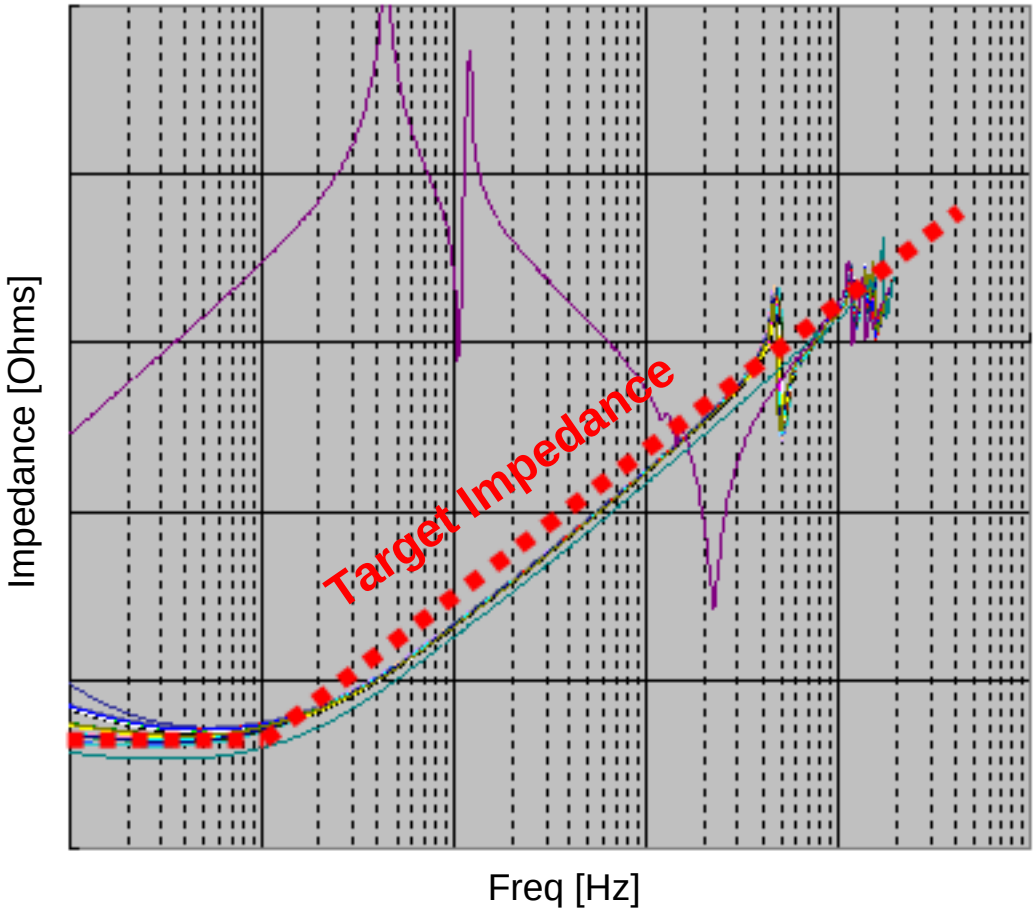
C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C

45 identified possible schemes

3. Simulation of impedance for all 45 combinations one by one.
   (1 hour per combination. This takes about 45 hours in total.)



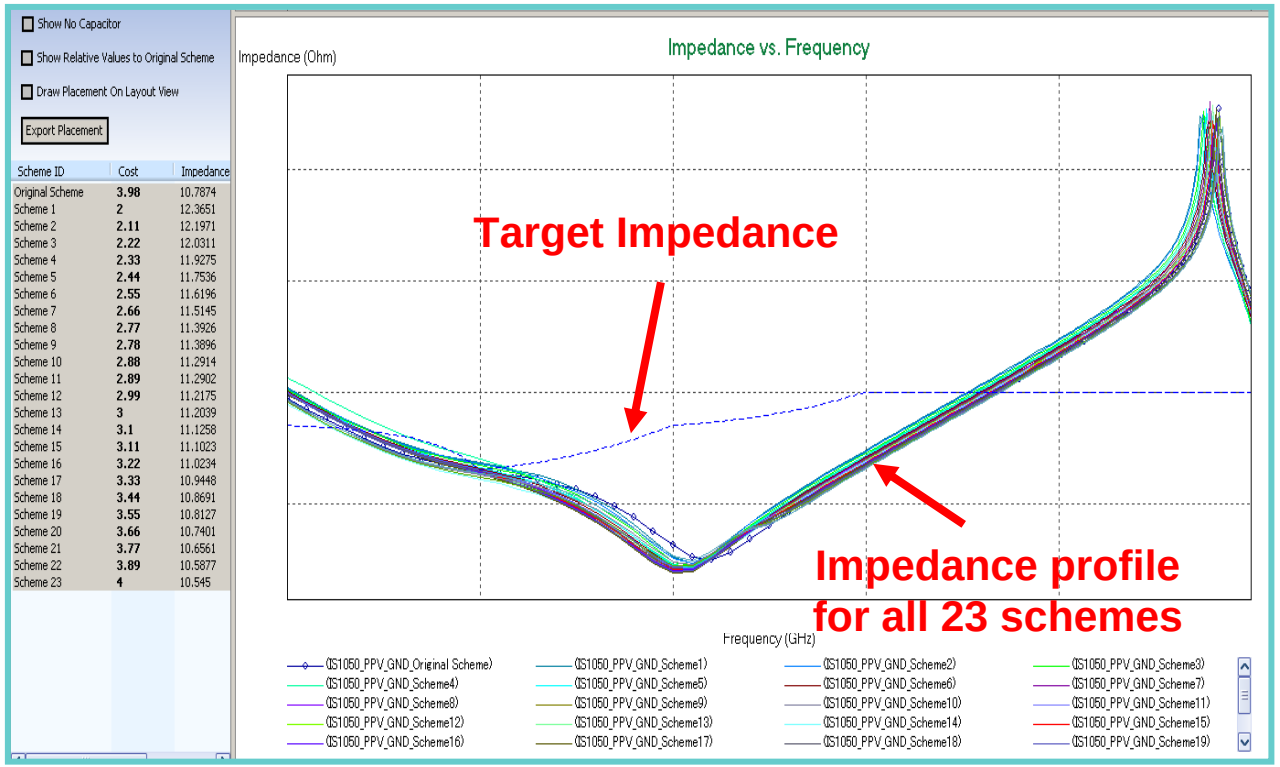
4. The best scheme, based on performance and cost, is identified by engineers. (This typically takes 4 hours.)

A typical project takes 50 hours for decap optimization.

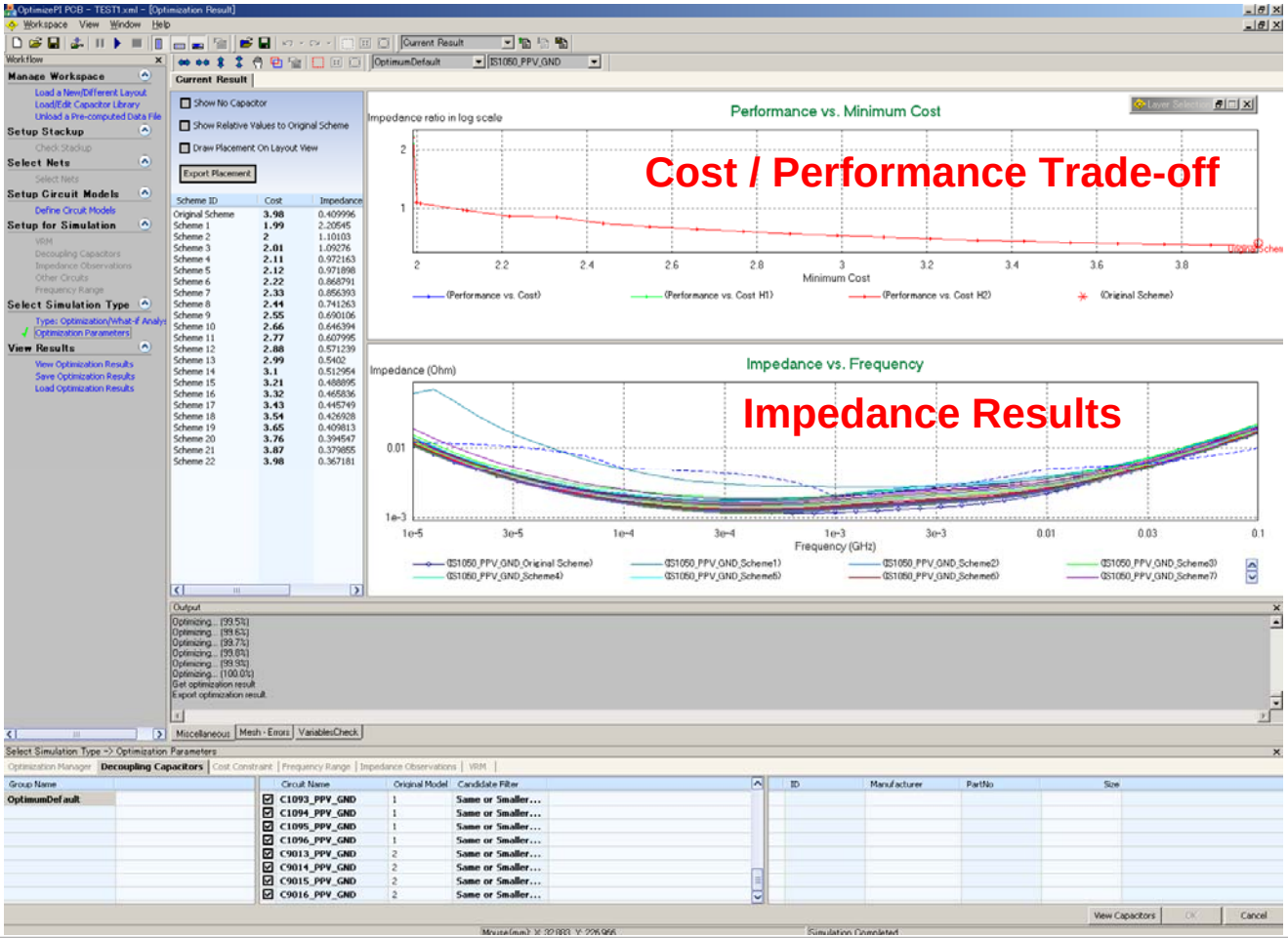
< OptimizePI
is now used instead >

1. Automatically identify the best scheme in 1 hour.

Extract
23 optimized
schemes



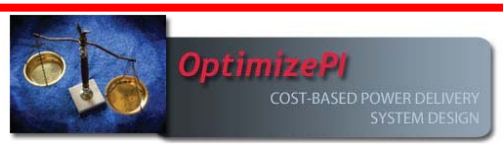
2. Result with OptimizePI enables engineer to quickly select the best scheme from the 23 candidates



OptimizePI gives results in 1 hour compared to 50 hours Toshiba spent before.

It is also important that Toshiba's basic flow is the same. OptimizePI adoption does not require a flow change.

OptimizePI results match with prior method for accuracy.



50H→1H

④Decap optimization

SPEED2000
SIGNAL & POWER INTEGRITY SOFTWARE FOR
IC PACKAGE & PCB

Create design rules

Troubleshooting

③Toshiba design guidelines

②Routing rules

⑤DRC

Layout of High-Speed Nets

⑥Check PDN voltage noise

Floor Plan Component Placement

Detailed Layout

①Pre-layout simulation

⑦Capacitor placement for EMI

Circuit Design Schematic

DRC for EMC

⑧EMC constraints check

System Requirements Architecture

Manufacturability Checks

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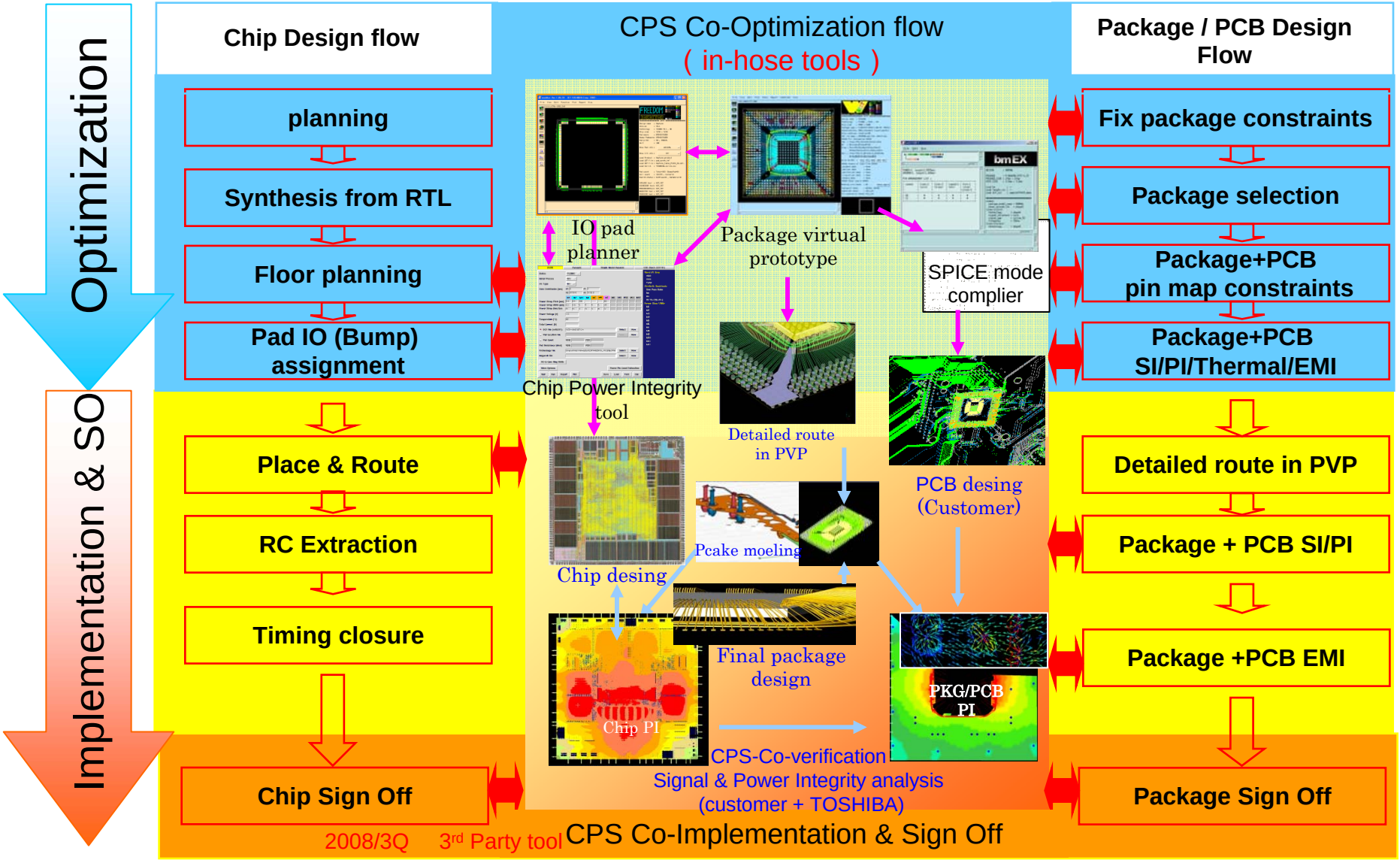
- Chip / Package / PCB Modeling

Methods to determine the target impedance for PDN optimization

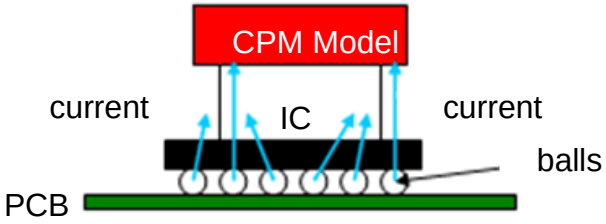
- LSI vendor provides – We use their information.

- LSI vendor doesn't provide – We make our own calculations.

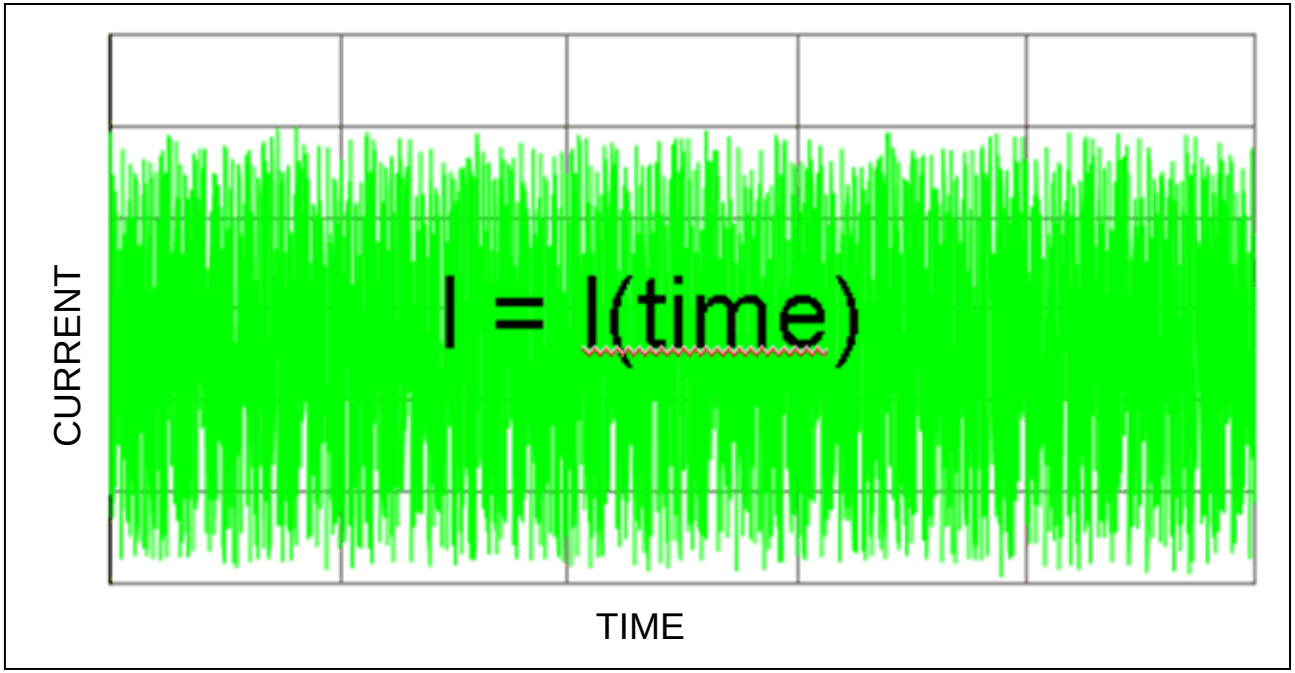
CAE Effort by Semiconductor group at Toshiba



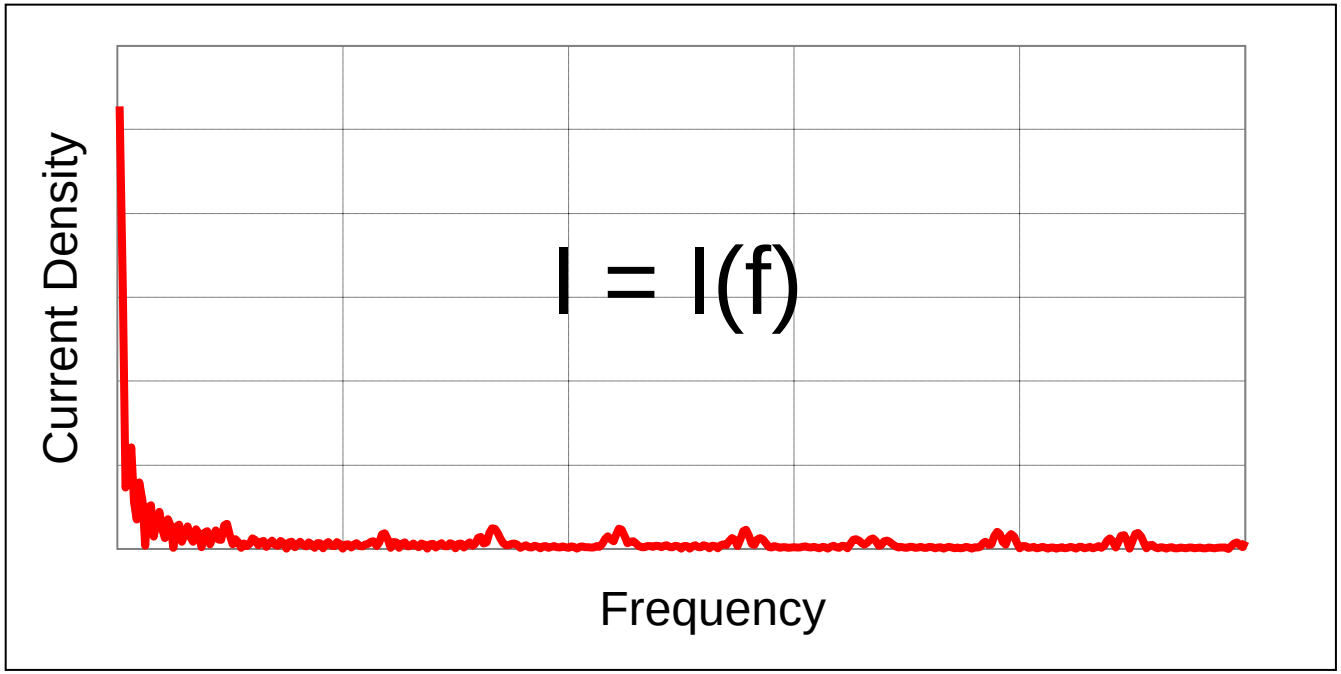
Nikkei Microdevices August, 2008



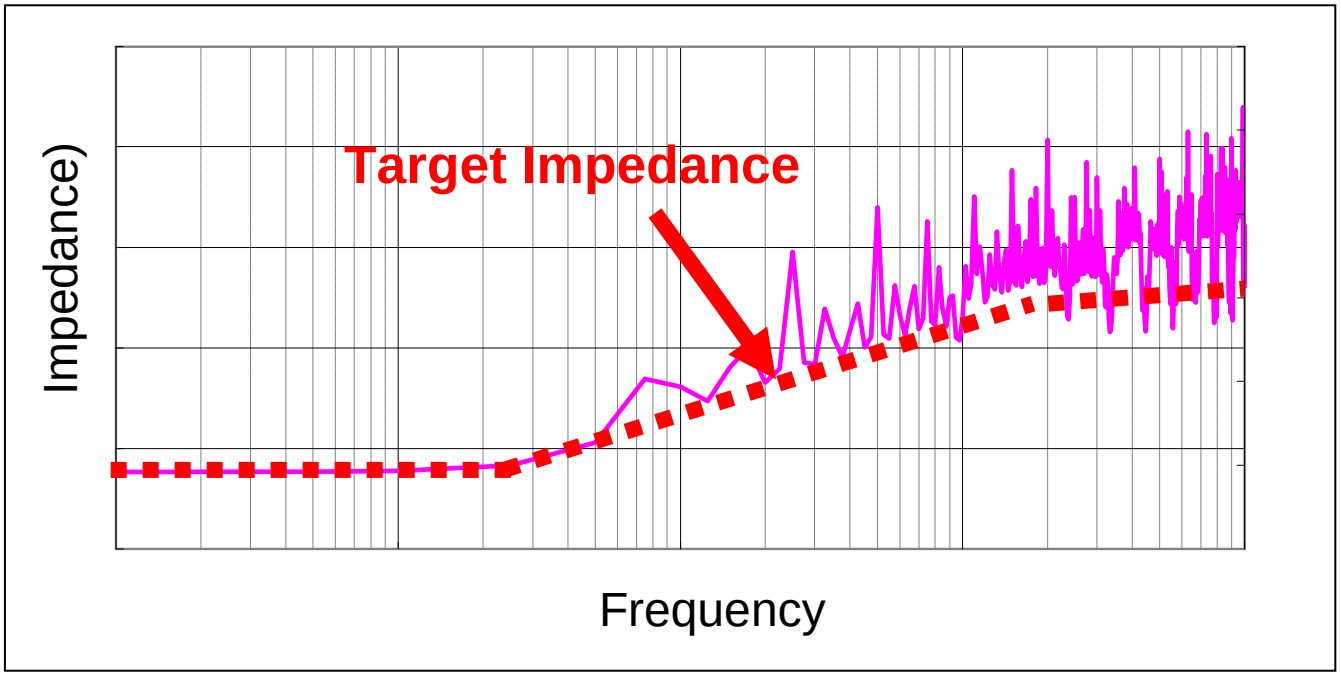
The total chip power current is extracted from all the power pin current observations.



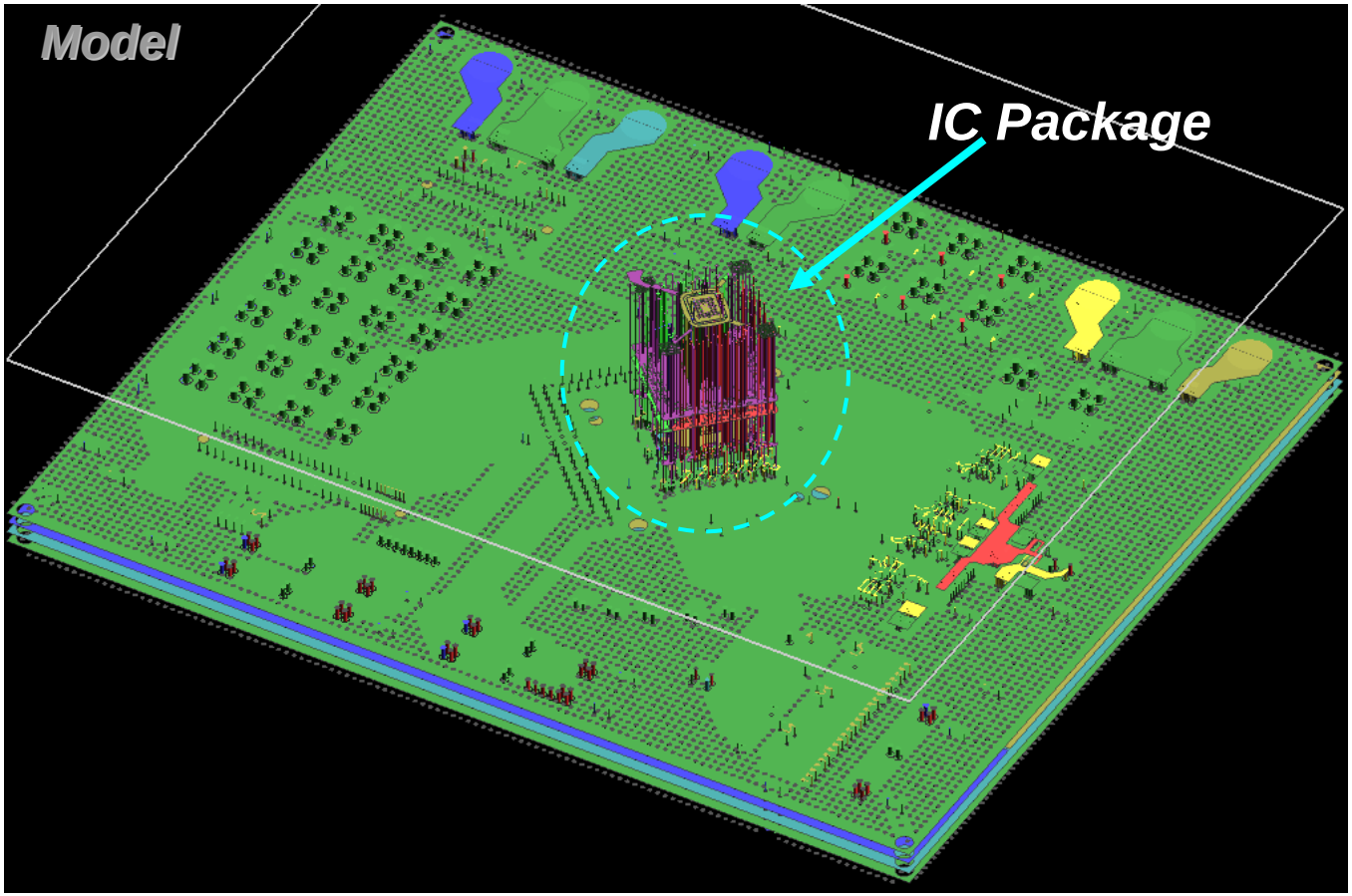
CPM (Chip Power Model)
includes parasitic of entire chip power delivery network

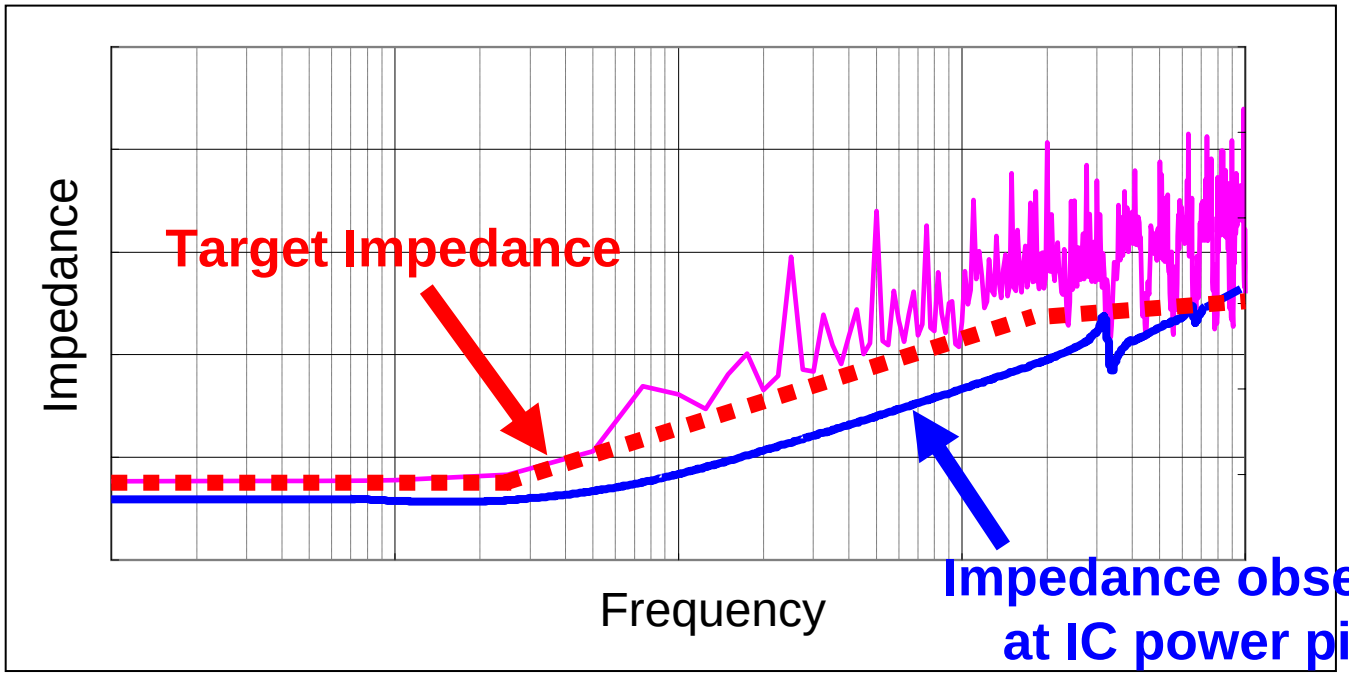


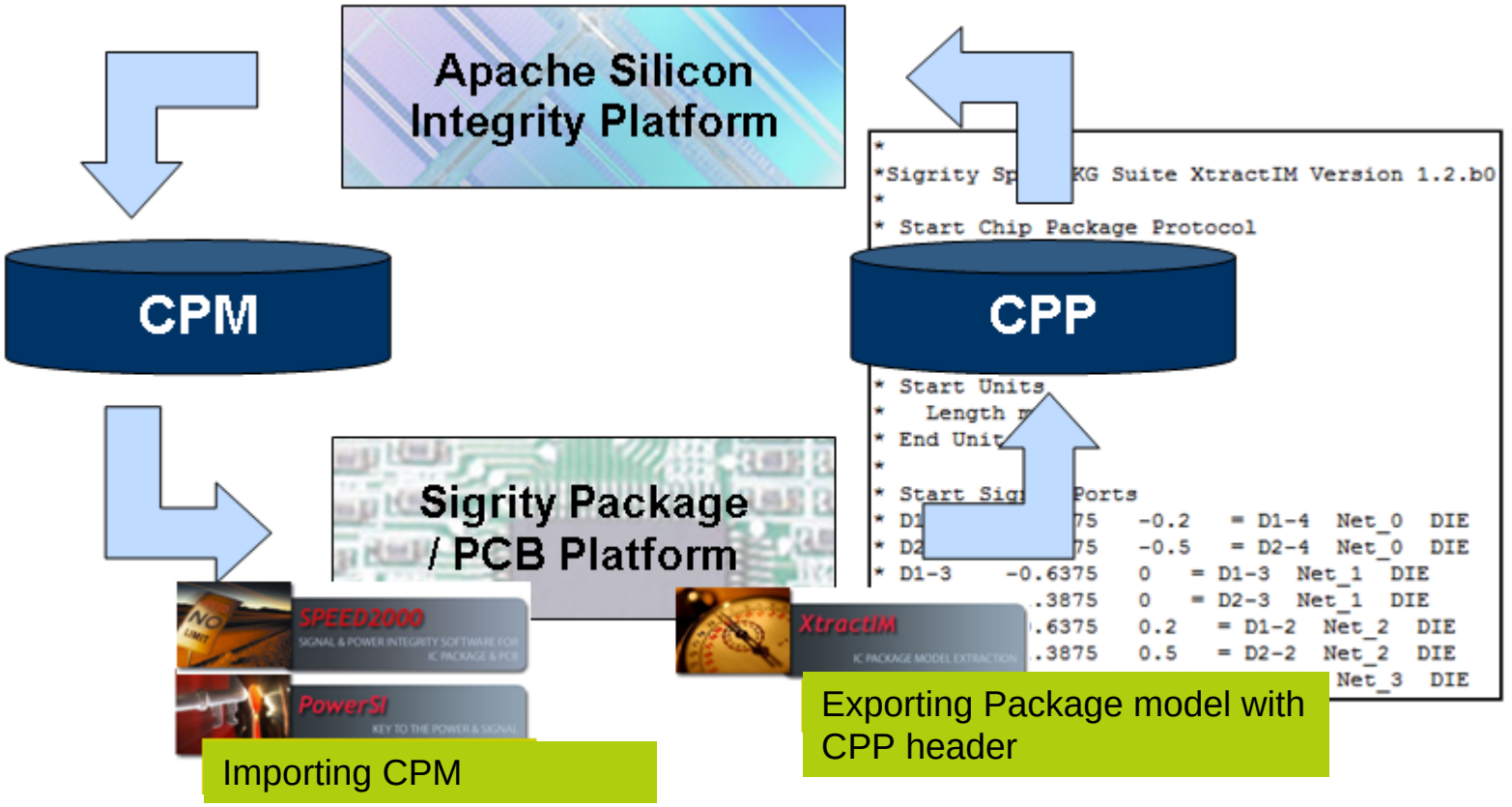
Fourier transform of CPM current waveforms



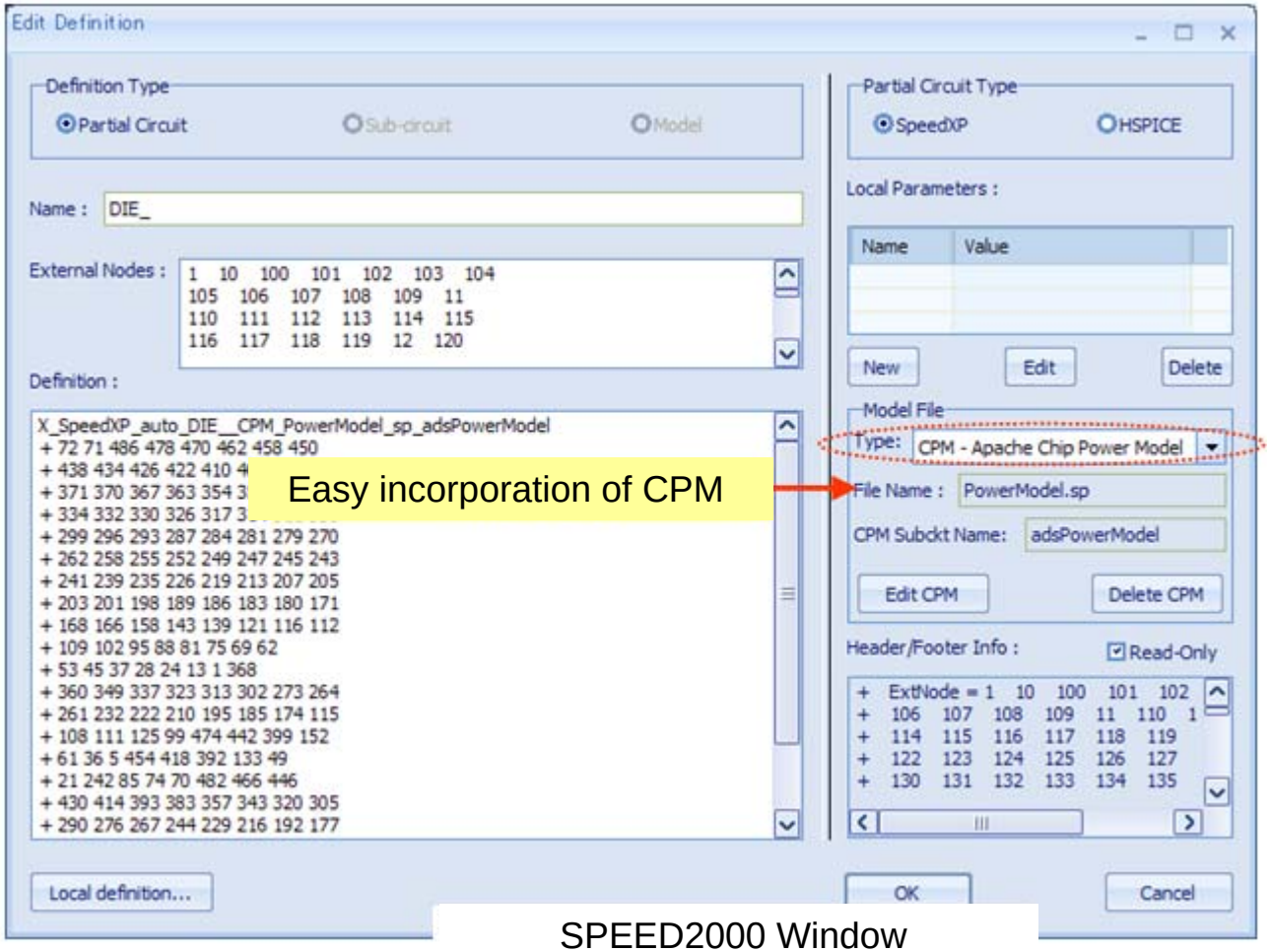
The current spectrum in frequency domain is used to calculate target impedance.


Model
IC Package


Impedance
Target Impedance
Frequency
Impedance observed
at IC power pins

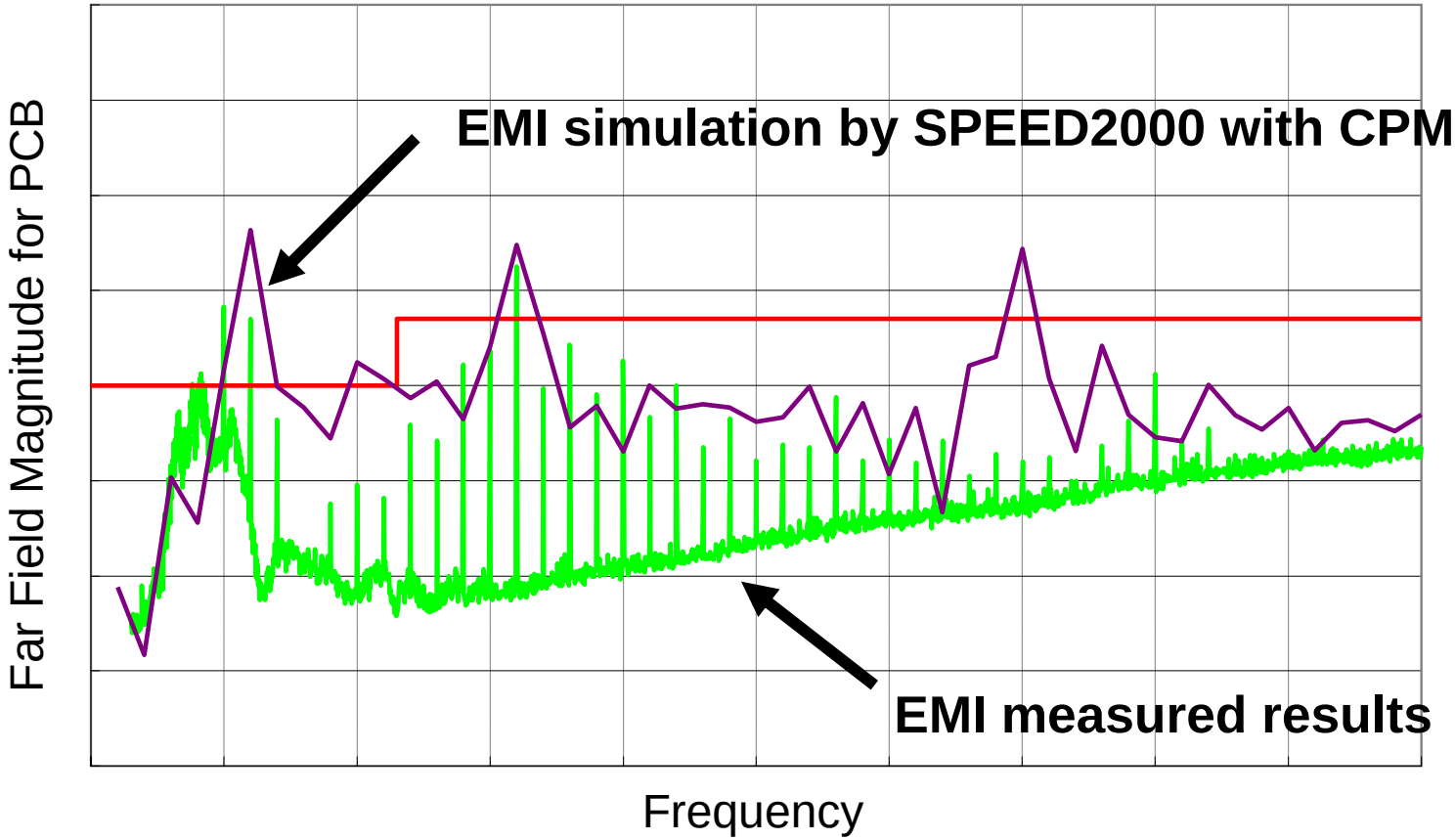


CPM and SPEED2000 used together



SPEED2000 Window

Using CPM Model in SPEED2000



CPM model used as a noise source in SPEED2000 simulation.
Far Field results show good correlation to measurements.

Summary

- CAE Utilization in PCB Design

  - Decap optimization flow with **OptimizePI**

  - **CPM** can help in calculating target impedance

  - **CPM** can be used with **SPEED2000** for EMC analysis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