UBM

LEARN HOW TO TURN SIMULATION INTO REALITY FOR PAM4 ANALYSIS

Sarah Boen, Tektronix
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SPEAKERS

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Sarah Boen is a Marketing Manager, specializing in solution strategy at Tektronix. She has worked at Tektronix in various roles for over 15 years; including Product Planning, Program Manager, and Software Design Engineer. She has an MBA and BSCS from the University of Portland.

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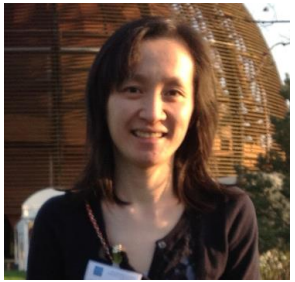

Xiaolan Wang is a DSP design engineer at Tektronix. Her research include high-speed data integrity characterization and signal analysis methodologies. She received her Ph.D. in Electrical Engineering and M.S. in Statistics from Johns Hopkins University.

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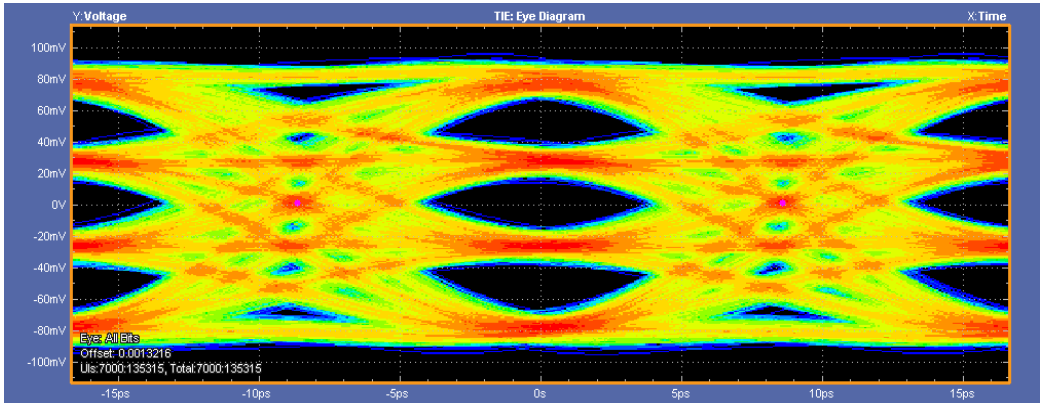
Ken Willis is the Product Engineering Director of High Speed Analysis Products at Cadence Design Systems. He has 25 years of experience in the modeling, analysis, design, and fabrication of high-speed digital circuits. Prior to Cadence, Ken held engineering, marketing, and management positions with the Tyco Printed Circuit Group, Compaq Computers, Sirocco Systems, Sycamore Networks, and Sigrity.

AGENDA

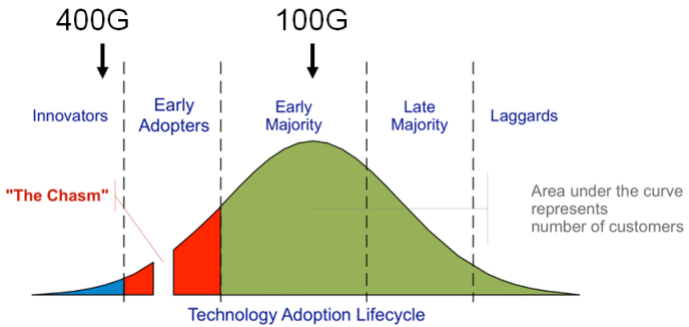
- **Introduction to PAM4**
  - Why Now
  - PAM4 vs. NRZ
- **Measurement Basics**
  - New PAM4 Measurements
  - Clock Recovery
  - Equalization and IBIS-AMI
- **PAM4 in Simulation and Measurement**
  - Measurement and Simulation Results



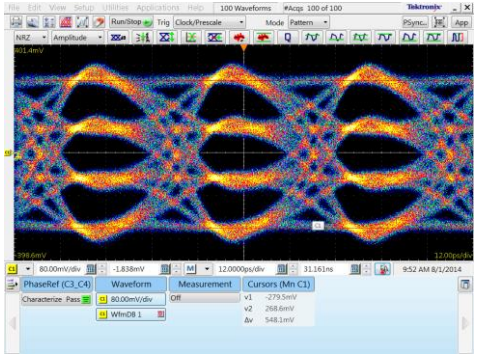
WHY PAM4 NOW?

- Commercially viable backplanes operating up to 56 GBd is the driver for PAM4
  - 1M Backplane (note KP4) <-40dB of loss @ 13GHz, barely supportable at 100G
  - Doubling of speed pushes backplanes into -70dB loss profiles; Higher order levels of modulation are the most effective way forward
- Interconnect single mode optics and CDAUI are amenable to 56 GBd, due to the relatively low loss and dispersion
  - Adopting PAM4 to maintain the same format and prevent conversion
- Multi-mode optics, not likely a candidate for PAM4 at 56 GBd
  - Development will lag single mode rollouts and not impact PAM4 adoption

CEI 3.0	802.3ba : (100G LR4/ER4)	25.78Gbps
KR4	802.3bj : (100G KR4/CR4/KP4)	25.78Gbps
CAUI4	802.3bm: (100G SR4)	25.78Gbps
CEI 3.1 / CDAUI-8	802.3bs : (400G DR4/LR8)	56Gbps/25.78Gbps

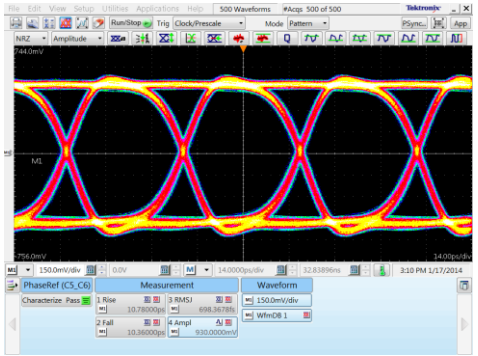


WHAT ARE THE DIFFERENCES BETWEEN PAM4 and NRZ?



PAM4

VS.



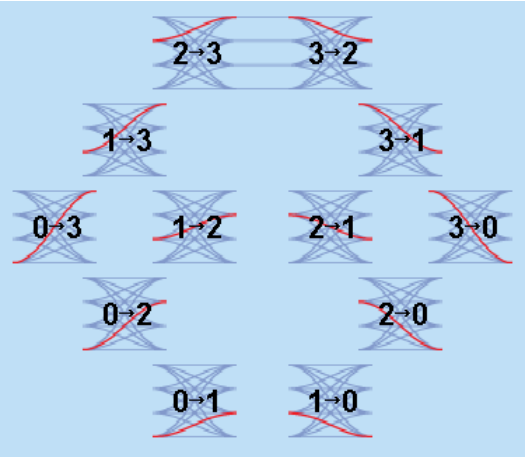
NRZ

- 4 Levels → 3 Eyes
- Sensitive to SNR (eyes smaller)
- 2 bits into 1 UI
- ½ Baud Rate for same data throughput (28 GBd = 56 Gbps)
- Additional complexity/cost to TX/RX

- 2 Levels → 1 Eye
- Less sensitive to SNR
- 1 bit in 1 UI
- 1X Baud Rate for same data throughput (28 GBd = 28Gbps)
- Less expensive TX/RX

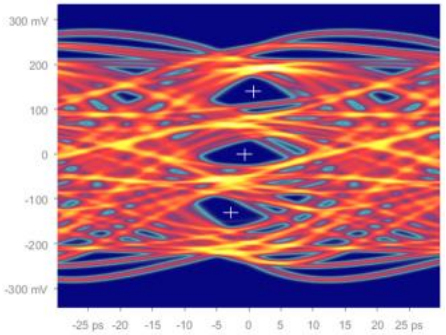
NEW MEASUREMENTS & TECHNIQUES

Measurements Per Transition Type



Example: Rise & Fall Times

Relative Eye Position Measurements



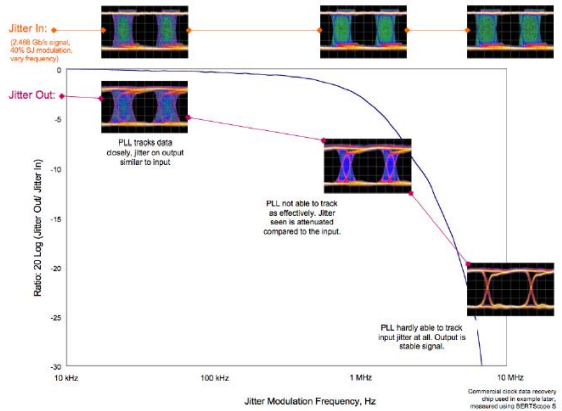
- Vertical Linearity
- Horizontal Offset

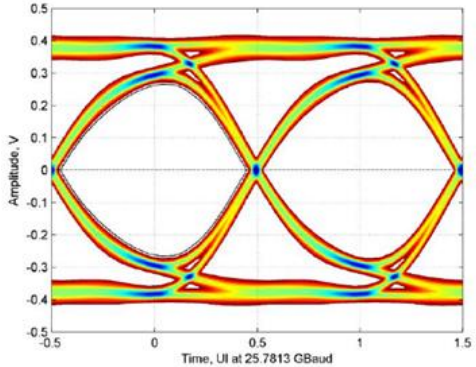
Clock Recovery Options

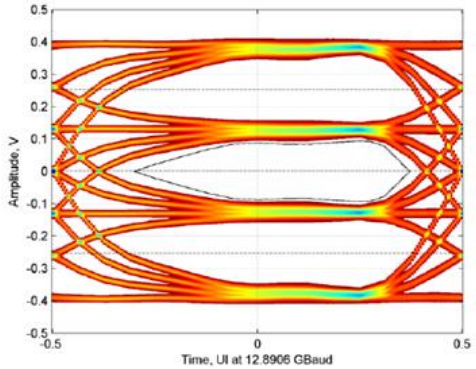
- “Conventional” ?
- Selected Edges ?
- Noise-Tolerant ?
- IBIS Model ?
- Spec-Compliant ?

PAM4 CLOCK RECOVERY

- To extract clock and bit sequence from embedded data streams
  - Required for equalization (DFE), jitter/noise decomposition and characterization







- Clock extraction in presence of multiple levels and transitions

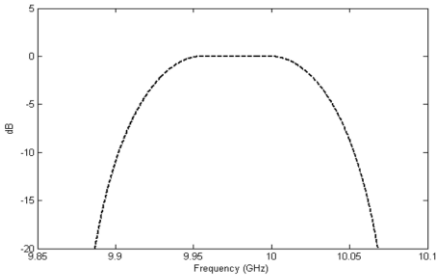
UBM

Clock Recovery for Signals with Spread Spectrum Clock Through Lossy Channels

Kan Tan, (Tektronix Inc.)

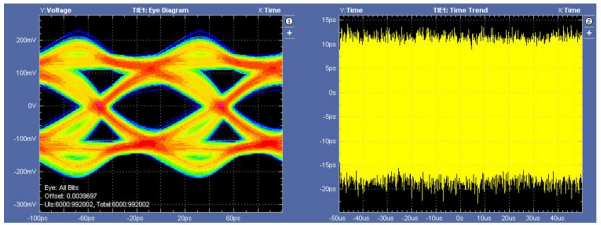
Improved Software Clock Recovery

- Use the Spectral line approach to get clock spectrum. Apply Tukey window to clean up the clock spectrum.
- Then convert to time domain. Then use the edge crossing based PLL to get the recovered clock.



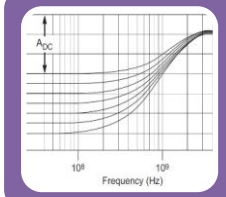
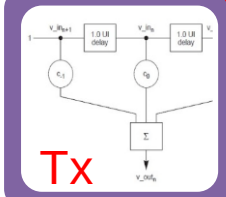
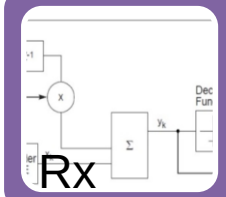
Clock Recovery Removes SSC

- Spectral line approach works well with signals through lossy channels.
- Edge crossing based PLL works well in tracking out low frequency SSC jitter.
- The combined approach tracks out the signals with SSC through lossy channels.



Thursday, January 21
2:50 PM – 3:30 PM
Ballroom B

PAM4 EQUALIZATION

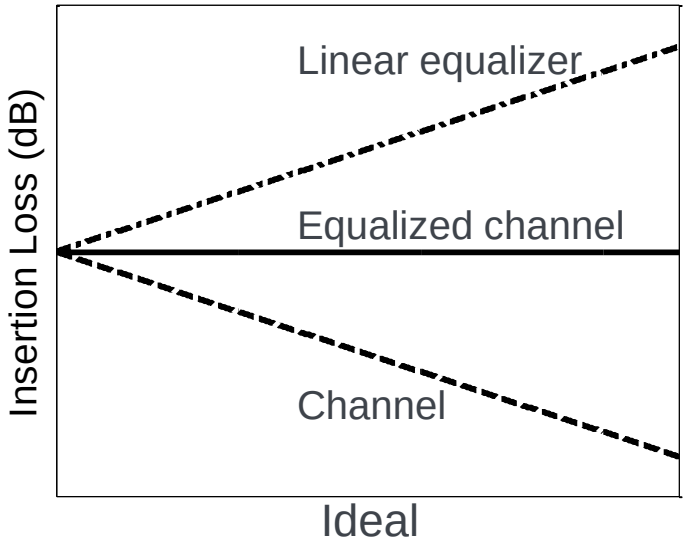
	Applied Signal	Time Domain	Frequency Domain	Impulse Response
 Continuous Time Linear Equalizer (CTLE)	Analog	Continuous	Infinite	IIR
 Feed Forward Equalizer (FFE)	Analog	Discrete	Nyquist	FIR
 Decision Feedback Equalizer (DFE)	Digital	Discrete	N/A (Nonlinear)	N/A (Nonlinear)

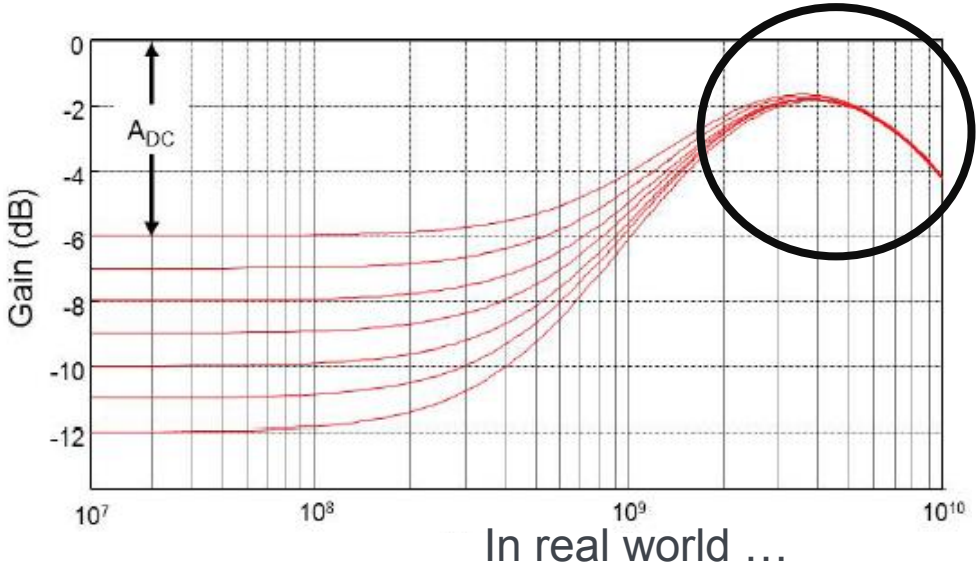
Tx

Rx

LIMITATION OF LINEAR EQUALIZER

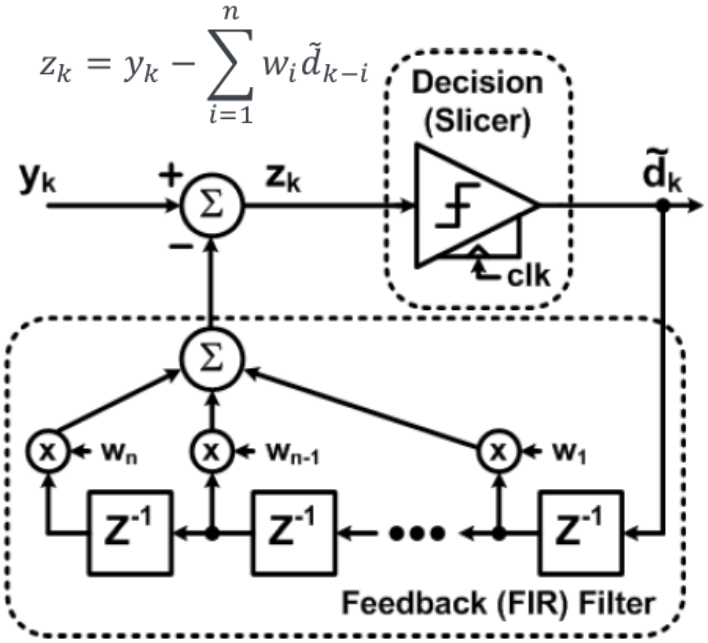
- Linear equalizers (CTLE, FFE) attempt to “invert” the channel
- But must damp down at high frequency to suppress noise → **Residual ISI**





NONLINEAR EQUALIZER

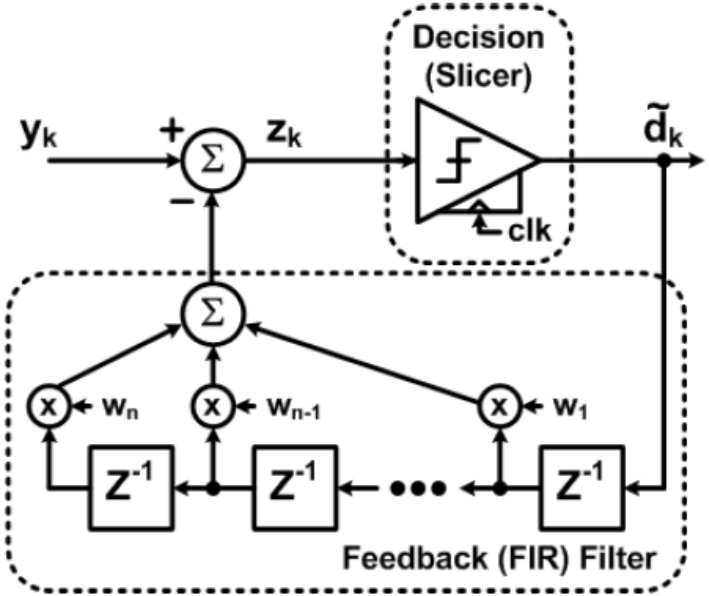
- Decision feedback equalizer (DFE)
  - ***Pros***
    - Compensate high frequency channel response w/o noise amplification
    - Remove postcursor ISI
  - ***Cons***
    - Does not remove precursor ISI
      - ***Solution***: Combine with FFE
    - Potential error propagation from bit error
      - ***Solution***: Efficient CTLE and CDR design



http://www.ece.tamu.edu/~spalermo/ecen689/lecture19_ee689_rx_dfe_eq.pdf

PAM4 DFE

- Unlike linear equalizer, DFE requires re-design and new considerations for PAM4
- Signaling-aware slicer and constellation
  - NRZ vs. PAM-4 requires different decision algorithms
- Self-adaptive optimization
  - DFE coefficients tuned from measurements alone
  - No back-channel needed



http://www.ece.tamu.edu/~spalermo/ecen689/lecture19_ee689_rx_dfe_eq.pdf

SIMULATION VS MEASUREMENT

- Traditionally two separate worlds
  - Simulate from the office and measure in the lab
- Today measurement “probe points” are not accessible
  - Equalization takes place inside the chip for multi-gigabit devices
  - Measurement equipment must simulate equalization to demonstrate if the data can be recovered
- Does it make sense to be simulating using different techniques?
  - NO !

CONSIDERATIONS FOR CORRELATION

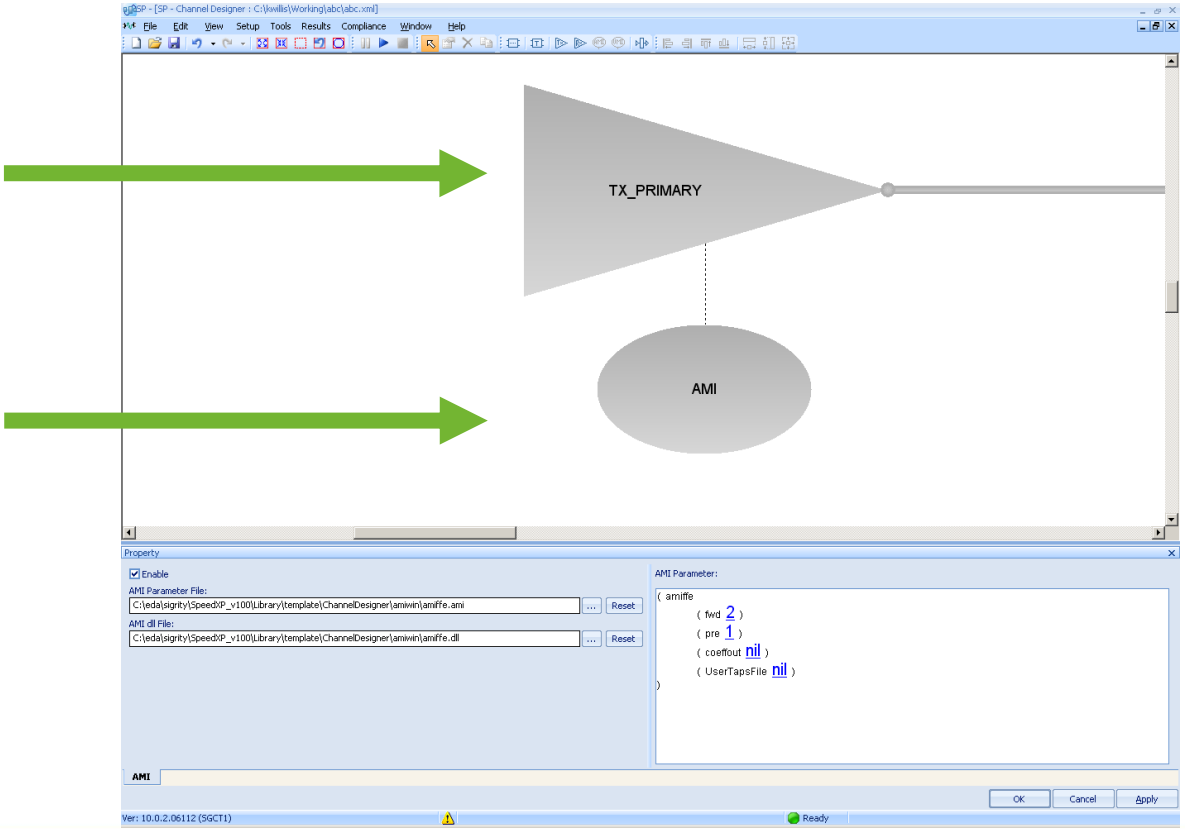
- Lab measurements have artifacts not typically present in simulation
  - Cables and connectors
  - Test equipment: Scopes, probes, …
- Simulation must model these or they must be removed from measurements
  - Models for simulation available from test vendor or can be measured directly
- Receiver models can impact results
  - IBIS-AMI provides a standard method for RX equalization

AMI → ALGORITHMIC MODELING INTERFACE

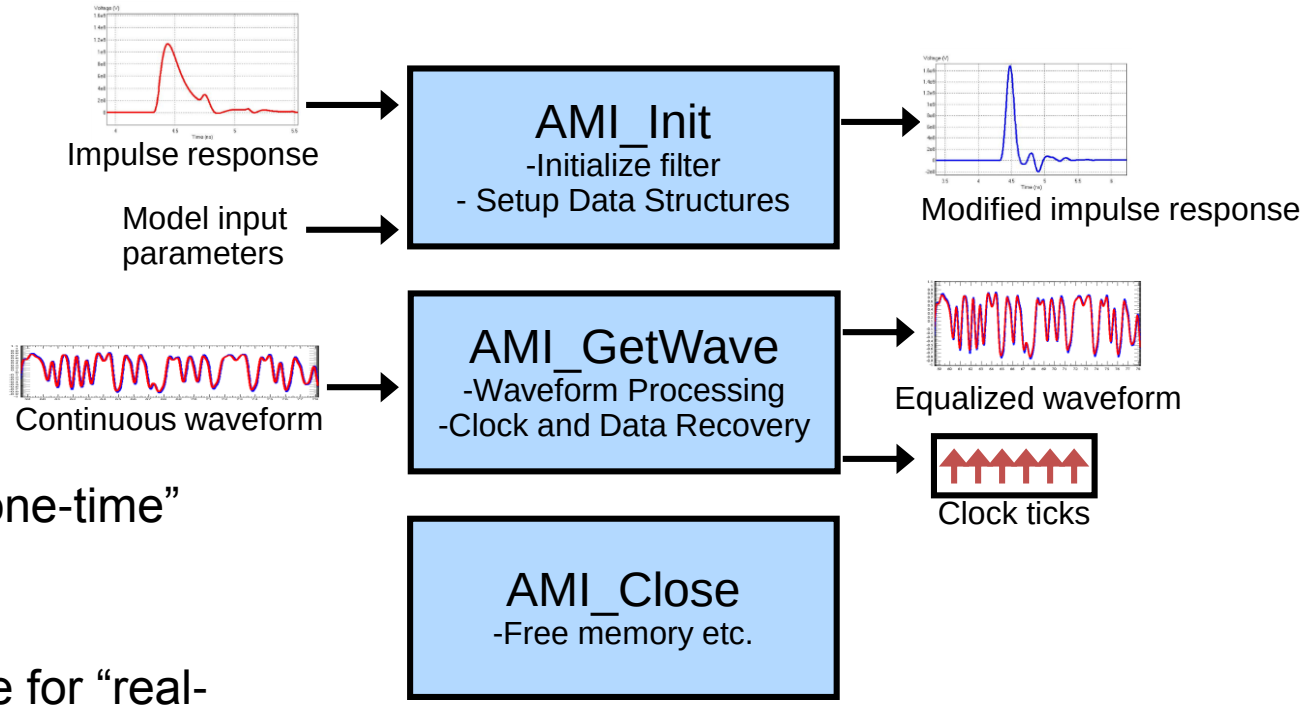
- Extension made to IBIS in 2007
- Enables software-based, algorithmic models to work together with traditional IBIS circuit models
- Enables SerDes equalization algorithms to be modeled and used during channel simulation
- IBIS-AMI enables plug-and-play simulation compatibility between SerDes models from different suppliers, in a standard commercial EDA format

IBIS-AMI → MODEL SUBCOMPONENTS

- Circuit component
  - I/O buffer stage
  - Voltage swing
  - Parasitics
  - SPICE or traditional IBIS format
- Algorithmic component
  - On-chip
  - Equalization functionality
  - DLL + AMI file



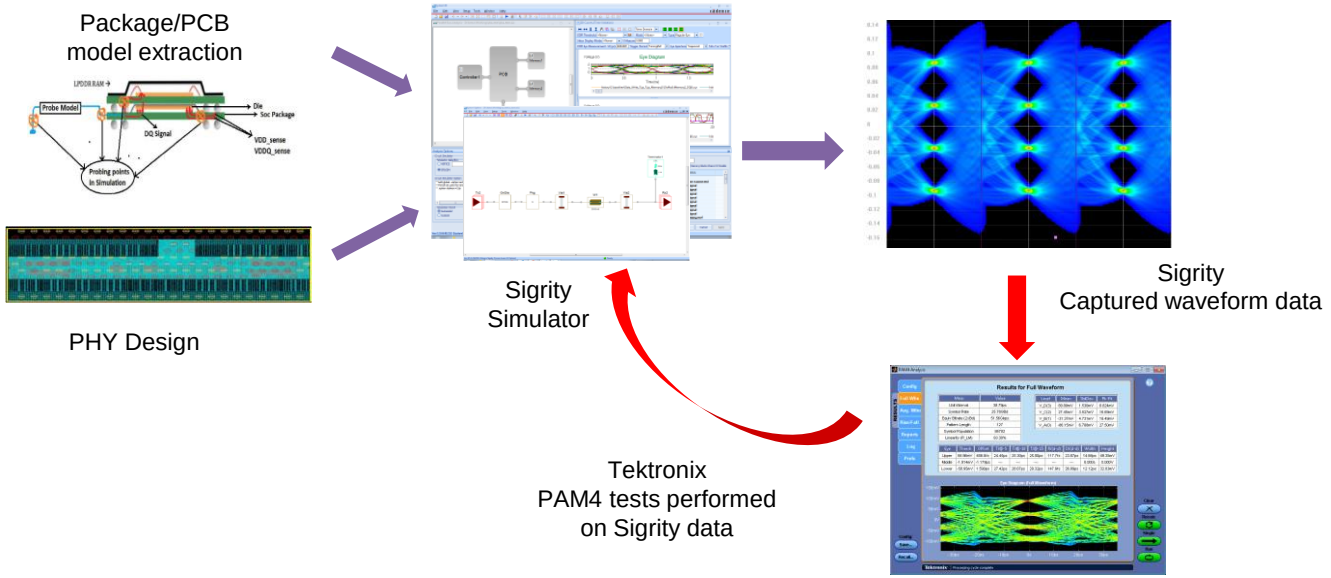
APIs IN IBIS-AMI MODELING



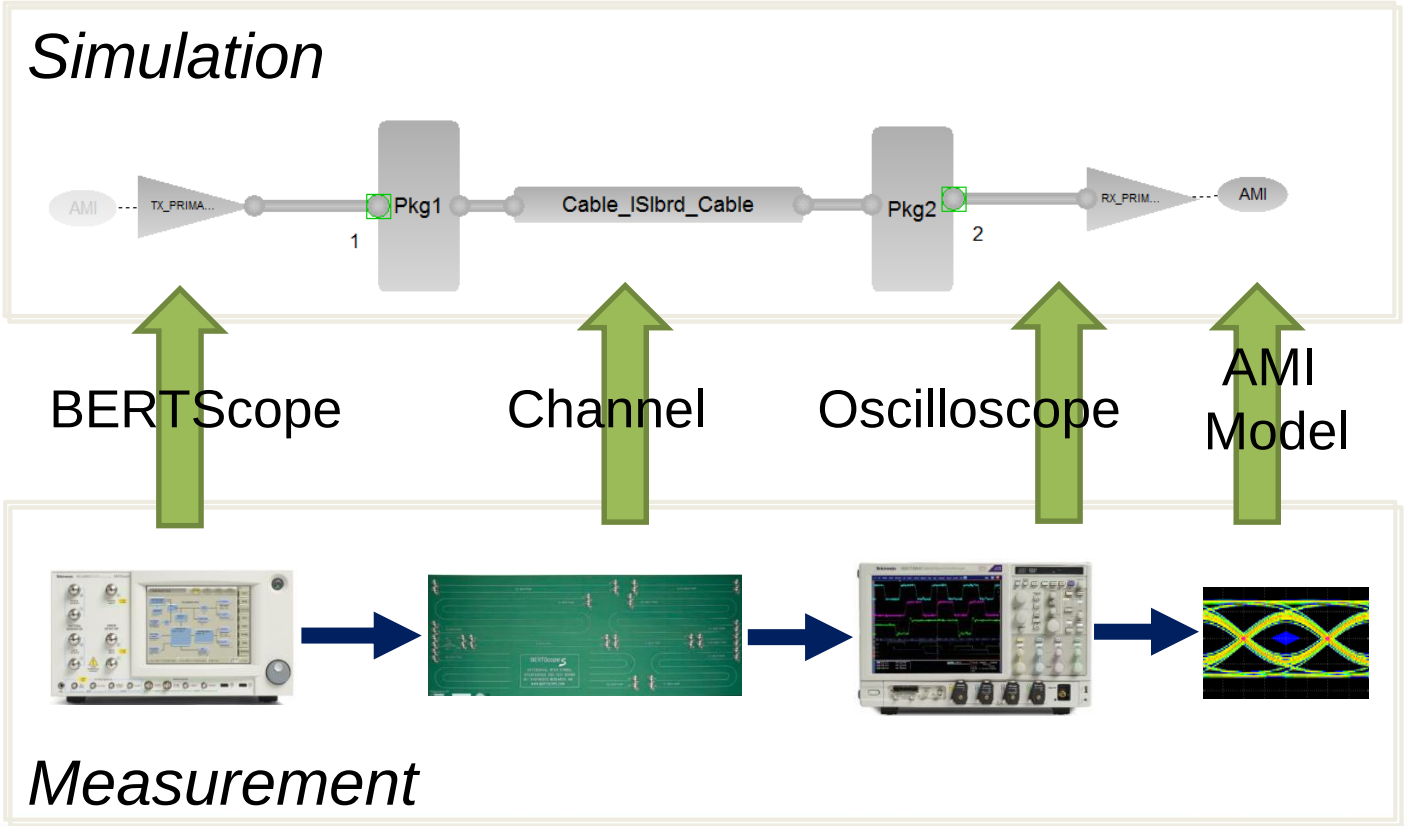
- AMI_Init for “one-time” adaptive EQs
- AMI_GetWave for “real-time” adaptive EQs

LEVERAGE LAB MEASUREMENTS IN SIMULATION

- Perform the same tests during the design and analysis stage that are used to sign-off in the lab



SYSTEM TOPOLOGY



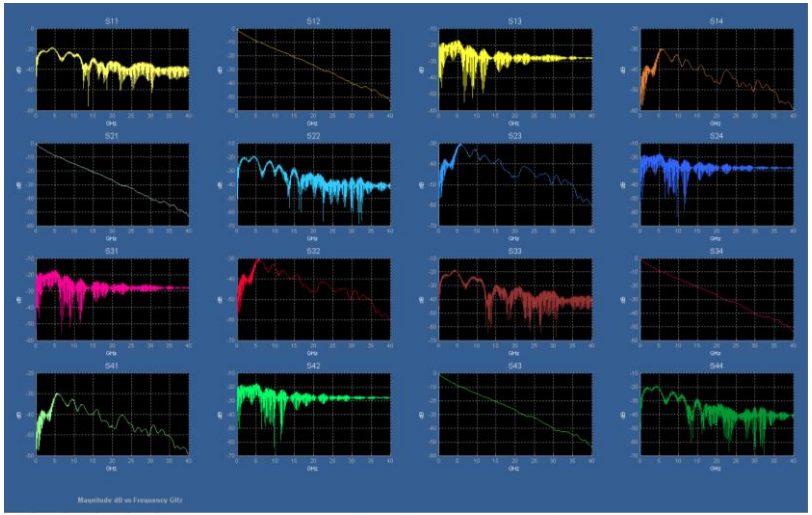
TRANSMITTER PROPERTIES

- Signaling rate: 25.78125 GBd
- Signaling: PAM4
- TX equalization: 5-tap FIR (1 precursor, 3 postcursor)
- Data pattern: PRBS7 for measurement and simulation

CHANNEL PROPERTIES

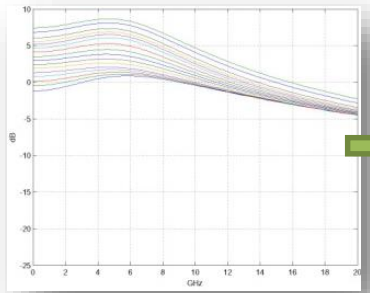
- http://www.ieee802.org/3/bs/public/channel/TEC/shanbhag_02_0914.pdf

– IEEE 802.3bs 400 Gb task force library
– Medium reach / Chip-to-chip channel using a single connector
– Insertion loss: 18.2 dB @ 12.9 GHz

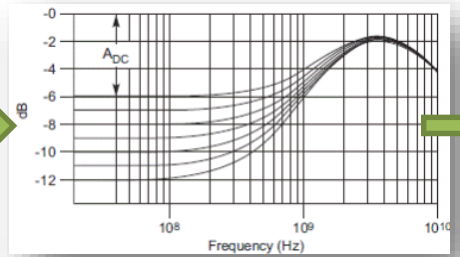


RECEIVER PROPERTIES

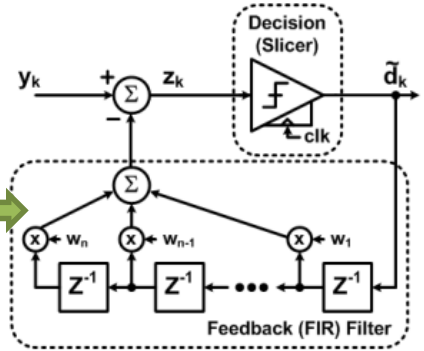
- Automatic Gain Control (AGC)
- Adaptive 2-pole Continuous Time Linear Equalizer (CTLE)
- 15-tap Decision Feedback Equalizer (DFE)



Auto Gain Control (AGC)

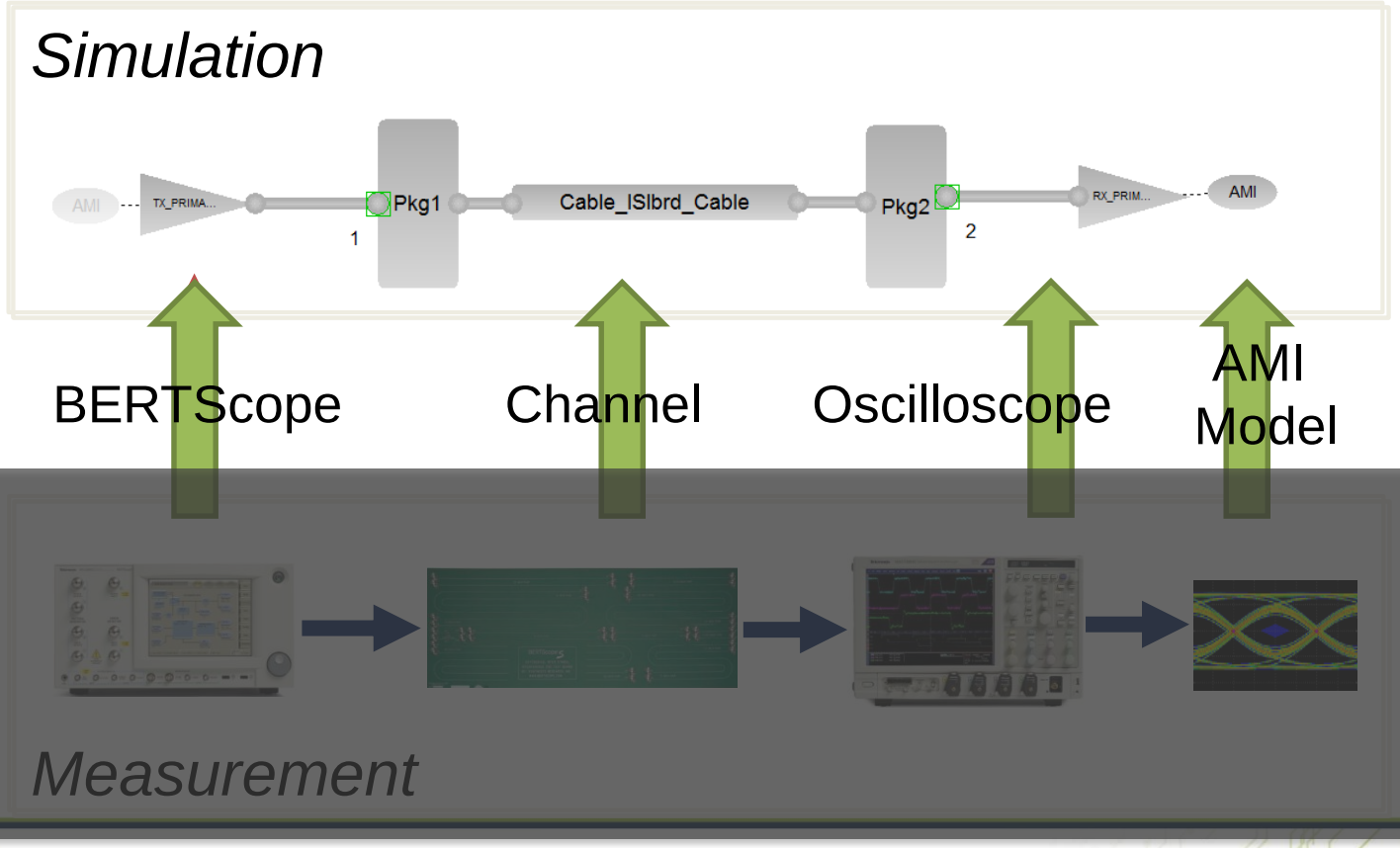


Continuous Time Linear Eq (CTLE)



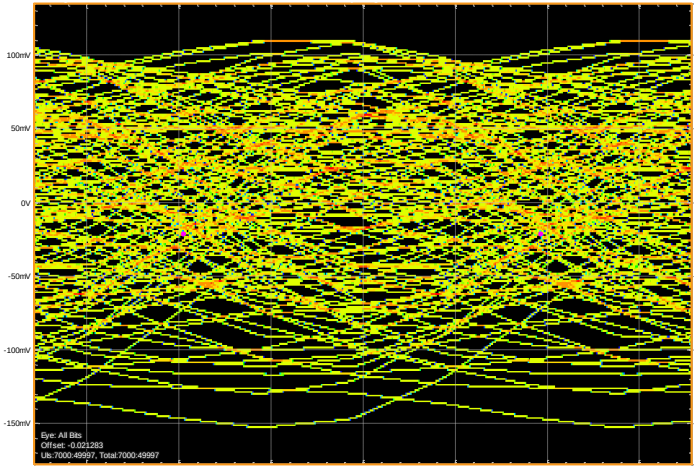
DFE + CDR

SIMULATION RESULTS

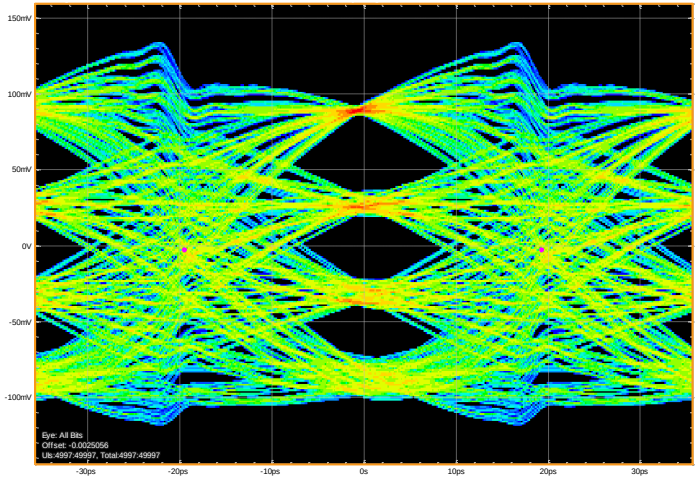


SIMULATION RESULTS

- 100,000 UIs at 64 samples/UI

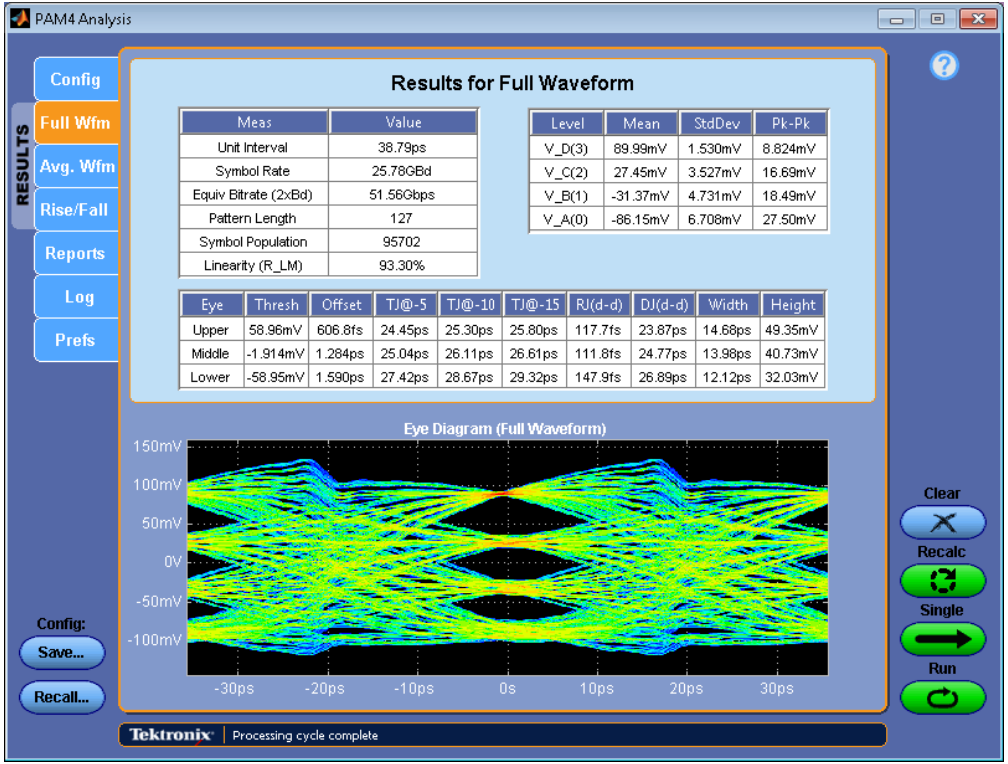


Before RX

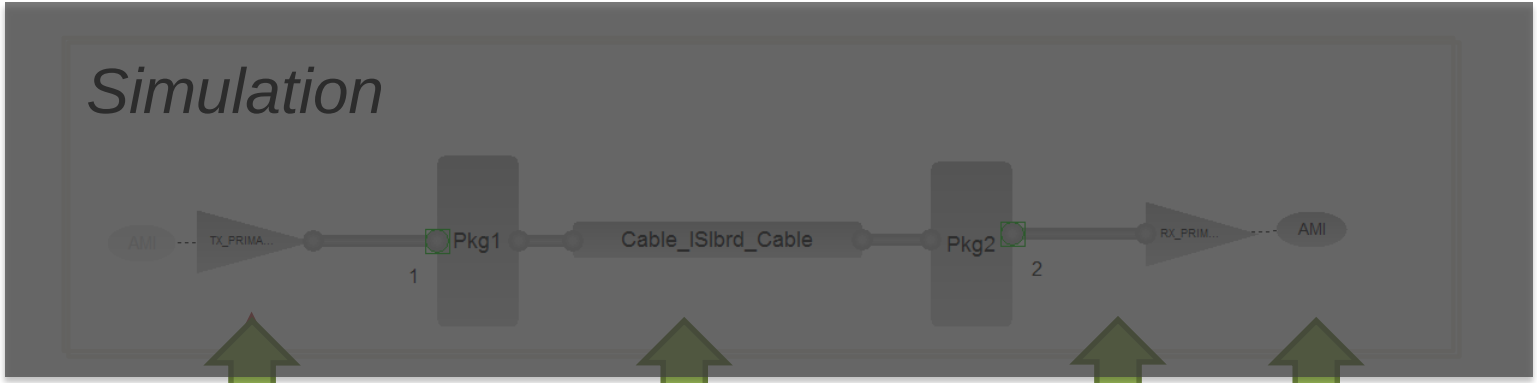


RX equalized

SIMULATION RESULTS



MEASUREMENT RESULTS

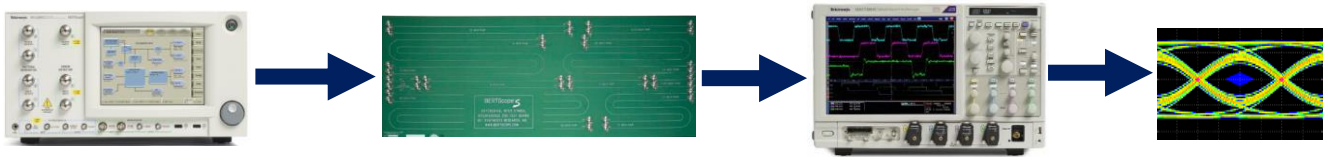


BERTScope

Channel

Oscilloscope

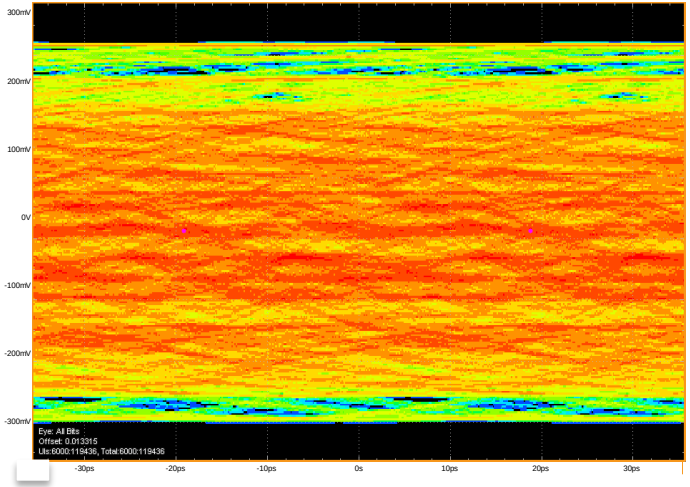
AMI Model



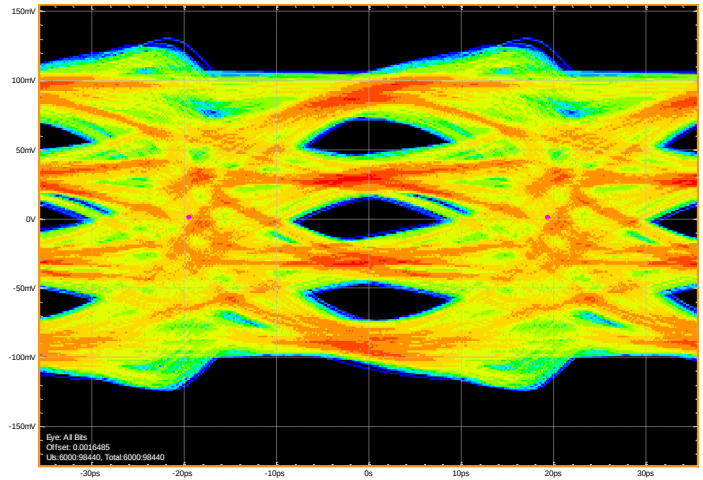
Measurement

MEASUREMENT RESULTS

- 10^6 samples at 200G samples/sec

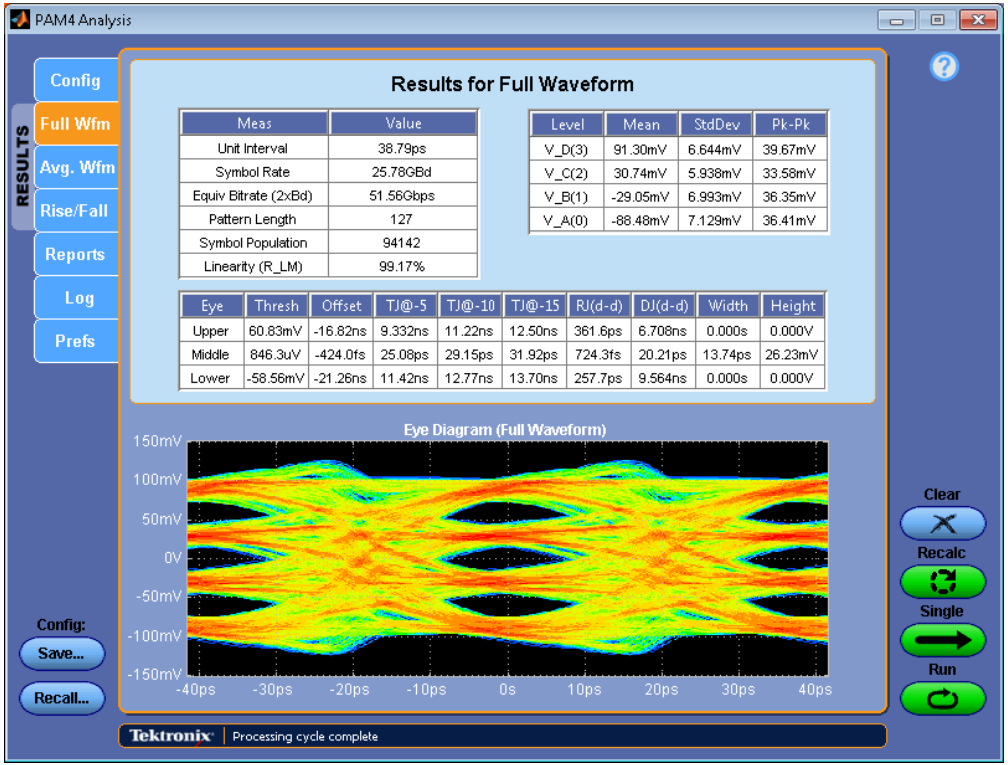


Before RX



RX equalized

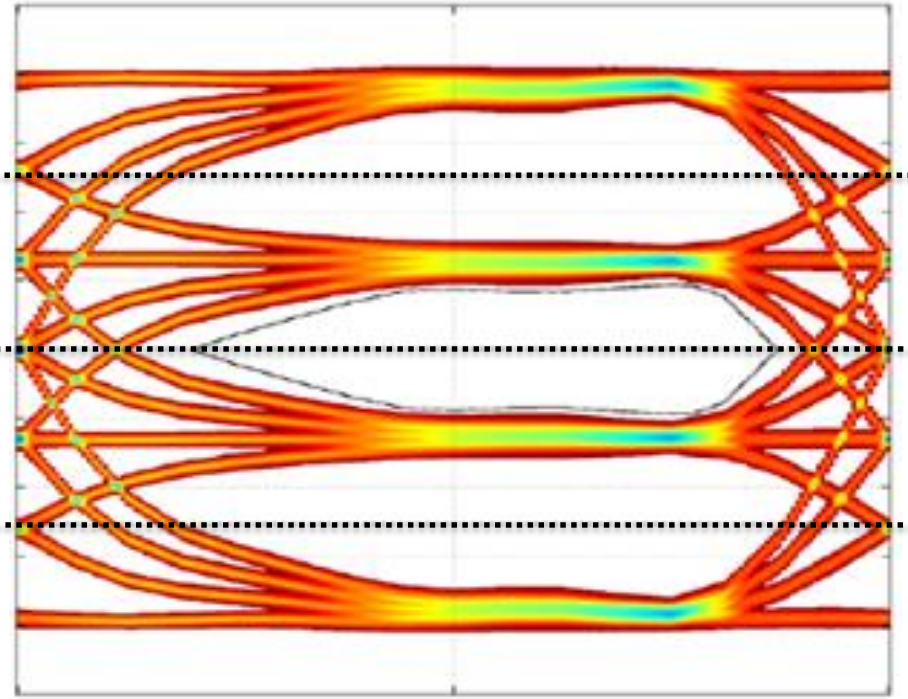
MEASUREMENT RESULTS



PRELIMINARY CORRELATION

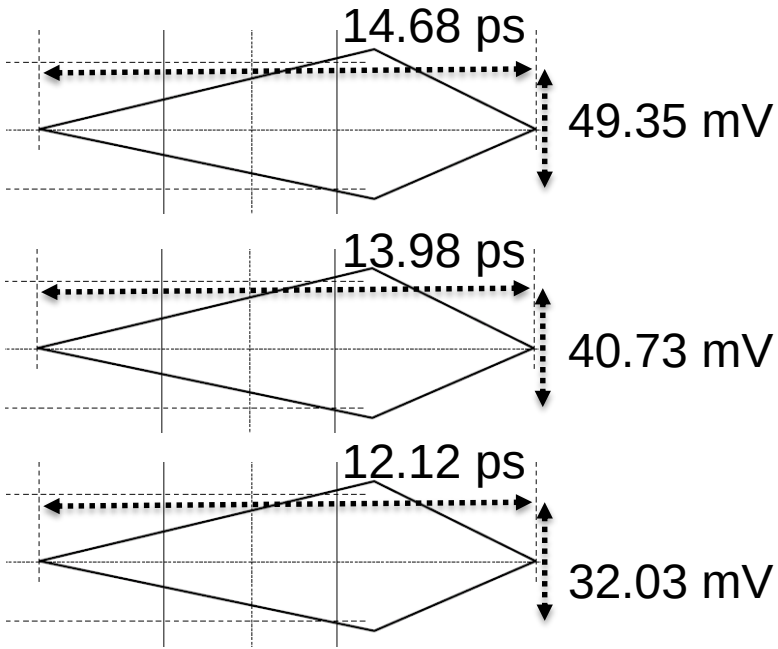
Simulation

Measurement

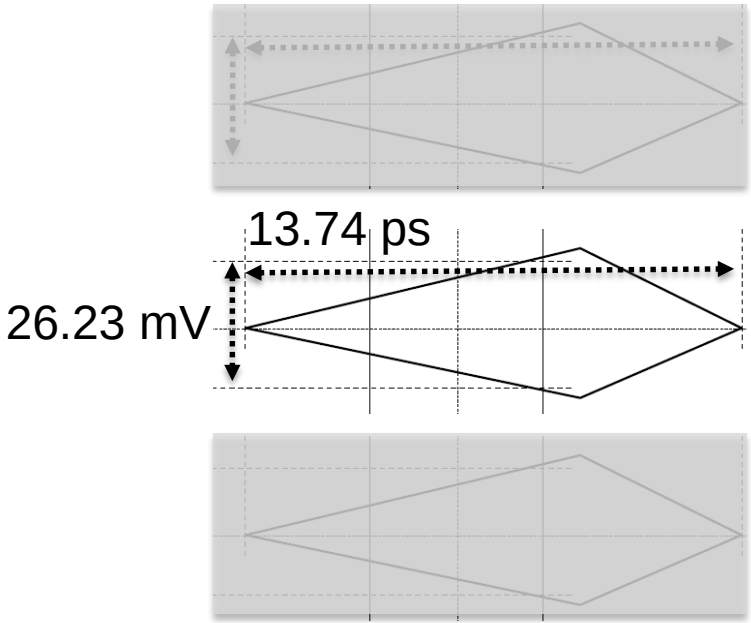


PRELIMINARY CORRELATION

Simulation



Measurement



SUMMARY

- Simulation/Measurement correlation requires accurate modeling of TX/RX/Channel
  - Quantify TX/RX/Channel/T&M instrument characteristics
  - Impulse response, jitter and noise profiles need to be accurately extracted and considered
- IBIS-AMI models enable accurate prediction of signaling inside the device after adaptive EQ
  - Design space exploration in early design phase (Design Level)
  - Final design signoff before going to manufacturing (System Level)
  - Final verification in the lab using measurement equipment
- Cadence and Tektronix are bridging the gap between simulation and lab measurement

Thank you!

QUESTIONS?