CHAPTER 14   SIGNAL INTEGRITY[*]

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14.1.   Introduction

In the realm of high-speed digital design, signal integrity has become a critical issue, and is posing increasing challenges to the design engineers. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the EMI/EMC discussions in the previous sections of this book. In this chapter, we will discuss what the typical signal integrity problems are, where they come from, why it is important to understand them and how we can analyze and solve these issues. Several software tools available at present for signal integrity analysis and current trends in this area will also be introduced.

The term Signal Integrity (SI) addresses two concerns in the electrical design aspects – the timing and the quality of the signal. Does the signal reach its destination when it is supposed to? And also, when it gets there, is it in good condition? The goal of signal integrity analysis is to ensure reliable high-speed data transmission. In a digital system, a signal is transmitted from one component to another in the form of logic 1 or 0, which is actually at certain reference voltage levels. At the input gate of a receiver, voltage above the reference value Vih is considered as logic high, while voltage below the reference value Vil is considered as logic low. Figure 14-1 shows the ideal voltage waveform in the perfect logic world, whereas Figure 14-2 shows how signal will look like in a real system. More complex data, composed of a string of bit 1 and 0s, are actually continuous voltage waveforms. The receiving component needs to sample the waveform in order to obtain the binary encoded information. The data sampling process is usually triggered by the rising edge or the falling edge of a clock signal as shown in the Figure 14-3. It is clear from the diagram that the data must arrive at the receiving gate on time and settle down to a non-ambiguous logic state when the receiving component starts to latch in. Any delay of the data or distortion of the data waveform will result in a failure of the data transmission. Imagine if the signal waveform in Figure 14-2 exhibits excessive ringing into the logic gray zone while the sampling occurs, then the logic level cannot be reliably detected.
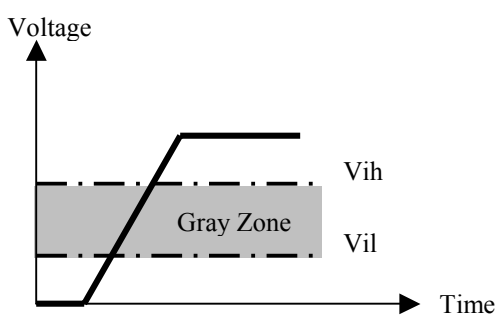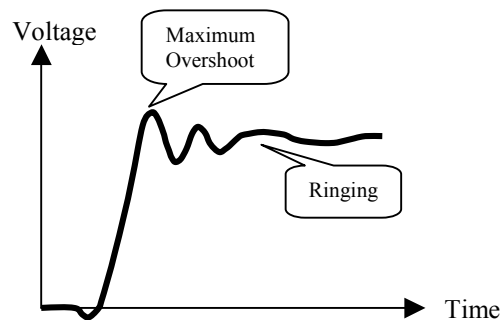

Figure 14-1. Ideal waveform at the receiving gate.

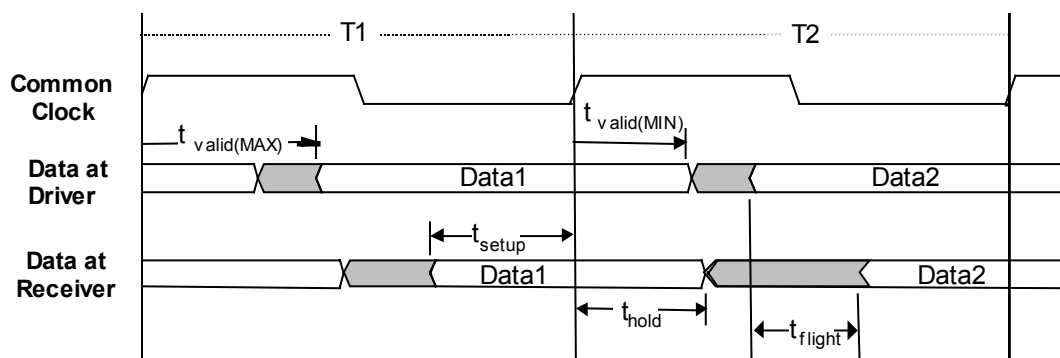**Figure 14-2. Real waveform at the receiving gate.**

Figure 14-3. Data sampling process and timing conventions.

## 14.2.   SI Problems

14.2.1.   Typical SI Problems

"Timing" is everything in a high-speed system. Signal timing depends on the delay caused by the physical length that the signal must propagate. It also depends on the shape of the waveform when the threshold is reached. Signal waveform distortions can be caused by different mechanisms. But there are three mostly concerned noise problems:

- **Reflection Noise**
  Due to impedance mismatch, stubs, vias and other interconnect discontinuities.

- **Crosstalk Noise**
  Due to electromagnetic coupling between signal traces and vias.

- **Power/Ground Noise**
  Due to parasitics of the power/ground delivery system during drivers' simultaneous switching output (SSO). It is sometimes also called Ground Bounce, Delta-I Noise or Simultaneous Switching Noise (SSN).

Besides these three kinds of SI problems, there are other Electromagnetic Compatibility or Electromagnetic Interference (EMC/EMI) problems that may contribute to the signal waveform distortions. When SI problems happen and the system noise margin requirements are not satisfied – the input to a switching receiver makes an inflection below Vih minimum or above Vil maximum; the input to a quiet receiver rises above Vil maximum or falls below Vih minimum; power/ground voltage fluctuations disturb the data in the latch, then logic error, data drop, false switching, or even system failure may occur. These types of noise faults are extremely difficult to diagnose and solve after the system is built or prototyped. Understanding and solving these problems before they occur will eliminate having to deal with them further into the project cycle, and will in turn cut down the development cycle and reduce the cost[1]. In the later part of this chapter, we will have further investigations on the physical behavior of these noise phenomena, their causes, their electrical models for analysis and simulation, and the ways to avoid them.

14.2.2.   Where SI Problems Happen

Since the signals travel through all kinds of interconnections inside a system, any electrical impact happening at the source end, along the path, or at the receiving end, will have great effects on the signal timing and quality. In a typical digital system environment, signals originating from the off-chip drivers on the die (the chip) go through c4 or wire-bond connections to the chip package. The chip package could be single chip carrier or multi-chip module (MCM). Through the solder bumps of the chip package, signals go to the Printed Circuit Board (PCB) level. At this level, typical packaging structures include daughter card, motherboard or backplane. Then signals continue to go to another system component, such as an ASIC (Application Specific Integrated Circuit) chip, a memory module or a termination block. The chip packages, printed circuit boards, as well as the cables and connecters, form the so-called different levels of electronic packaging systems, as illustrated in Figure 14-4. In each level of the packaging structure, there are typical interconnects, such as metal traces, vias, and power/ground planes, which form electrical paths to conduct the signals. It is the packaging interconnection that ultimately influences the signal integrity of a system.
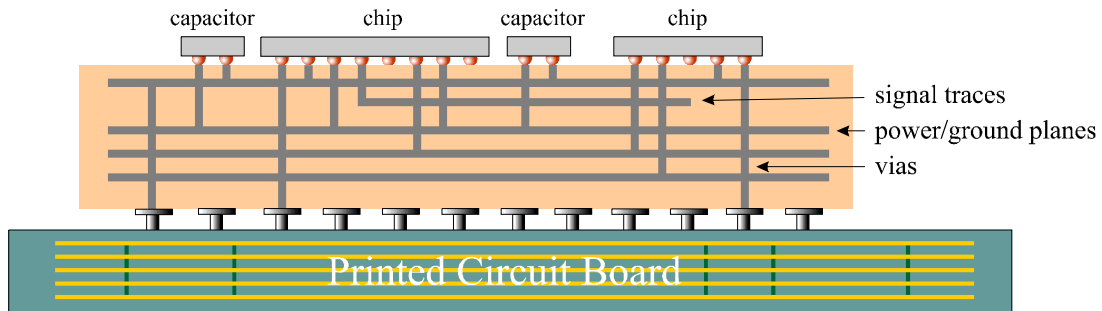
Figure 14-4. Signal Integrity Challenges Appear in IC Packages and PCBs.

14.2.3.   SI In Electronic Packaging

Technology trends toward higher speed and higher density devices have pushed the package performance to its limits. The clock rate of present personal computers is approaching gigahertz range. As signal rise-time becomes less than 200ps, the significant frequency content of digital signals extends up to at least 10 GHz. This necessitates the fabrication of interconnects and packages to be capable of supporting very fast varying and broadband signals without degrading signal integrity to unacceptable levels. While the chip design and fabrication technology have undergone a tremendous evolution: gate lengths, having scaled from 50 µm in the 1960s to 0.18 µm today, are projected to reach 0.1 µm in the next few years; on-chip clock frequency is doubling every 18 months; and the intrinsic delay of the gate is decreasing exponentially with time to a few tens of pico-seconds. However, the package design has lagged considerably. With current technology, the package interconnection delay dominates the system timing budget and becomes the bottleneck of the high-speed system design. It is generally accepted today that package performance is one of the major limiting factors of the overall system performance.

Advances in high performance sub-micron microprocessors, the arrival of gigabit networks, and the need for broadband Internet access, necessitate the development of high performance packaging structures for reliable high-speed data transmission inside every electronics system. Signal integrity is one of the most important factors to be considered when designing these packages (chip carriers and PCBs) and integrating these packages together.

14.3.   SI Analysis

14.3.1.   SI Analysis in the Design Flow

Signal integrity is not a new phenomenon and it did not always matter in the early days of the digital era. But with the explosion of the information technology and the arrival of Internet age, people need to be connected all the time through various high-speed digital communication/computing systems. In this enormous market, signal integrity analysis will play a more and more critical role to guarantee the reliable system operation of these electronics products. Without pre-layout SI guidelines, prototypes may never leave the bench; without post-layout SI verifications, products may fail in the field. Figure 14-5 shows the role of SI analysis in the high-speed design process. From this chart, we will notice that SI analysis is being applied throughout the design flow and tightly integrated into each design stage. It is also very common to categorize SI analysis into two main stages: preroute analysis and postroute analysis.
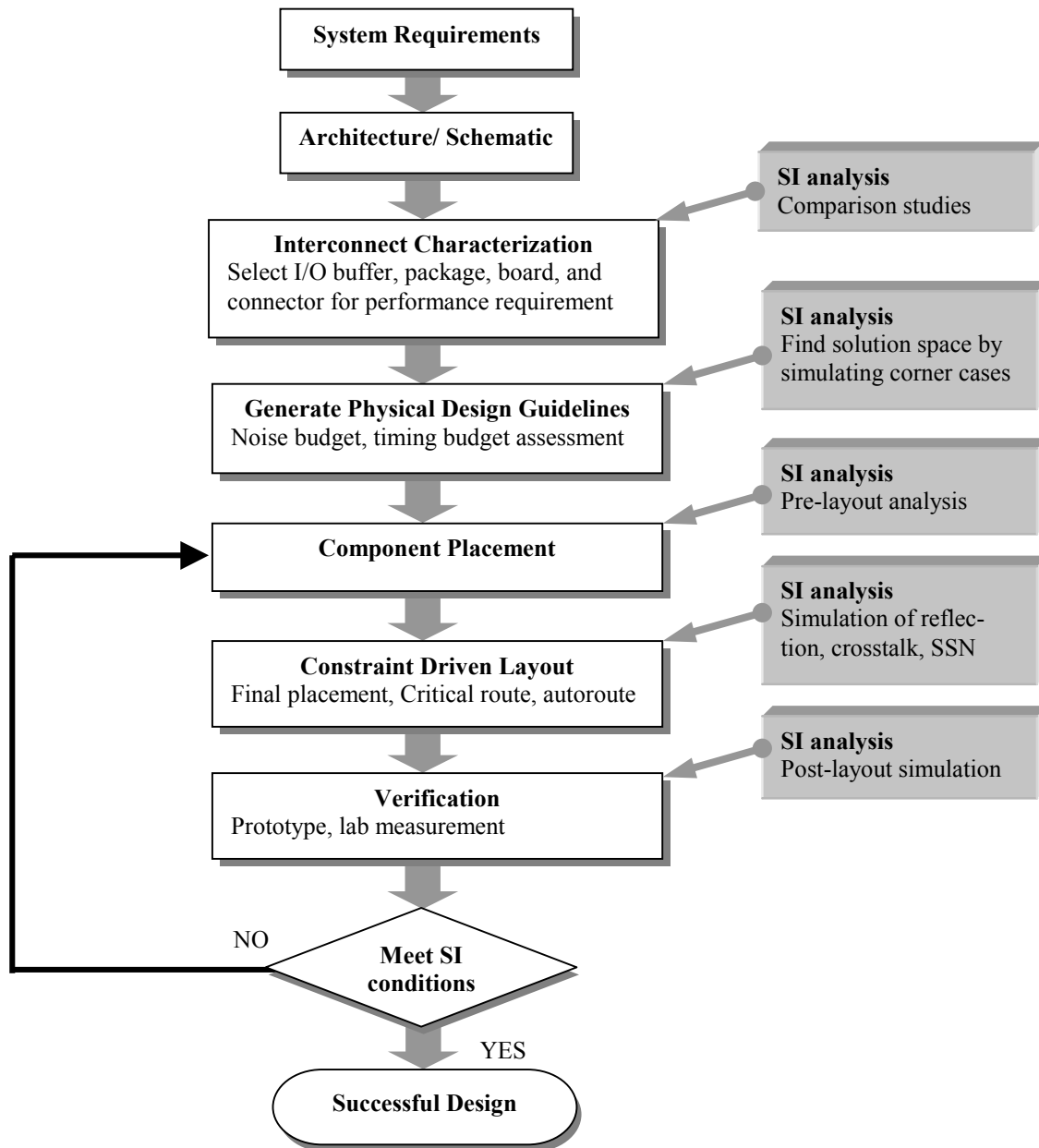
Figure 14-5. SI analysis in the design flow.

In the preroute stage, SI analysis can be used to select technology for I/Os, clock distributions, chip package types, component types, board stackups, pin assignments, net topologies, and termination strategies. With various design parameters considered, batch SI simulations on different corner cases will progressively formulate a set of optimized guidelines for physical designs of later stage. SI analysis at this stage is also called constraint driven SI design because the guidelines developed will be used as constraints for component placement and routing. The objective of constraint driven SI design at the preroute stage is to ensure that the signal integrity of the physical layout, which follows the placement/routing constraints for noise and timing budget, will not exceed the maximum allowable noise levels. Comprehensive and in-depth preroute SI analysis will cut down the redesign efforts and place/route iterations, and eventually reduce design cycle.

With an initial physical layout, postroute SI analysis verifies the correctness of the SI design guidelines and constraints. It checks SI violations in the current design, such as reflection noise, ringing, crosstalk and ground bounce. It may also uncover SI problems that are overlooked in the preroute stage, because postroute analysis works with physical layout data rather than estimated data or models, therefore it should produce more accurate simulation results.

When SI analysis is thoroughly implemented throughout the whole design process, a reliable high performance system can be achieved with fast turn-around.

In the past, physical designs generated by layout engineers were merely mechanical drawings when very little or no signal integrity issues were concerned. While the trend of higher-speed electronics system design continues, system engineers, responsible for developing a hardware system, are getting involved in SI and most likely employ design guidelines and routing constraints from signal integrity perspectives. Often, they simply do not know the answers to some of the SI problems because most of their knowledge is from the engineers doing previous generations of products. To face this challenge, nowadays, a design team (see Figure 14-6) needs to have SI engineers who are specialized in working in this emerging technology field. When a new technology is under consideration, such as a new device family or a new fabrication process for chip packages or boards, SI engineers will carry out the electrical characterization of the technology from SI perspectives, and develop layout guideline by running SI modeling and simulation software[2]. These SI tools must be accurate enough to model individual interconnections such as vias, traces, and plane stackups. And they also must be very efficient so what-if analysis with alternative driver/load models and termination schemes can be easily performed. In the end, SI engineers will determine a set of design rules and pass them to the design engineers and layout engineers. Then, the design engineers, who are responsible for the overall system design, need to ensure the design rules are successfully employed. They may run some SI simulations on a few critical nets once the board is initially placed and routed. And they may run post-layout verifications as well. The SI analysis they carry out involves many nets. Therefore, the simulation must be fast, though it may not require the kind of accuracy that SI engineers are looking for. Once the layout engineers get the placement and routing rules specified in SI terms, they need to generate an optimized physical design based on these constraints. And they will provide the report on any SI violations in a routed system using SI tools. If any violations are spotted, layout engineers will work closely with design engineers and SI engineers to solve these possible SI problems.
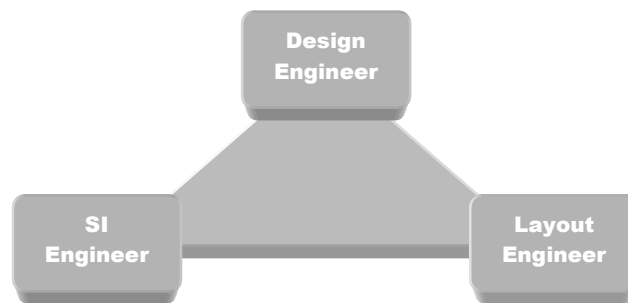
Figure 14-6. SI engineer in a design team.

14.3.2.   Principles of SI Analysis

A digital system can be examined at three levels of abstraction: logic, circuit theory, and electromagnetic (EM) fields. The logic level, which is the highest level of those three, is where SI problems can be easily identified. EM fields, located at the lowest level of abstraction, comprise the foundation that the other levels are built upon[3]. Most of the SI problems are EM problems in nature, such as the cases of reflection, crosstalk and ground bounce. Therefore, understanding the physical behavior of SI problems from EM perspective will be very helpful. For instance, in the following multi-layer packaging structure shown in Figure 14-7, a switching current in via *a* will generate EM waves propagating away from that via in the radial direction between metal planes. The fields developed between metal planes will cause voltage variations between planes (voltage is the integration of the E-field). When the waves reach other vias, they will induce currents in those vias. And the induced currents in those vias will in turn generate EM waves propagating between the planes. When the waves reach the edges of the package, part of them will radiate into the air and part of them will get reflected back. When the waves bounce back and forth inside the packaging structure and superimpose to each other, resonance will occur. Wave propagation, reflection, coupling and resonance are the typical EM phenomena happening inside a packaging structure during signal transients. Even though EM full wave analysis is much more accurate than the circuit analysis in the modeling of packaging structures, currently, common approaches of interconnect modeling are based on circuit theory, and SI analysis is carried out with circuit simulators. This is because field analysis usually requires much more complicated algorithms and much larger computing resources than circuit analysis, and circuit analysis provides good SI solutions at low frequency as an electrostatic approximation.
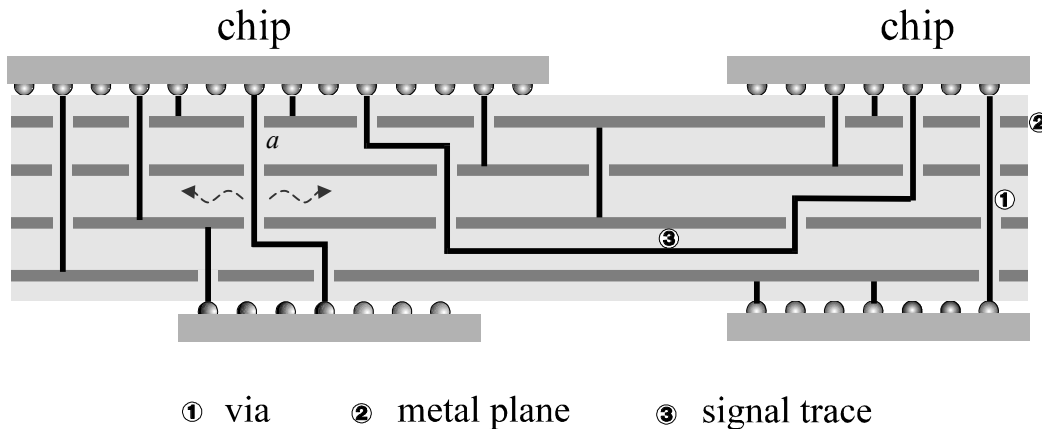

① via   ② metal plane   ③ signal trace

Figure 14-7. Multi-layer packaging structure.

Typical circuit simulators, such as different flavors of SPICE, employ nodal analysis and solve voltages and currents in lumped circuit elements like resistors, capacitors and inductors. In SI analysis, an interconnect sometimes will be modeled as a lumped circuit element. For instance, a piece of trace on the printed circuit board can be simply modeled as a resistor for its finite conductivity. With this **lumped circuit model**, the voltages along both ends of the trace are assumed to change instantaneously and the travel time for the signal to propagate between the two ends is neglected. However, if the signal propagation time along the trace has to be considered, a **distributed circuit model**, such as a cascaded R-L-C network, will be adopted to model the trace. To determine whether the distributed circuit model is necessary, the rule of thumb is – if the signal rise time is comparable to the round-trip propagation time, you need to consider using the distributed circuit model.

For example, a 3cm long stripline trace in a FR-4 material based printed circuit board will exhibits 200ps propagation delay. For a 33 MHz system, assuming the signal rise time to be 5ns, the trace delay may be safely ignored; however, with a system of 500 MHz and 300ps rise time, the 200ps propagation delay on the trace becomes important and a distributed circuit model has to be used to model the trace. Through this

example, it is easy to see that in the high-speed design, with ever-decreasing signal rise time, distributed circuit model must be used in SI analysis.

Here is another example. Considering a pair of solid power and ground planes in a printed circuit board with the dimension of 15cm by 15cm, it is very natural to think the planes acting as a large, perfect, lumped capacitor, from the circuit theory point of view. The capacitor model C= erA/d, an electro-static solution, assumes anywhere on the plane the voltages are the same and all the charges stored are available instantaneously anywhere along the plane. This is true at DC and low frequency. However, when the logics switch with a rise time of 300ps, drawing a large amount of transient currents from the power/ground planes, they perceive the power/ground structure as a two-dimensional distributed network with significant delays. Only some portion of the plane charges located within a small radius of the switching logics will be able to supply the demand. And voltages between the power/ground planes will have variations at different locations. In this case, an ideal lumped capacitor model is obviously not going to account for the propagation effects. Two-dimensional distributed R-L-C circuit networks must be used to model the power/ground pair.

In summary, as the current high-speed design trend continues, fast rise time reveals the distributed nature of package interconnects. Distributed circuit models need to be adopted to simulate the propagation delay in SI analysis. However, at higher frequencies, even the distributed circuit modeling techniques are not good enough, full wave electromagnetic field analysis based on solving Maxwell's equations must come to play. As presented in later discussions, a trace will not be modeled as a lumped resistor, or a R-L-C ladder; it will be analyzed based upon transmission line theory; and a power/ground plane pair will be treated as a parallel-plate wave guide using radial transmission line theory.

Transmission line theory is one of the most useful concepts in today's SI analysis. And it is a basic topic in many introductory EM textbooks. For more information on the selective reading materials, please refer to the Resource Center in Chapter 16.

In the above discussion, it can be noticed that signal rise time is a very important quantity in SI issues. So a little more expanded discussion on rise time will be given in the next section.

14.4.   SI Issues in Design

14.4.1.   Rise Time and SI

Not long ago, the typical rise and fall time of the transistor were still in the nano-second range. Today, with the vast improvement of the chip fabrication technology, the silicon size is shrinking dramatically and the transistor channel length is greatly reduced into sub-micron range. This trend leads to today's logic families operating at much higher speed. Their rise and fall time are on the order of hundreds of pico-second. As we move into deep-sub-micron regime, it will not be a surprise to see signals with even faster switching characteristics. Since many SI problems are directly related to dV/dt or dI/dt, faster rise time significantly worsens some of the noise phenomena such as ringing, crosstalk, and power/ground switching noise. Systems with faster clock frequency usually have shorter rise time, therefore they will be facing more SI challenges. But even if a product is operating at 20Mhz clock frequency, it may still get some SI problems that a 200MHz system will have when modern logic families with fast rise time are used.

14.4.2.   Transmission Lines, Reflection, Crosstalk

In chip packages or printed circuit boards, a trace with its reference plane constitutes a type of transmission line (Figure 14-8a), as well as when it is sandwiched between two metal planes (Figure 14-8b). A pair of parallel conducting wires separated by a uniform distance, such as the pins and wires in a cable or socket, are transmission lines (Figure 14-8c). A pair of metal planes with an attached via is another type of transmission line (Figure 14-8d).

Microstripline	Stripline	Wire Pair	Radial transmission line
8a	8b	8c	8d
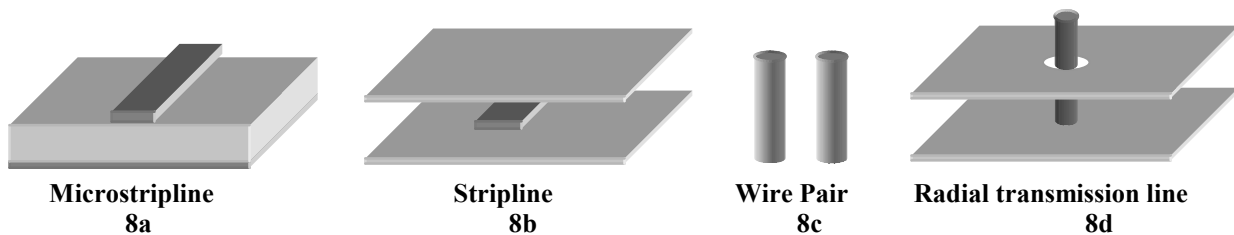
Figure 14-8. Different types of transmission line structures in packages and printed circuit boards.

These transmission lines shown in Figure 14-8 serve the purpose of sending signals from point A to point B. All the transmission lines have basic parameters such as per-unit-length R (resistance), L (inductance), G (conductance) and C (capacitance), unit-length time delay (inverse of the propagation speed), and characteristic impedance. For simple transmission line structures such as parallel-plate, these parameters can be analytically obtained. For other types of transmission line structures, usually a 2D static EM field solver (or some empirical formulas) is needed to obtain these parameters.

In SI analysis, since the electric models for many interconnects can be treated as transmission lines, it is important to understand the basics of transmission line theory and get familiar with common transmission line effects in high-speed design.

Reflection is a well-studied transmission line effect. In high-speed system, reflection noise increases time delay and produces overshoot, undershoot and ringing. The root cause of reflection noise is the impedance discontinuity along the signal transmission path. When a signal changes its routing layer and the impedance values are not consistent (manufacturing variations, design considerations, etc.), reflection will occur at the discontinuity boundary. When a trace is routed over planes with perforations at different locations (degassing holes, via holes, etc.), crossing a gap, having branches (stubs), or passing the proximity of another trace, impedance discontinuity will occur and reflection can be observed. When a signal finally reaches the receiving end of a transmission line, if the load is not matched with the transmission line characteristic impedance, reflection will also happen. To minimize reflection noise,

common practices include controlling trace characteristic impedance (through trace geometry and dielectric constant), eliminating stubs, choosing appropriate termination scheme (series, parallel, RC, Thevenin), and always using a solid metal plane as the reference plane for return current.

Crosstalk, caused by EM coupling between multiple transmission lines running parallel, is also a well-studied subject in Electromagnetics. It can cause noise pick up on the adjacent quiet signal lines that may lead to false logic switching. Crosstalk will also impact the timing on the active lines if multiple lines are switching simultaneously. Depending on the switching direction on each line (even mode switching, that is, all lines going either from low-to-high, or from high-to-low, usually yields most delay), the extra delay introduced may significantly increase/decrease the sampling window. The amount of crosstalk is related to the signal rise time, to the spacing between the lines, and to how long these multiple lines run parallel to each other. To control the crosstalk, one can make the lines space apart, add ground guarding band in between the signal lines, keep the parallelism to minimum, and keep the traces close to the reference metal planes.

Besides the crosstalk between traces, via coupling is sometimes also important[4].

14.4.3.   Power/Ground Noise

Power/ground noises occupy 30%+ noise budget in today's high-speed design. It is one of the most difficult EM effects to be modeled in SI analysis because of the complexity of the power/ground distribution system.

In chip package and printed circuit board, power/ground planes with vias form power distribution networks[5]. Transient currents drawn by a large number of devices (core-logic, off-chip drivers) switching simultaneously can cause voltage fluctuations between power and ground planes, namely the simultaneous switching noise (SSN), or Delta-I noise, or power/ground bounce. SSN will slow down the signals due to imperfect return path constituted by the power/ground distribution system. It will cause logic error when it couples to quiet signal nets or disturbs the data in the latch. It may introduce common mode noise in mixed analog and digital design. And it may increase radiation at resonant frequencies. With ever-increasing IC transition speed and I/O count, packages with new emerging technologies are capable of switching under 200 ps transition time and sinking up to 20 A of power supply current. The SSN increases significantly as this trend continues. Meanwhile, as package design engineers try to lower the system operating voltage to solve the heating problem, the SSN affects more easily the reliability of device performance. To deal with this challenge, electrical properties of power/ground planes in packaging structures need to be accurately characterized.

As discussed in the previous section "Principles of SI Analysis", the power/ground planes are distributed circuits. The physical behavior of SSN between power/ground planes is an EM problem in nature. To accurately simulate SSN, wave propagation, reflection, edge radiation, via coupling, and package resonance are all needed to be considered. In many literatures, effective inductors are used to model electrical properties of power and ground planes[6][7]. The effective inductor model (Figure 14-9a), which is valid only at the low frequency limit, does not take into account the wave propagation and resonance in power and ground planes. It is therefore unsuitable and inaccurate to model high-speed packaging structures. The wire-antenna model (Figure 14-9b), which computes the currents in conducting wires by the Method of Moments, is another approximation of the power and ground plane structures[8]. This approach can take care of the wave propagation and via interactions, but it requires long computation time for complex structures. It is also not convenient to directly link this frequency domain technique with time domain circuit simulators. The popular 2D capacitor/inductor mesh model has been used in circuit simulators to model power and ground planes by many companies (Figure 14-9c). With this method, conductor planes are divided into small elements, and each element is modeled by its element capacitor and inductors. The main advantage of this approach is its transient SPICE type circuit simulation, but it also features long computation time and large memory space usage.
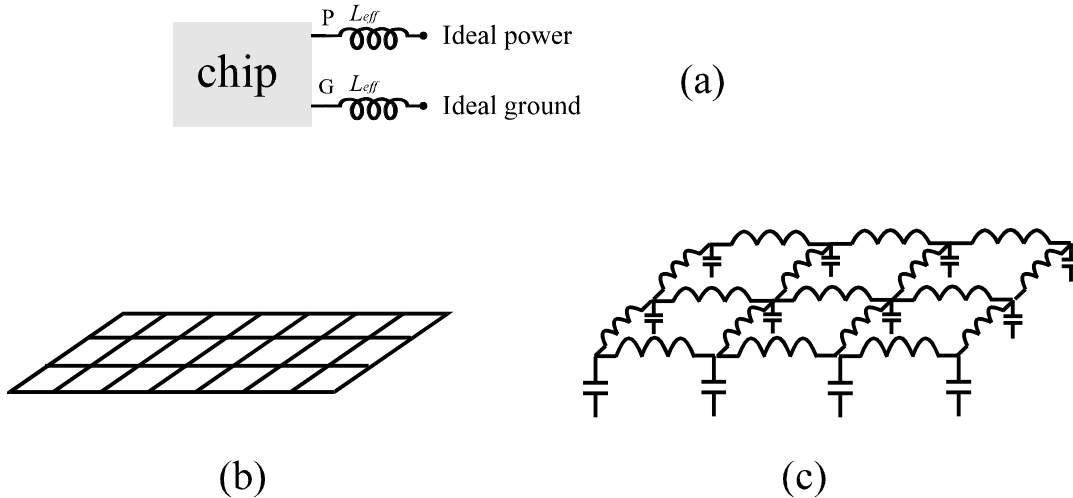
Figure 14-9. **(a)** Effective inductor model
(b) Wire antenna model
(c) Inductance/capacitance mesh model

For high accuracy modeling, full-wave electromagnetic field solvers, such as the three-dimensional finite-difference time-domain (FDTD) method or finite element method (FEM), in principle, can always be applied. But three-dimensional electromagnetic field solvers need very large computer resources (long computation time and huge computer memory space), so they are not suitable for prompt modeling in practical design and analysis.

In summary, the conventional techniques for multi-layer power/ground modeling and SSN simulation can be described as a three-stage process:

1. Extract the paracitics (equivalent circuit models) of the power/ground distribution system using EM field analysis based on Finite Element Method, Method of Moment, or Partial Element Equivalent Circuit method (For discussions on these EM modeling approaches, please see next section);

2. Combine the driver/receiver (transistor or behavioral model) and signal traces (transmission line model) with the extracted power/ground models into a SPICE type of circuit networks;

3. Run SPICE type of circuit simulations for SSN analysis.

The drawbacks of this kind of traditional approach are:

1. Long extraction time for practical PCB power/ground plane structures;

2. Huge equivalent circuit networks for multi-layer power/ground structures with thousands of power/ground vias if accurate EM models need to be included;

3. Over simplified power/ground equivalent circuit model when some EM effects are neglected;

4. Extracted models are frequency dependent and bandwidth limited;

5. Need to re-extract the models once the physical layout is changed;

6. Since the power/ground distribution system is extracted alone without considering the effects from signal distribution system, the extracted model loses the interaction between power/ground system and signal system.

For fast and accurate power/ground noise simulation, special purpose EM field solvers and hybrid simulation approaches must be adopted. A better approach[9][10], which links field solvers and circuit solvers together and solves them simultaneously in a single computation stage, yields much more simulation efficiency for power/ground noise analysis. This approach eliminates the extraction of

11

equivalent circuit model for power and grounds. It directly solves the Maxwell's equations for the fields inside the multi-layer structure, while in the meantime (at the same time step), it finds the circuit simulation solutions. The linking mechanism of this approach for the structure in Figure 14-7 is illustrated in Figure 14-10.
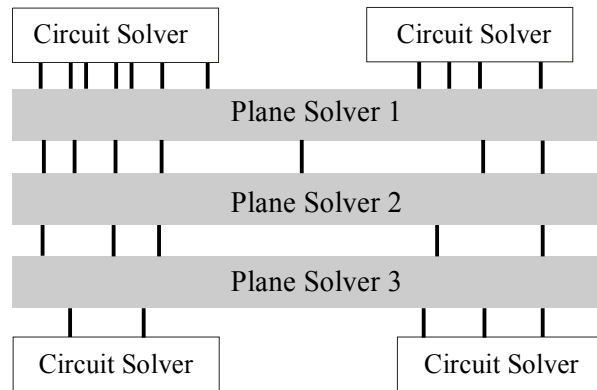
Figure 14-10. Power/ground noise analysis using combined field analysis and circuit analysis.

Decoupling strategy is another important aspect in power/ground model and SSN simulation, because, in the end, suppressing the power/ground noise with better stackup, optimized decoupling capacitor (Decap) placement, and the right combination of Decap values, is the objective of the SI analysis. Many papers have contributed detailed discussions in this area [11][12].

14.5. Modeling and Simulation

14.5.1. EM Modeling Techniques

Common EM modeling methodologies used in SI analysis are listed below [13][14]. SI tools with field solvers will most likely incorporate one or more of the following methods. Knowing the basics of these methods will help SI engineers determine the pros and cons of the tools and the application ranges of the tools.

1. Boundary Element Method (BEM) and Method of Moment (MoM), the same methods with different names.
   - Integral equation formulation;
   - Unknowns confined to conductors;
   - Require construction of Green's Function that can be complicated to generate for complex structures. Not well suited for inhomogeneous dielectric material;
   - Require solving dense matrix.

2. Finite Difference Time Domain (FDTD) method, a general purpose and versatile approach for arbitrary inhomogeneous geometries.
   - Differential equation formulation;
   - Direct time domain solution of Maxwell's equations;
   - Unknown throughout entire region. Computer intensive;
   - No matrix inversion.

3. Finite Element Method (FEM), a general purpose and versatile approach for arbitrary inhomogeneous geometries.
   - Laplace/Helmholtz equation formulation;
   - Computer intensive;
   - Sparse matrix.

4. Partial Element Equivalent Circuit (PEEC) approach, a simplified and approximate version of MoM.
   - Integral equation formulation from magneto-quasistatic analysis;
   - Unknowns confined to conductors.

14.5.2.   SI Tools

A good SI tool should contain the following key components: 2D field solvers for extracting RLGC matrices of single/couple transmission lines; single/couple lossy transmission line simulator; 3D field solvers for wirebonds, vias, metal planes; behavior modeling of drivers and receivers. They should also take physical layout files as input data and post process simulation results in time domain (timing and waveform measurement) and frequency domain (impedance parameter and S-parameter). Table 14-1 shows the major SI tools currently available on the market.

Company	Tool	Function
Ansoft	SI 2D	2D static DC EM simulation extracts inductance and capacitor
	SI 3D	3D static DC EM simulation extracts resistance, inductance and capacitance
	PCB/MCM Signal Integrity	PCB/MCM pre and post route SI analysis
	Turbo Package Analyzer	Package RLGC extraction
Applied Simulation Technology	ApsimSI	Reflection and Crosstalk simulation for lossy coupled transmission lines
	ApsimDELTA-I	Delta-I noise simulation
Cadence	SPECCTRAQuest	SI simulation: transmission line simulation, power plane builder
HP Eesof	Picosecond Interconnect Modelling Suite	Frequency-domain and time-domain simulation for coupled lines and I/O buffers
Hyperlynx (PADS)	HyperSuite	Single/couple transmission line simulation.
INCASES (Zuken)	SI-WORKBENCH	Lossy coupled transmission line simulation
Mentor Graphics	IS_Analyzer	Delay, Crosstalk simulation
Quantic EMC	BoardSpecialist Plus	Delay, Crosstalk simulation
Sigrity	SPEED97/SPEED2000	Power/ground noise simulation with couple lossy transmission line analysis
Viewlogic Systems (Innoveda)	XTK	Couple lossy transmission line analysis
	AC/Grade	Power/ground modeling

Table 14-1. Major Sigrity Integrity tools.

14.5.3. IBIS

The Input/Output Buffer Information Specification (IBIS) is an emerging standard used to describe the analog behavior of the Input/Output (I/O) of a digital Integrated Circuit (IC). IBIS specifies a consistent software-parsable format for essential behavioral information. With IBIS, simulation tool vendors can accurately model compatible buffers in SI simulations.

Improvement of chip and package design technology accompanying industrial competition has resulted in the need for new descriptive models of integrated circuit drivers and receivers. These models should be nonproprietary and capable of maintaining suitable accuracy and speed in the simulation of transmission lines and signal integrity related effects such as crosstalk and power/ground bounce (noise).

Simulation of digital I/O buffers, together with their chip packages and printed circuit boards, can mainly be done in two ways. The traditional approach is to use transistor level models, which is useful when small-scale simulations or analysis of some particular network is the objective of the simulation. This approach would be very time consuming for simulations of large number of buffers and their interconnections. Transistor level models may also reveal vendor's proprietary device information. As a solution to this problem, behavioral models of devices such as I/O Buffer Information Specification (IBIS) are introduced[15]. The behavioral IBIS modeling data can be derived from measurements as well as circuit simulations. Simulations with behavioral models can be generally executed faster than the corresponding simulations with transistor level models. A behavioral device model does not reveal any detailed and sensitive information about the design technology and the underlying fabrication processes, so the vendor's intellectual property would be protected.

The behavioral IBIS based models of a device provide the DC current vs. voltage curves along with a set of rise and fall time of the driver output voltage and packaging parasitic information of the I/O buffer. It should be noted that the IBIS modeling data itself does not provide explicit information on driver transient state transitions beyond the steady-state I-V curves. The extraction of the transient state transition of buffers is necessary for correct SI simulations. There have been few publications in the public domain on how this extraction is accomplished [16][17].

IBIS behavioral model presentation of a device as shown in Figure 14-11 provides information about the I/V characteristics of the power and ground clamp diodes of the buffer, the input or output die capacitance (C_{comp}) and the characteristics of the package (the values of the lead inductance (L_{pkg}), resistance (R_{pkg}) and capacitance(C_{pkg})). IBIS modeling data also includes DC steady state I/V characteristics of the upper and lower devices and the voltage vs. time characteristics of (high-to- low) and (low-to-high) transition for a specific set of given load Z_{meas} (normally a passive resistor).
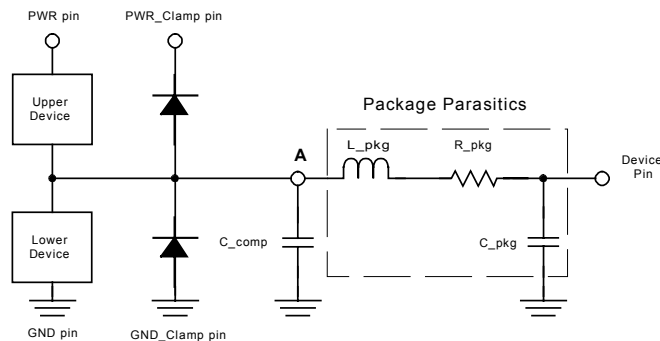

Figure 14-11. IBIS representation of an I/O buffer.

For more information on IBIS, please refer to the Resource Center in Chapter 16 for official IBIS web site and email forum.

14.6.   A SI Example

The previous sections discussed the definition of SI, typical SI problems, their causes and their importance. Some backgrounds on the SI analysis including theoretical principles, modeling methodologies and simulation tools were also introduced. In this section, an example will be shown how a SI problem was solved using simulation tools for a practical product during the design process.

This is a 4 layer PCB with a stackup of signal/power/ground/signal. A DSP chip is placed near the center of the board. The signals from the chip have 500ps edge rate. During the routing stage, attentions had been given on the crosstalk constraints so that the spacing between adjacent traces were wide enough and would not generate excessive coupling noise. After the prototype was built, measurement revealed that a clock net experienced quite large coupling noise whenever the chip had drivers switching simultaneously. Visual examination showed that the clock net was routed far away from the switching signal traces, and no constraint violation of crosstalk was found (Figure 14-12 shows the topology of the clock net, the signals, and the location of the chip). Detailed post-layout crosstalk simulation also verified that the coupling between the clock trace and the signal traces was minimal. So where was the pickup noise coming from?
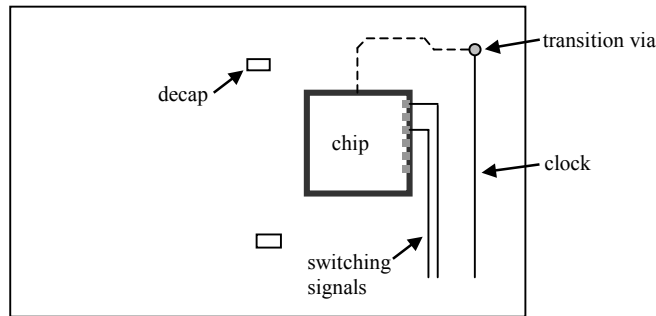
Figure 14-12. Illustration of the problematic clock net on the PCB during simultaneous switching output.

Since the noise pick-up always occurred during simultaneous switching output (SSO), a thorough analysis on power/ground noise was carried out in the next SI simulation stage. With the 3D model of the PCB structure in place and the switching circuits attached, EM fields inside the PCB were solved using a commercial SI tool, SPEED97, developed by Sigrity, Inc (Resource Center, Chapter 16, SI software vendor). Figure 14-13 displays an instantaneous snap shot of the spatial voltage fluctuations between the power and ground planes during signal transients at 1.51ns, whereas Figure 14-14 shows the spatial distribution of the historical peak values of the noise voltages between the power and ground planes within 10ns. From the graph (Figure 14-14), the location of the switching sources and the on-board decoupling capacitors can be easily identified. It can also be noticed from Figure 14-14, that another area showing large power/ground noise swing is at the upper corner, and that is where the clock via resides. It was clear then when the clock trace changed its routing layer from top to bottom, the transition via between the power and ground planes picked up the power/ground noise. The grayscale image in Figure 14-15 again illustrates that the clock via is in the hot spot of the simultaneous switching noises.
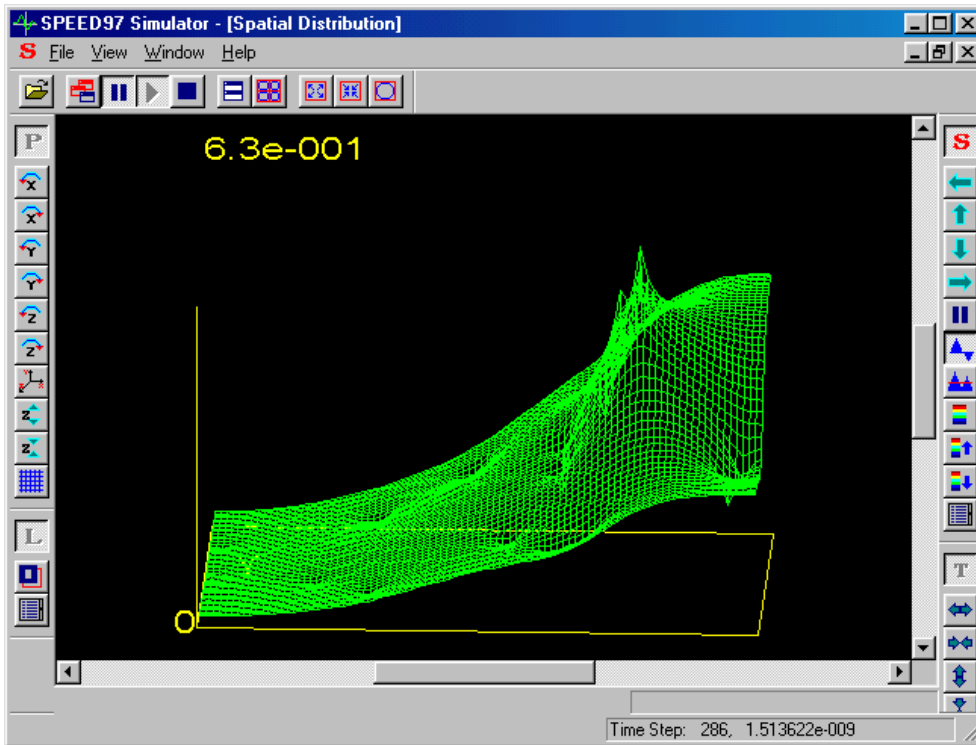
Figure 14-13. Spatial noise distribution between the power and the ground plane at 1.51 ns.
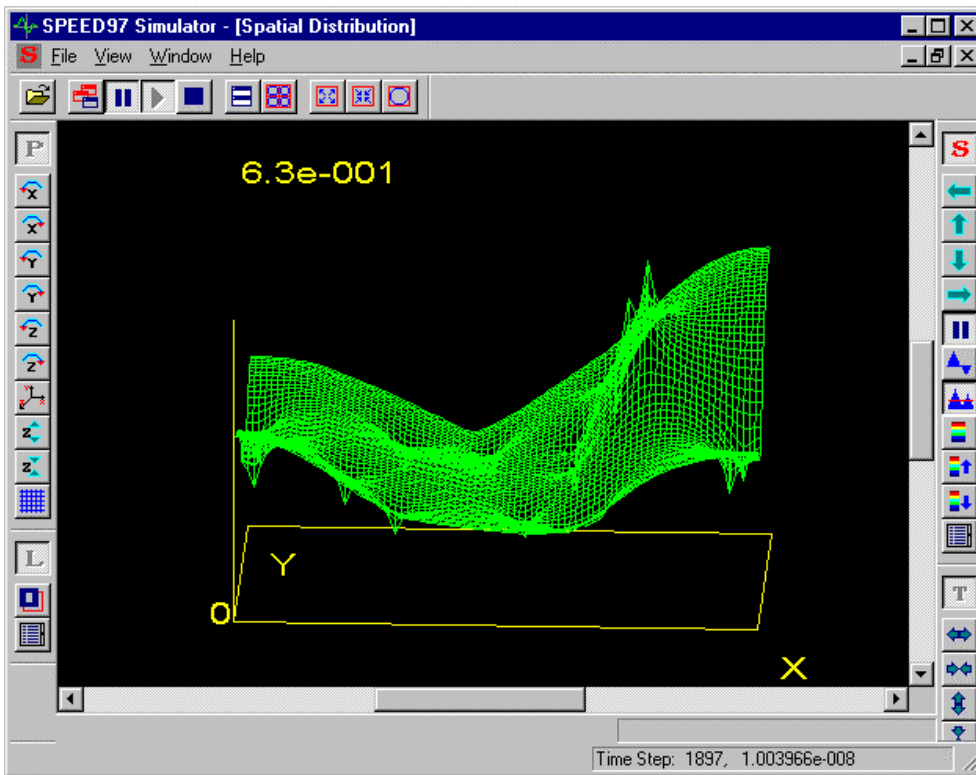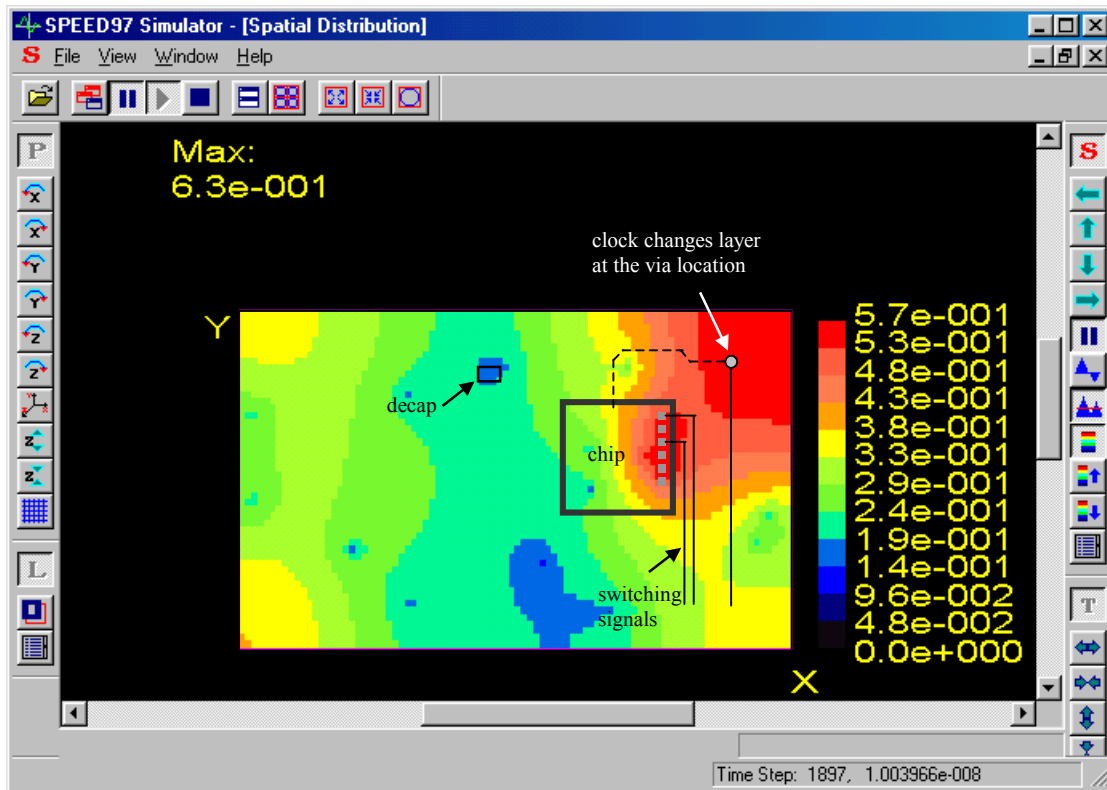

Figure 14-14. Spatial distribution of the peak noise voltage between the power and the ground plane within 10ns.

Figure 14-15. Clock net picks up simultaneous switching noise at the via location.

The solution for suppressing the coupling noise was rather simple. By adding an extra decoupling capacitor near the clock via at the upper corner of the board, power/ground noise at that location was reduced and the induced coupling noise in the clock was kept below noise margin. The proper value of the decoupling capacitor was determined through a series of what-if simulations using the above-mentioned SI tool. Later modified PCB prototype verified the prediction from the field simulations. It was a successful design, after a careful SI analysis.

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SI Jargon

Fall Time
Time for a signal to change from a logic high state to a logic low state.

Flight Time
Time difference between the signal at the driver reaching Vref with a reference/test load and the signal at the receiver reaching Vref. Flight time is also known as bus loss, since it historically was used to derate the spec Tco timing to account for the difference between the spec load and the actual system load impact on circuit timing.

ISI (Inter Symbol Interference)
ISI refers to the interactions between the logic value/symbol from the previous switching cycle and the symbol traveling on the same channel of the current cycle. ISI occurs as a result of energy stored in the channel summing with a latter unrelated signal. It is dependent upon multi-cycle reflections and affects the rising/falling edge and settling characteristics.

Jitter
Jitter refers to deviation in time between edges of individual signals that are periodic. For example, clock jitter is the time deviation from the clock period (the clock period may be compressed or expanded). Jitter can also affect source-synchronous circuits that have transactions spanning multiple cycles or edges, and it can also be applied to differences between rise and fall edges of a signal.

Overshoot/Undershoot
Overshoot/Undershoot occurs when a signal transition goes beyond the Vol/Vil for a falling edge and Voh/Vih for a rising transition.

Period
For common clock circuits and multi-clock cycle transactions, period refers to a single clock or strobe cycle duration from a rising edge transition to the next rising edge transition (or falling edge to falling edge). For example, a 1GHz cycle period is 1ns duration.

Push-out/Pull-in
Push-out and pull-in refer to the difference in signal flight time due to signal coupling effects and signal return path discontinuities. Comparing with the delay of single-bit switching, push-out means all the drivers switching at the same direction (even mode), whereas pull-in means all the other drivers switching at the opposite direction (odd mode).

Ringback
Ringback is when a signal rising edge crosses beyond the Vih threshold and re-crosses threshold again before settling beyond Vih. Depending upon the magnitude and duration of the re-crossing, the settling time may need to be calculated from the final crossing of Vih. This also applies to signal falling edges re-crossing Vil before settling below Vil. For a clocked signal, ringback is typically allowed as long as the signal settles beyond the Vih/Vil threshold to satisfy the setup timing requirement.

Rise Time
Rise time is the time for a signal to change from a logic low state to logic high state. This may also include partial transitions as well (10% ~ 90% amplitude change, or rise through specific voltage thresholds, such as 0.5V ~ 1V).

Skew
Skew is the difference between two or more signals in their delay at a specified voltage threshold. For a common clock circuit, skew may be critical between a driver and receiver clock to determine setup or hold time impact. For a source-synchronous system this can apply to strobe vs. signal or strobe vs. strobe.

Tco (Clock to output valid delay)
Tco is the delay between component clock input (at a specified input voltage threshold) and a valid signal output (at a specified reference load and output voltage threshold). This delay for system design is typically specified at component package pins or input/output pads.

Th (Signal hold time to clock input)
This is the time required for the input signal to remain valid (above Vih for rising and below Vil for falling) beyond the input clock edge transition of the receiving component. Hold time is used both at receiving components for common clock and source-synchronous timing.

Tsu (Signal setup time to clock input)
This is the time required for the input signal to be settled about Vih (rising) or below Vil (falling) at the receiving component before its input clock edge transition. Setup time is used both at receiving components for common clock and source-synchronous timing.

Vil/Vih (Voltage input low/high)
Vil and Vih refer respectively to the maximum low input voltage for a high to low input transition and minimum high input voltage for a low to high input transition. The input signal needs to remain stable beyond these voltage limits to be guaranteed latched in.

Vol/Voh (Voltage output low/high)
Vol and Voh are the low and high, respectively, voltage levels guaranteed at the driver output reference point for the driven signal.

Vt (Threshold voltage)
Vt refers to the input threshold voltage which determines whether a high or low state is sensed at the receiver input. In some cases, an input threshold is specified with an additional noise margin or overdriver region specified for timing specification or signal condition requirements.

Resource Center

Internet

SI-LIST (email forum and web archives for SI discussions with 1000+ participants)
- *Email Group*:   to subscribe from si-list or si-list-digest: send e-mail to majordomo@silab.eng.sun.com. In the BODY of message put: SUBSCRIBE si-list or SUBSCRIBE si-list-digest, for more help, put HELP.
- *Web Archives*:   si-list archives are accessible at http://www.qsl.net/wb6tpu

IBIS
- *IBIS-USERS*: email forum for IBIS related discussions. To participate in IBIS discussions, send your email address to ibis-request@vhdl.org .
- *Official IBIS Web site*: http://www.eia.org/eig/ibis/ibis.htm

Other Internet portals that provide SI related information (in alphabetical order)
www.bogatinenterprises.com
www.chipcenter.com
www.dacafe.com
www.ednmag.com
www.eetimes.com
www.pcdmag.com
www.sigcon.com

SI Software Vendor (in alphabetical order)

Ansoft (www.ansoft.com)
Applied Simulation Technology (www.apsimtech.com)
Cadence (www.cadence.com)
Hyperlynx (www.hyperlynx.com)
Incases (www.incases.com)
Mentor Graphics (www.mentorg.com)
Quantic EMC (www.quantic-emc.com)
Sigrity (www.sigrity.com)
Viewlogic (www.viewlogic.com)

Papers

IEEE Conference Proceedings:
EPEP (Electrical Performance of Electronic Package)
ECTC (Electronic Components and Technology Conference)
EMC (Electromagnetic Compatibility) Symposium

IEEE Journal:
CPMT (Components, Packaging and Manufacturing Technology) www.cpmt.org
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EMC (Electromagnetic Compatibility) www.emcs.org

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