对于高速设计，功率和信号完整性对印刷电路板设计人员形成越来越大的挑战，必须在制造印刷电路板原版前直接分析。经过功率完整性和信号完整性分析的印刷电路板，电磁兼容性明显改善。通过配电系统分析，可辨别印刷电路板上的热点，以及改善层间噪声（电源层和地线层之间的噪声）与电源层和地线层之间的阻抗。我们推荐以下方法：降低层间噪声；优化电源层和地线层之间的阻抗；最大限度降低串扰和反射；改善SSO响应；减轻边缘辐射。

Using SIGNAL INTEGRITY ANALYSIS to Achieve EMC

SI and EMC engineers usually take different routes to get to the same destination. Now EMC engineers may not have to spend so much time out on the test range.

by VISHRAM PANDIT, JOHN RYMKIEWICZ, ROBERT DAVIS and RAJ RAGHURAM

In the area of high-speed design, power and signal integrity pose increasing challenges to PCB designers. It is necessary to analyze the power and signal integrity issues at the upfront design level before the prototype board is fabricated. Electromagnetic compatibility (EMC) improves significantly for a board that undergoes power integrity and signal integrity analysis. Typical signal integrity issues are reflections and crosstalk; typical power integrity issues are power supply system input impedance, simultaneous switching noise, PCB resonance, decoupling capacitors placement, and edge radiations[1].

Power distribution systems (PDS) play an important role in power and signal integrity and electromagnetic interference (EMI). It is necessary to analyze the input impedance between power and ground and further provide an equivalent circuit model for signal integrity analysis. Simultaneous switching noise must be simulated in the time domain with nonlinear IBIS drivers and receivers[2]. Here we will discuss how to design boards for EMC considerations based on first designing for signal and power integrity.

EMC becomes a challenge when dealing with electronic designs with fast rising edges. Manufacturers need to comply with emissions regulations mandated by the Federal Communications Commission and the European Union. With an increase in speed and reduced board size, the traditional EMI design methods are becoming inadequate. The different types of EMI include radiation from connectors, cables, traces and the board edge. EMI is influenced by originating sources, coupling phenomena and radiating elements. The causes of source-level EMI include differential- and common-mode currents. Researchers have established various beneficial EMI design rules[3,4]. Some rules include:

- Use decoupling capacitors between power and ground. Use multiple caps in parallel depending on the frequency of the IC in consideration. Select a capacitor based on its self-resonant frequency (SRF).
- Terminate adequately the high-frequency clock lines.
- Back off the power plane from the edge of the board.
- Filter out connectors.
- Use stitching vias at the board edges.
- Use ferrites for decoupling power planes from power pins.
- Tightly couple forward and return path currents for critical nets.

Once the PCB design is outlined and the layout is done, it becomes essential to analyze the performance of the design. Power and signal integrity analysis has a direct impact on EMI performance. Power and signal integrity design help mitigate the EMI at the source level. We used a five-step process to improve EMI by analyzing and improving signal and power integrity:

1. Reduce inter-layer noise.
2. Optimize impedance between power and ground.
3. Minimize crosstalk and reflections.
4. Improve simultaneous switching output (SSO) response.
5. Alleviate edge radiation.

Interlayer noise is the noise between the power and ground planes of the structure. A way of simulating this noise is to place a Gaussian source or pulse to excite the region between the planes. The pulse propagates from the source location to the edge of the board, gets reflected, comes back, and so on. Over a period of time, the peak noise or voltage at each location between power and ground can be plotted and visualized. It is possible to see, for example, that the voltage is markedly lower where decoupling caps or shorting vias

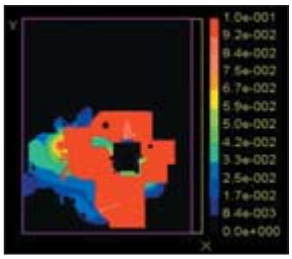

FIGURE 1. Interlayer noise shown in a 2.5 V plane used in satellite communications systems with no capacitor connected.

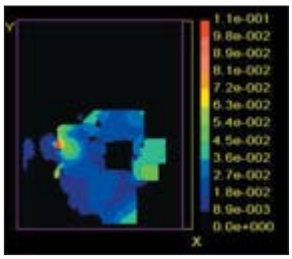

FIGURE 2. The same board after adding decoupling capacitors, shorting vias and other modifications.

are present. It provides a methodology for placing decoupling caps and/or vias to reduce power/ground noise. If the profile of the current drawn from power and ground of the various ICs on the board is known, this can be used to excite the power/ground region and measure the noise instead of the Gaussian source.

FIGURE 1 shows the interlayer noise for a 2.5 V plane used in satellite communications systems. (Screen shots taken from Sigrity Speed2000 analyzer except Figures 6 and 7.) No capacitor is connected. Next, from the analysis of interlayer noise, the following were optimized:

- The number of capacitors between power and ground.
- ESL of the capacitors.
- Placement of the capacitors.
- Ground plane structure, continuous vs. slotted.
- Power plane structure.
- Thickness of the board at different layers.
- Material properties of the board (e.g., loss).
- Shorting vias.

FIGURE 2 shows the improvement after putting in decoupling capacitors, shorting vias and other modifications.

The same methodology of using a Gaussian source to excite the power/ground region can be used to calculate the power/ground impedance. Usually, this impedance is designed to be below a certain value over the frequency range of operation. A time domain simulation is performed as in Figure 1 above. However, we must consider the Fourier transforms of the voltage across the source and the current through the source. The ratio gives the impedance as a function of frequency. Assume, as an example, that the system can tolerate 0.5 V of power/ground noise and that 0.5 A of high-frequency current is being switched. This would mean that the impedance should be less than 1Ω (0.5 V/0.5 A) over the frequency range of operation.

FIGURE 3 shows the impedance response of the original board without the capacitors. **FIGURE 4** show the impedance improvement after adding decoupling capacitors, shorting vias and the other modifications used in Figure 2. For EMI, the PDS impedance shall be low for frequencies below 1 GHz.

Signal Integrity Considerations

Much of what's been covered so far relates to power/ground noise or power integrity, i.e., the effect of having a fluctuating power supply voltage. But even if the power supply is ideal, the board must first satisfy the conventional signal integrity criteria. The lines must be properly terminated in order to minimize reflections, and crosstalk between adjacent traces must be kept within limits. This analysis is done using transmission line theory that involves solving the telegrapher's equations in time domain along with the nonlinear loads and drivers. Terminating lines and minimizing reflections is easier to do and there are well-known techniques such as series termination, parallel termination, Thevenin termination, etc. It is important that this be done first, before the more difficult power integrity issues are handled.

In our case, simulations are performed for data bus going from the processor to the SDRAM. The impedance of the traces is 70Ω. A series termination of 15Ω is added to get a smooth transition at the receiver end assuming ideal supplies. The data bus is bi-directional and a series termination ideally required a termination at both ends; i.e., two resistors per data line. (At a later stage in the design, we decided to leave out the terminations and live with the poorer signal quality.)

The ultimate test for the board is to consider some worst-case scenarios and ensure that the waveforms at all parts of the board meet the specifications. This is typically accomplished by switching a large number of drivers at the same

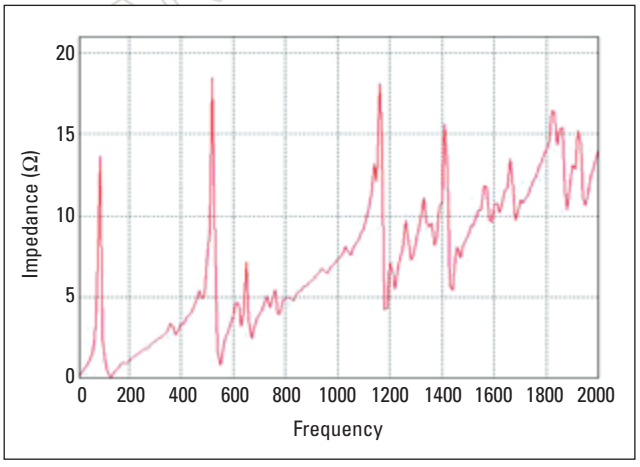

FIGURE 3. Impedance response of original board, sans capacitors.

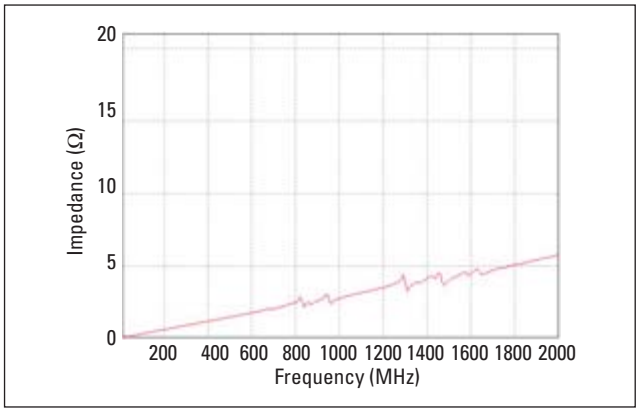

FIGURE 4. Impedance improvement after adding decoupling capacitors, shorting vias and other modifications used in Figure 2.

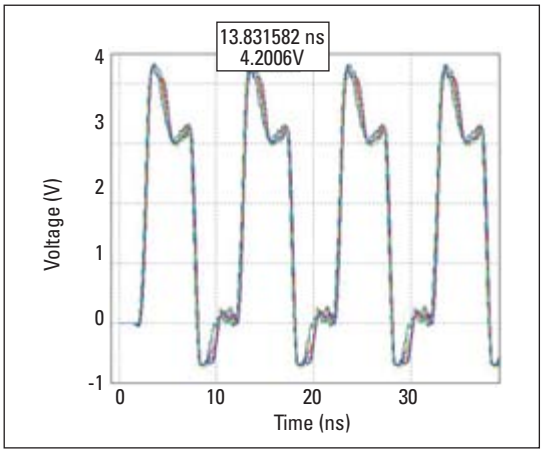

FIGURE 5. SSO for the data bus using IBIS models for the processor and the SDRAM, and the non-ideal power and ground planes are modeled. Worst-case scenario occurs when the data bus is switching simultaneously on all the clock cycles.

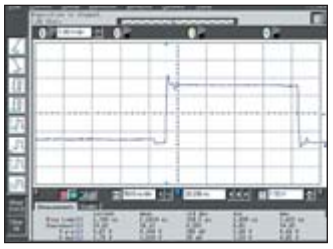

FIGURE 6. Oscilloscope data line D11 shows overshoot similar to that found in the simulations.

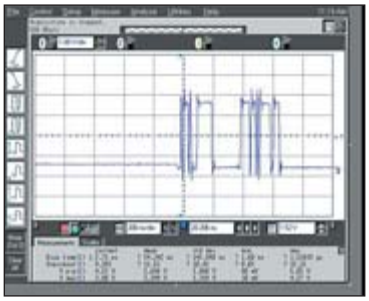

FIGURE 7. Oscilloscope data line D14 also indicates overshoot similar to simulations.

time. For example, one may switch 62 lines of a 64-bit bus at the same time. One of the remaining two lines may be a victim line (quiet line) with the output low and the other may be a victim line with the output high. If the waveforms on the quiet and driven lines or nets are acceptable, then the board is probably OK. Here we used IBIS models for the drivers and receivers and did a complete analysis of the board with 16 drivers switching.

FIGURE 5 shows the SSO for the data bus. IBIS models for the processor and the SDRAM are used, and the non-ideal power and ground planes are modeled. The worst-case scenario is observed where the data bus is switching simultaneously on all the clock cycles. The oscilloscope measurements shown for data line D11 in FIGURE 6 and for data line D14 in FIGURE 7 indicate that the overshoot is very similar to that found in the simulations. The difference between the switching periods is attributed to the data not switching at every clock cycle, and the period is much larger.

There are two sources of radiation from a board. The first is trace radiation from the top and bottom layers of the board. Assuming the planes corresponding to these traces are ideal, the differential-mode radiation can be calculated from the trace currents. In our case, the microstrip traces carried very little current and the trace radiation was negligible. A second source of radiation is edge radiation. Fields in the region between power and ground travel to the edge of the board, where they radiate. Any non-idealities in the planes such as holes, finite impedance, etc., translate into power/ground noise and edge radiation. The edge radiation is therefore directly related to power/ground noise and power integrity of the board. A board with good power integrity automatically has lower power/ground noise and lower edge radiation.

The edge radiation is also simulated for the SSO case. All the bus lines of the data bus are switched simultaneously to represent the worst case. This is a relative analysis because other components contributing to EMI are excluded. The outer cover is not modeled. FIGURE 8 shows the edge radiation for the SSO case. FIGURE 9 shows the design after being modified to improve EMI performance due to SSO. The modifications include patches on the power and ground plane, shorting vias and decoupling capacitors. The modifications are implemented on the board as much as possible.

It must be noted that because this is a relative analysis, it does not guarantee that the board will pass EMI. There are other factors such as coupling phenomena and radiating elements that contribute to EMI. Also, these simula-

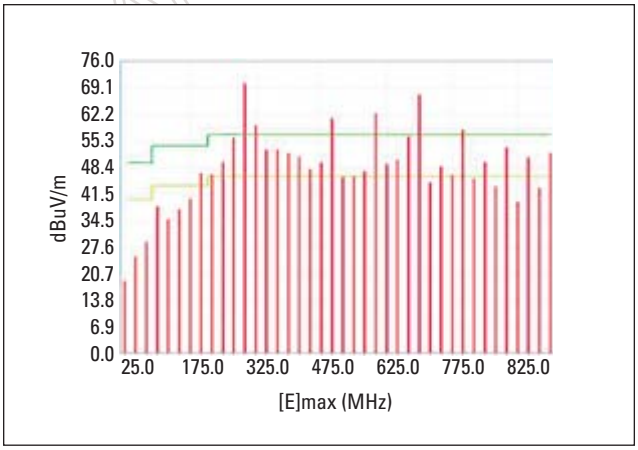

FIGURE 8. Edge radiation for SSO, before modification.

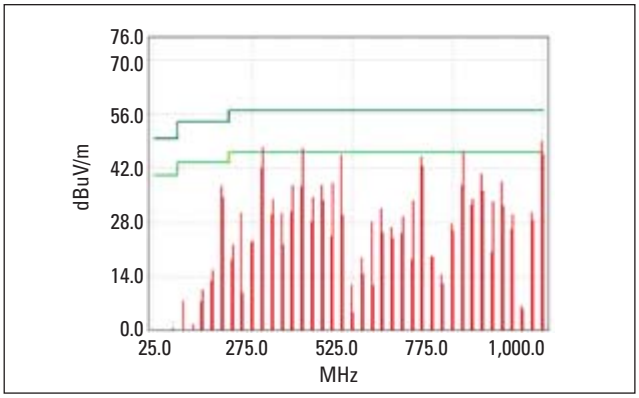

FIGURE 9. Edge radiation for SSO after EMI modifications, including patches on the power and ground plane, shorting vias and decoupling capacitors.

tions are only for one particular area of the board. When all the circuitry on the board is active, the radiation may increase. On the other hand, the properly designed outer cover may help reduce EMI. The purpose of the modifications based on these simulations is to ensure that the source-level EMI is mitigated as far as possible for that particular circuitry. The debug time in the lab was minimum, which can be directly attributed to the improvement in power and signal integrity upfront.

Conclusions

Upfront power and signal integrity analysis help improve EMI performance. With the PDS analysis, the hot spots on the board are identified and interlayer noise and impedance between power and ground are improved.

The SSO simulations are performed with non-ideal power and ground planes. The edge radiation due to SSO is improved by varying different parameters on the board.

The following modifications are implemented based on the simulations:

- Power plane structure is analyzed. It must be continuous. The location of power planes is optimized. It needs to be backed off from the edge of the board.
- Ground plane continuity is analyzed and implemented. Ground patches and islands are optimized.
- Decoupling capacitor placement is carefully chosen.
- The number of required decoupling capacitors is determined. Apart from the power lines of the ICs, they are also used throughout the board, wherever interlayer noise is higher.
- Capacitors are chosen based on their value, ESL and SRF. These parameters are varied and optimized.
- SSO response is analyzed and improved. Overshoots and ringing is minimized wherever possible.
- Shorting vias are implemented wherever necessary. Stitching vias are used at the edges of the board. PCD&M

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