Serial Link Engineering: A Novel Jitter/Noise Metric to Qualify Channel Components

Kumar Keshavan, Tariq Abou-Jeyab

Sigrity Inc.
4675 Stevens Creek Blvd., Santa Clara, CA 95051 USA
ckumar@sigrity.com
tariqa@sigrity.com

***Abstract*—System Interconnects are increasingly dominated by serial links. Understanding the contribution of different system components to jitter and noise, and subsequently tuning those components, is the key to a successful design. In this paper we're proposing a novel eye-area based normalized jitter and noise metric. We show how this metric can consistently be used for different data rates, to offer insight into various components and to identify the ones that are limiting the design. The study also reveals how seemingly small structures and device parasitics can non-linearly increase their jitter and noise contribution to the overall system.**

I. Introduction

The accuracy of any channel or serial link simulation relies heavily on how good the model is for each channel component. By channel we're referring to the path from transmitter to receiver, and may include components such as backplanes, packages, add-in cards, connectors and any other passive component. In this paper we'll be focusing on a single-channel topology, but the methodology is applicable to multi-channel system which can include crosstalk. Fig. 1 illustrates the single-channel topology.

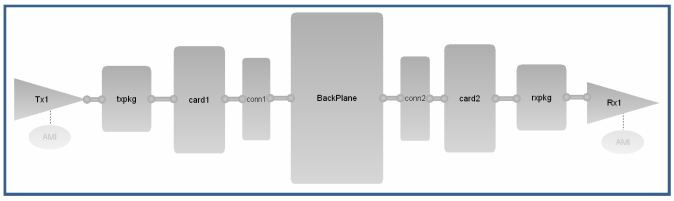

Figure 1. Single-channel topology

Each channel component plays a role in the overall performance of the system, and assessing their contribution is a key to a successful design.

One popular design metric that is used in channel analysis is Bit Error Rate or BER based on the Dual Dirac method **[1, 2]**. Another is Signal Interference Ratio or SIR **[3]**. Those two methods have been explored, along with a new eye-area based normalized jitter and noise metric, which is introduced in this paper. We have found in this study that the latter method is best suited for design assessment of system interconnects.

In the following sections we will describe this method and show how different components in a system contribute to jitter and noise. We also track how their contribution change with increasing data rate. This behaviour will provide guidance on which components are the ones to focus the design efforts on.

II. System Components

As shown in the introduction, the single channel system is comprised of the following components:

TABLE I
Single Channel Components

Component	Circuit model
Tx, Rx	Tx – Nmos output driver behavior model Rx – simple input behavior model
Txpkg, Rxpkg	Flipchip package (s4p)
Card1, Card2	Approx. 3in daughter card; w-element model
Conn1, Conn2	VHDM distributed circuit connector model
Backplane	24in XAUI type channel (s4p)

Fig. 2 shows the behavior model of the output stage of the transmitter (Tx). For clarity only the single ended portion is shown. In real circuit implementation, this model is usually implemented with a bank of nmos drivers. The number of nmos drivers and their strengths will determine the single-level output of Tx.

The key points to note here are: (1) during switching the nmos driver will present a *time varying impendac*e. (2) The output capacitance of the driver will present *frequency dependent impedance*. The combination of (1) and (2) will present a non-ideal termination to the system.

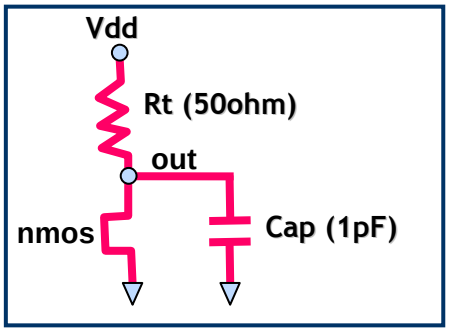

Figure 2. Single ended Tx

A single ended Rx is illustrated in Fig. 3. Similarly to Tx, the input impedance is frequency dependent.

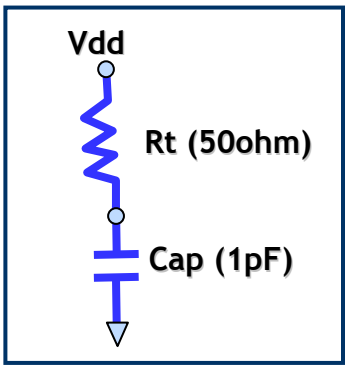

Figure 3. Single ended Rx

As can be seen Tx and Rx constitute impedance discontinuities. The effect of that will get worse at increased data rates.

Similar discontinuities can exist at different parts of the system, such as cards, connectors and vias.

III. Measurement Metrics

Our focus in this study was design assessment of how to quantify the contribution of each component to overall system noise and jitter.

We looked at three different types of metrics:

A. *Bathtub and Bit Error Rate (BER)*

One of the best known methods to derive BER is Dual Dirac method from bathtub curves. Based on Gaussian tail extrapolation, the bathtub curve can be characterized by its intersection and slope. The intersection is proportional to deterministic jitter; whereas the slope represents random jitter. Fig. 4 shows an example of the bathtub curve **[4]**.

One of the major problems with this method is that it only looks at one slice of the eye, which is usually at the midpoint voltage level. We can extend it to include noise at the centre of the eye, but still is not comprehensive, since it doesn't look at the entire eye.

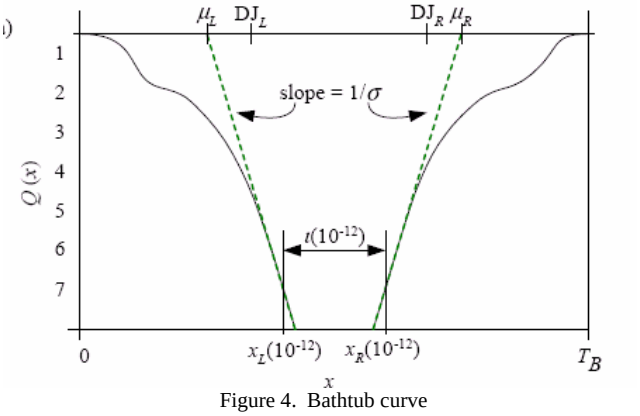

Figure 4. Bathtub curve

B. *Signal Interference Ratio (SIR)*

It's defined for a specific data rate, and it's fundamentally a method to measure the quality of the pulse response in the system.

The pulse response is divided into a portion constituting the signal and other constituting the noise. The ratio between the signal and noise energies is defined as the Signal Interference Ratio or SIR **[3]**. Fig. 5 illustrates the pulse response with the signal and noise portions.

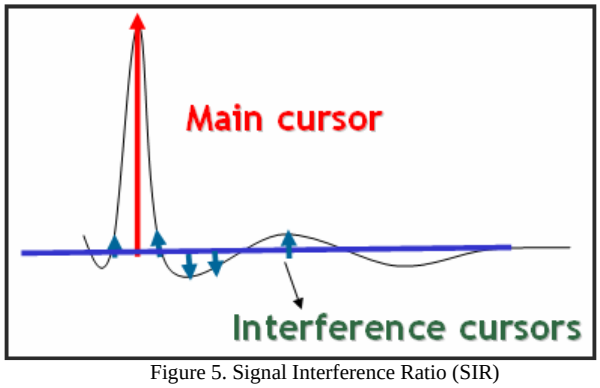

Figure 5. Signal Interference Ratio (SIR)

We found this method very useful in assessing filter performance at a particular data rate. It was not very useful in comparing performance at different data rates.

C. *Normalized jitter and noise (NJN)*

One of the well understood and useful metrics used to assess system performance is the eye opening. The conventional scheme for the eye opening is inconsistent in that only the time scale is normalized.

We created a normalized jitter and noise metric by using the entire area of the eye (Total area) as the normalizing parameter.

The normalized jitter and noise can be defined as:

NJN = 1- (Eye area/Total area).

Total area and Eye area are shown in Fig. 6. Note that the Total area includes the Eye area. The eye area used in this NJN metric reflects deterministic jitter contribution.

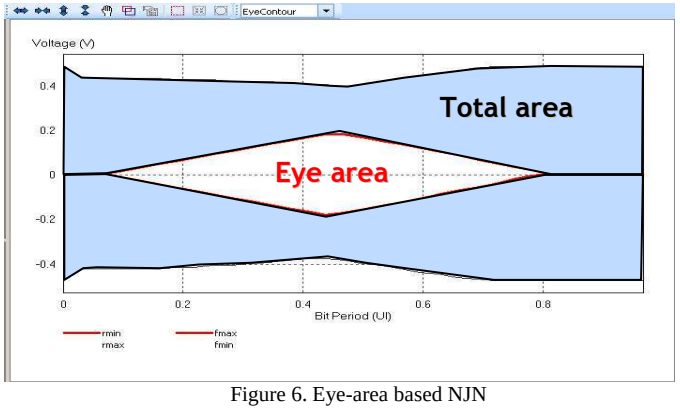

Figure 6. Eye-area based NJN

We've looked at other methods as well, such as BER, but it did not provide consistent results, especially when removing the backplane from the system.

In our study the NJN metric performed extremely well in systems consisting of different components and different data rates.

IV. Simulation Methodology

The goal of this study is to find out the effect of each system component on jitter and noise. We used a "subtractive" methodology to examine each component's contribution.

We started with a reference system as shown is Fig. 1. Then we *swept* each component model, one at a time. For example, for passive components we substituted the real model with a short circuit one. In the case of Tx and Rx, we assessed their contribution by swapping the real models with ones without parasitics.

We studied the system for three different data rates, 2.5Gbps, 5Gbps and 8Gbps. Our system used channel simulation technology to allow high bit rate simulation. In our case we used 200,000 bits.

The channel simulation platform is illustrated in Fig. 7.

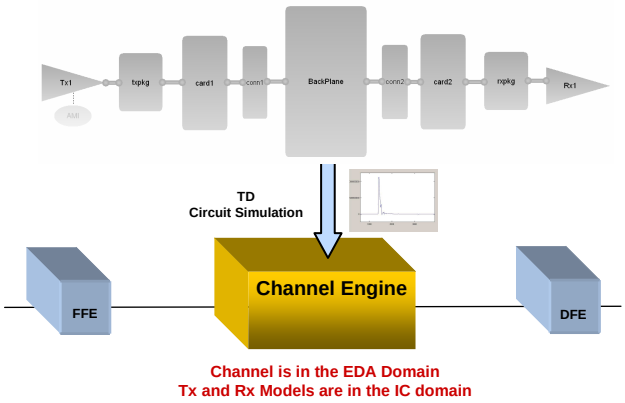

Figure 7. Channel simulation platform

In order to use our NJN metric at any data rate we need to have a non-zero eye opening. At high data rate that's only possible if using equalization.

In our study we used Feed Forward Equalizer (FFE) at the transmitter (Tx). The FFE used was an AMI model, which automatically optimized the filter for the channel.

AMI stands for Algorithmic Modeling Interface. This interface has been standardized recently by IBIS **[5]**.

AMI models are usually written in high-level languages, and offer many advantages over circuit level models. Unlike the circuit level models, AMI models are architecture centric and look at the device from the top down. Such an approach makes those models highly efficient and can be orders of magnitude faster than circuit level models, without loss in accuracy. Moreover, it can have built-in optimization as in the case of the FFE model used here, which automatically optimizes the filter coefficients for the best eye opening.

V. Simulation Results

The simulation results for the three data rates have been condensed into three pie charts as shown in Fig. 8, Fig 9 and Fig 10. Each pie chart shows the normalized jitter and noise contribution from each component in the system.

A simple frequency domain analysis would lead one to conclude that the backplane should be the dominant contributor to eye closure.

Examining the normalized jitter and noise data shows a different picture. In low data rates, the backplane is indeed the dominant contributor to jitter and noise in the system. However; as the data rate increases, the contribution of the "rogue" elements of the system has been observed to increase disproportionately.

For example, the effect the parasitic capacitance of the Tx and Rx increases 6 times, when the data rate doubles from 2.5Gbps to 5Gbps. Similarly, the connecter increases its share from 1% to 10%.

Overall from 2.5Gbps to 8Gbps, the percentage contribution from smaller structures increases at the expense of contribution from the backplane. Most likely this behavior can be attributed to discontinuities.

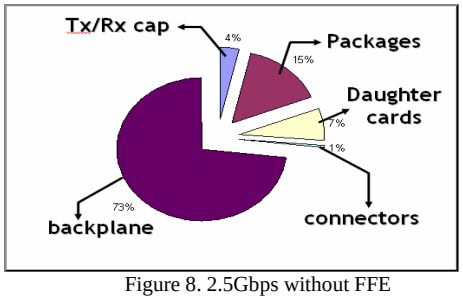

Figure 8. 2.5Gbps without FFE

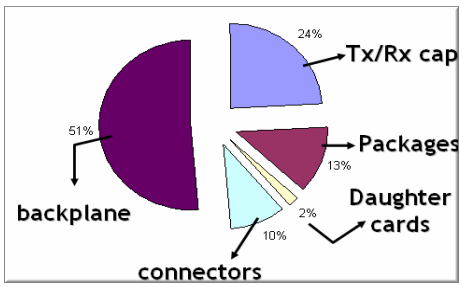

Figure 9. 5Gbps with 5 tap FFE

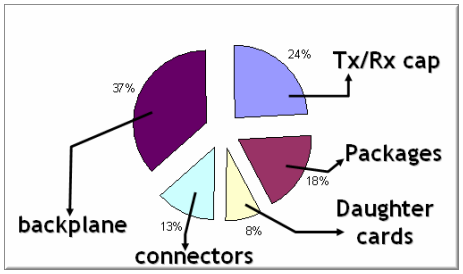

Figure 10. 8Gbps with 5 tap FFE

It should be noted that the absolute jitter values obtained from this "subtractive" methodology, are not additive, i.e, you

cannot linearly combine the jitter values of the components to get the total system jitter.

Our preliminary study indicates that a non-linear function addition will lead to a total jitter to component jitter relationship. Further work is required in that area.

VI. Conclusion

We have developed a quantitative metric, to assess system components and provide a rational basis for system design. Using this metric we've shown how small structures can have a dramatic effect on high data rate system performance.

References

[1] http://www.stateye.org/

[2] Stefan Sercu and Jan De Geest, *"BER Link Simulations", DesignCon, February 2003*

[3] Bilal Ahmad, "*Performance Specification of Interconnect*", *DesignCon, February 2003*

[4] Ransom Stephens, *Jitter analysis: The dual-Dirac model, RJ/DJ, and Q-scale, Version 1.0, Agilent Technologies, 31-December-2004*

[5] http://eda.org/pub/ibis/ver5.0/ver5_0.pdf