A review of PCB-level power delivery system

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Power delivery system (PDS) analysis and design have become increasingly important in the communication, networking and consumer electronics industries.

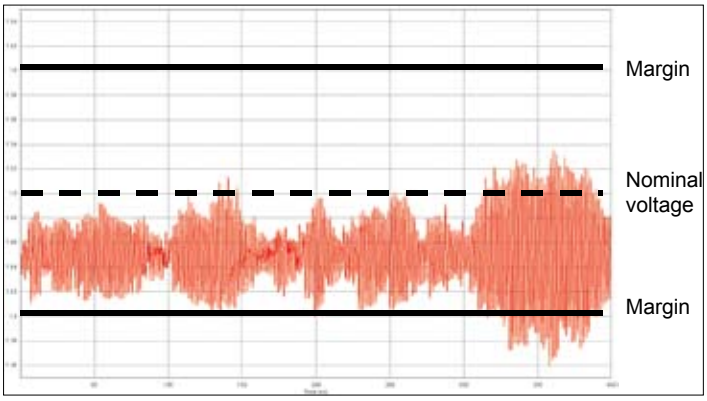

Figure 1: The migration from 130nm to 90nm has shrunk supply voltages to 1.2V and below, and increased currents supplied to devices through the PDS.

As reported by the International Technology Roadmap for Semiconductors, IC power-supply voltage continues to drop with the inevitable scaling of VLSI technology. The migration from 130nm to 90nm has shrunk supply voltages to 1.2V and below, and considerably increased currents supplied to devices through the PDS (**Figure 1**). These developments pose challenges to PDS design–from DC IR drop to AC dynamic voltage fluctuation control–especially as margins get tighter.

A PDS used in high-speed design can be divided into three sections: silicon (on-chip), IC package and PCB (**Figure 2**). The on-chip power-grid structure contains several metal layers with either x or y direction power and ground rails. Vias are used to connect the rails sitting on different metal layers.

For high-performance chips, there are integrated decoupling cells for both core and I/O powers. Like a small PCB, an IC package can have several power and ground plane layers with complex shapes. There are also on-package decoupling sites reserved for small capacitors. The PCB usually has more well-defined solid power and ground planes, large and small discrete caps, and a voltage regulator module. Wire bonds, C4 bumps and solder balls connect the silicon, package and board.

The entire PDS must ensure stable voltages in multiple power domains for power to reach the IC devices at a nominal level. However, there will always be noise induced by switching currents and frequency-dependent distributed parasitics inherent in PDS. The voltage variation can be estimated by the equation $\Delta V = Z\Delta I$, where ΔV is the voltage fluctuation that appears at device end and ΔI is the switching current. Z is the power ground input impedance looking into the entire PDS at the device end. To reduce voltage variations, the PDS must have very low impedance. At DC, such low impedance reflects a low IR drop for the power supply; at AC, such low impedance provides low transient noise generated by switching currents.

PDS and signal distribution system are closely related since power and ground serve as signal return paths and reference planes.

DC IR drop

Much attention has been given to on-chip IR drop in view of the severe resistive loss caused by the small size (a few microns and below) of the chip power grid. Board-level IR drop (in the range of tens to hundreds of millivolts) can have a significant impact on high-performance designs if you:

- Always check your board for "Swiss-cheese" effect, neck-down and dynamic plane cut (**Figure 3**).
- Worry about insufficient pin, via, ball, bump, copper weight for the current paths, or the imbalance of these current paths.
- Design a low-voltage and/or high-current product that has difficulty meeting the voltage drop margin.

For example, higher-density, high-pin-count components have large via fields, and their associated anti-pads create a Swiss-cheese effect on the power distribution layers of both IC packages and PCBs. This effect creates a smaller equivalent conductor of higher resistance. Given the high impedance path of the PDS, insufficient power might be delivered to some devices on the PCB. A good DC IR drop simulation is thus needed to estimate the voltage margin of PDS. Furthermore, through various what-if analyses, it can help formulate design solutions or guidelines during the pre- and post-layout stages. Layout, system, SI and power engineers can also use IR drop analysis as a sign-off tool for design rule checking (DRC) for every power and ground net on all boards, with a comprehensive IR drop constraint manager. This flow can minimize layout issues on complex PDS geometries, which can only be identified by an automated software solution.

Figure 4 shows that IR drop analyses can pinpoint critical voltage and current distribution in the PDS for a high-performance PCB.

Impedance analysis

Most people equate a pair of metal planes with a parallel-plate capacitor. Planes actually provide the "plane capacitance" that helps maintain power-supply voltage stability. At low frequency, when the wavelength is much larger than the plane dimension, the pair of planes does indeed behave as a capacitor.

However, as frequency increases, the planes' charac-

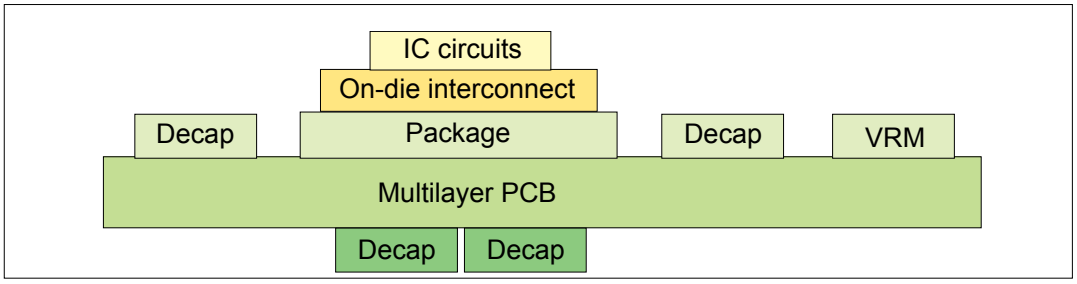

Figure 2: A PDS can be divided into three physical sections: silicon, IC package and PCB.

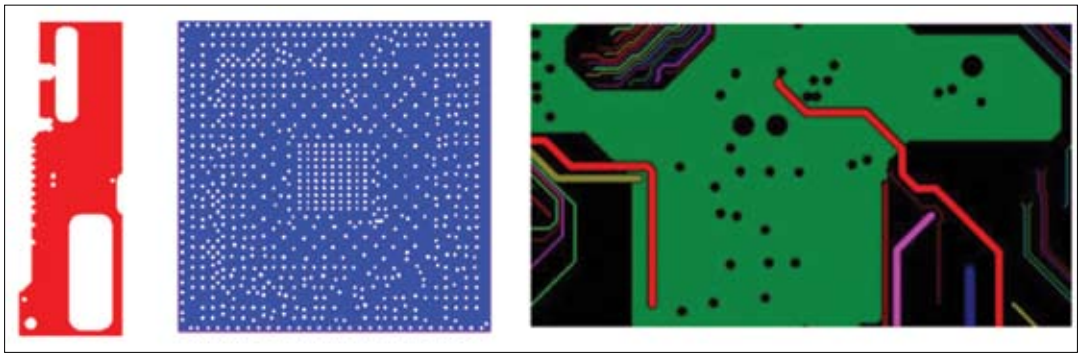

Figure 3: Common physical designs increase current path resistances at PCB level.

teristics become much more complex. More precisely, a pair of planes forms a parallel-plate transmission-line system. Power and ground noise, or the corresponding electromagnetic fields, spread through and follow the rules of the parallel-plate transmission-line system. When the noise wave spreads and reaches the edges of the planes, a small portion of the high frequency energy will radiate, but the larger part of the energy will bounce back. Multiple reflections from different edges of the planes cause the resonance inside the PCB.

Resonance inside the PCB is a distinct phenomenon in AC power and ground impedance analysis. **Figure 5** shows the input impedance of a pair of planes as compared with the impedance of a pure capacitor and pure inductor. The plane size is about 30cm x 20cm with about 100µm plane separation and filled up with FR4 material. The plane capacitance is about 20.9nF, and a VRM mounted on board is modeled as a 3nH inductor. One can see that the planes (without VRM, red curve) behave as a capacitor up to tens of MHz (tracking the blue curve, value going down). Above 100MHz, the impedance of the plane is mostly inductive (value going up and tracking the green curve). At hundreds of MHz range, a number of peaks corresponding to the resonant behavior start to appear, showing the plane is no longer purely inductive.

By now, it is clear that a low-impedance PDS (from DC to AC) is essential for low voltage fluctuation. The design goal for PDS also gets clearer: to reduce inductive effect, enhance capacitive effect and remove/reduce high-value resonance peaks.

To reduce PDS impedance, the following design practices may be applied:

1. Reduce the distance between the power and ground planes.
2. Make the planes bigger.
3. Increase the dielectric constant of the material between planes.
4. Add more power and ground plane pairs.

Due to manufacturing and other design considerations, however, designers often need other methods and greater flexibility to reduce PDS impedance. Adding discrete decoupling capacitors on board is a good alternative, especially in removing resonance peaks within specific frequency ranges.

Figure 6 shows the input impedance of a PDS simulated by Sigrity PowerSI with three different scenarios:

a) Without VRM modeled, without any decoupling capacitors mounted on board
b) With VRM modeled as a short circuit, without any decoupling capacitors mounted
c) With VRM modeled as a short circuit, with some decoupling capacitors mounted

In the first scenario (blue line), the PDS input impedance observed at the IC-chip location shows a capacitive behavior at low frequency. As frequency increases, the first natural resonant peak shows up at 800MHz, corresponding to the physical size of the power ground planes.

In the second scenario (green line), the input impedance appears to be inductive at low frequency, which corresponds to the loop inductance from the IC-chip location to the VRM location. This loop inductance and the plane capacitance together induce a resonant peak at around 200MHz.

In the third scenario (red line), with decoupling capacitors mounted on board, the 200MHz resonant peak is pushed to a much lower frequency range (< 20MHz). With a much lower amplitude, the first strong resonant peak now appears at about 1GHz. This plot illustrates that, by adding decoupling capacitors, PDS achieved low and smooth AC impedance response within the major operating spectrum. Low PDS noise can therefore be expected.

The addition of decoupling capacitors gives an engineer the flexibility to tune the PDS impedance and consequently achieve low power ground noise. However, design issues, such as where to place decou-

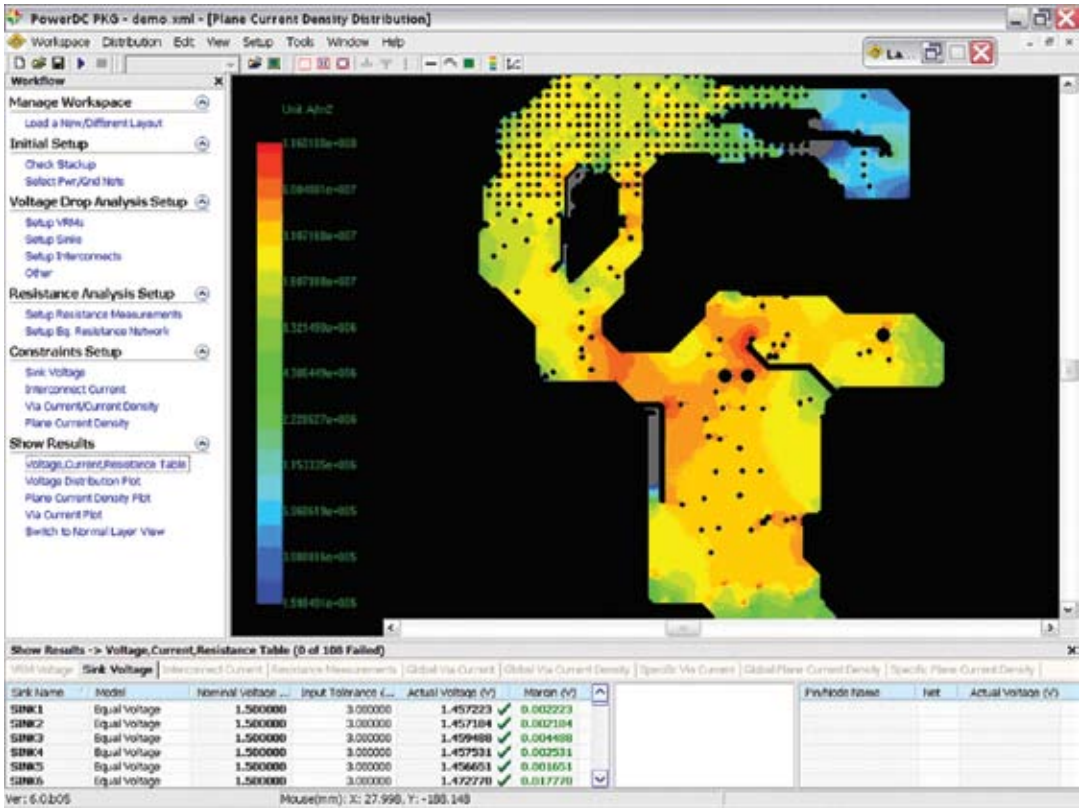

Figure 4: IR drop analyses can pinpoint critical voltage and current distribution in the PDS for a high-performance PCB.

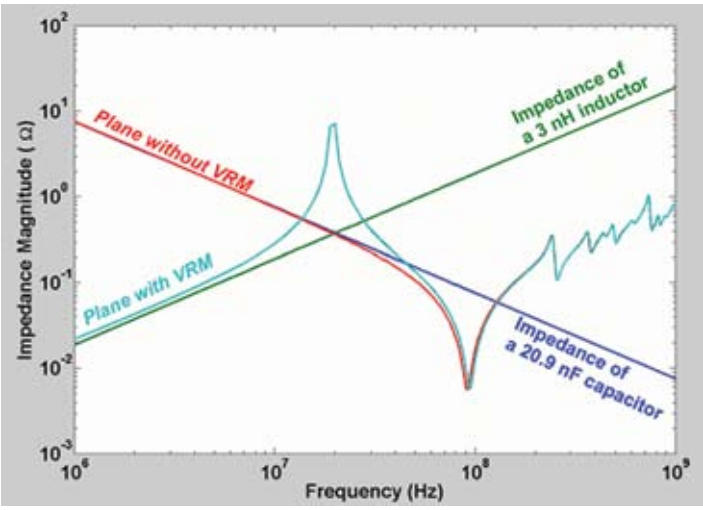

Figure 5: Figure shows the input impedance of a pair of planes as compared with the impedance of a pure capacitor and pure inductor.

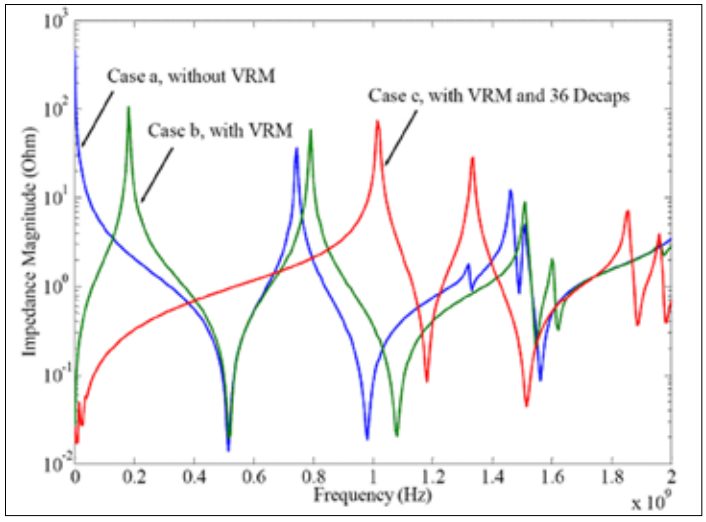

Figure 6: Shown is the input impedance of a PDS simulated by Sigrity PowerSI with three different scenarios.

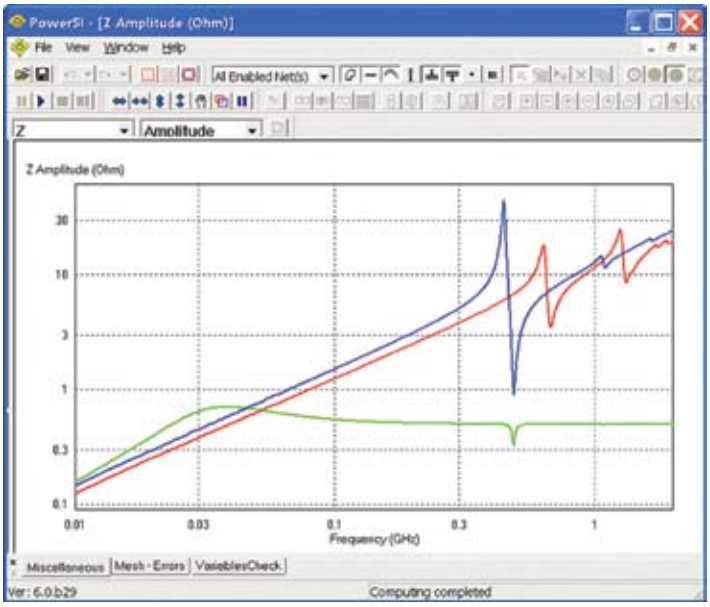

Figure 7: The graph shows input impedance simulation results with different configurations.

pling capacitors, how many should be placed on the board, what type of capacitors should be used, are sure to emerge. Extensive PDS simulations using the right tools are necessary to determine an effective decoupling strategy for a particular design.

Co-design concept

Figure 6 reveals a very important fact: on-board decoupling capacitors can only cover frequency range of up to several hundreds of MHz. Beyond that, the parasitic inductance associated with each discrete decoupling capacitor will greatly reduce the decoupling effect. PDS impedance cannot be further reduced just by board-level capacitors. From several hundreds of MHz and beyond, package PDS capacitance and on-package discrete decoupling capacitors come into play. And for gigahertz range decoupling needs, on-chip power grid capacitance and on-chip decoupling capacitors are the only answer. **Figure 7** shows three cases. The red line represents the input impedance of a board with some decoupling capacitors. The first resonant peak is around 600MHz to 700MHz. After a package is added into the model, the extra package inductance causes the resonant peak to reach around 450MHz as shown by the blue line. Then after adding the chip model, the high-frequency resonant peaks are eliminated by the on-chip capacitance; but a very low and weak resonance is introduced at the 30MHz range as shown by the green line. This 30MHz resonance peak will manifest in the time domain voltage droop as the middle frequency envelope of the high frequency switching waveform.

On-chip decoupling is effective, but it consumes precious silicon real estate and leakage current. Moving certain on-chip capacitance to package level could be a good design compromise, but it requires system-level knowledge from chip, package to board. Typical board-level engineers may not have access to such design data and simulation tools while IC designers usually don't care much about downstream package and board designs. But it is clear that a system-level approach involving co-design of chip-package and package-board will be the future trend in PCB design and analysis.