A Resonance-Free Power Delivery System Design Methodology applying 3D Optimized Extended Adaptive Voltage Positioning

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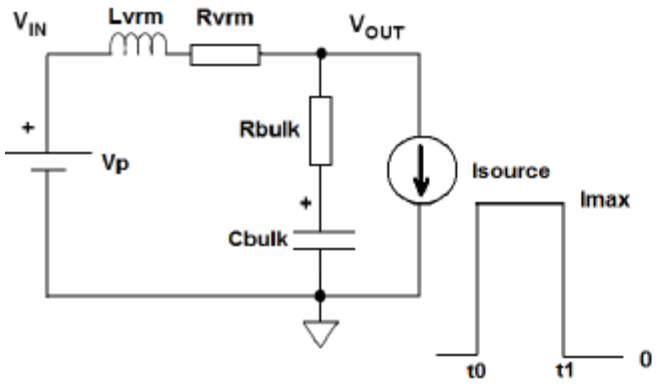
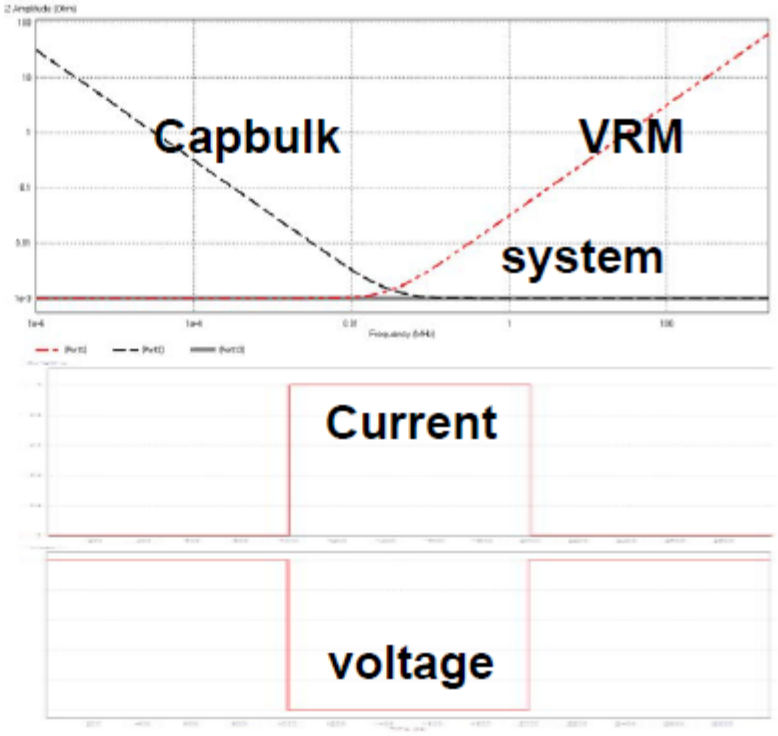
Agenda

- Adaptive voltage positioning (AVP)
- Extended adaptive voltage positioning (EAVP)
- Optimized extended adaptive voltage positioning
  - Method
  - Real case application
- Time domain verification

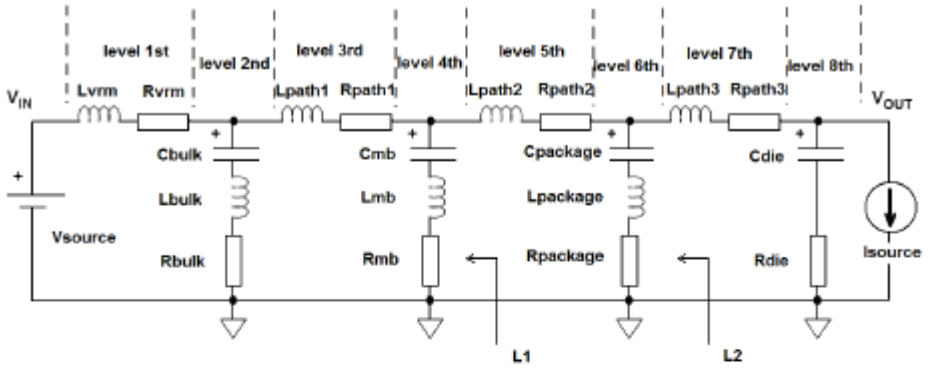
Adaptive Voltage Positioning (AVP)

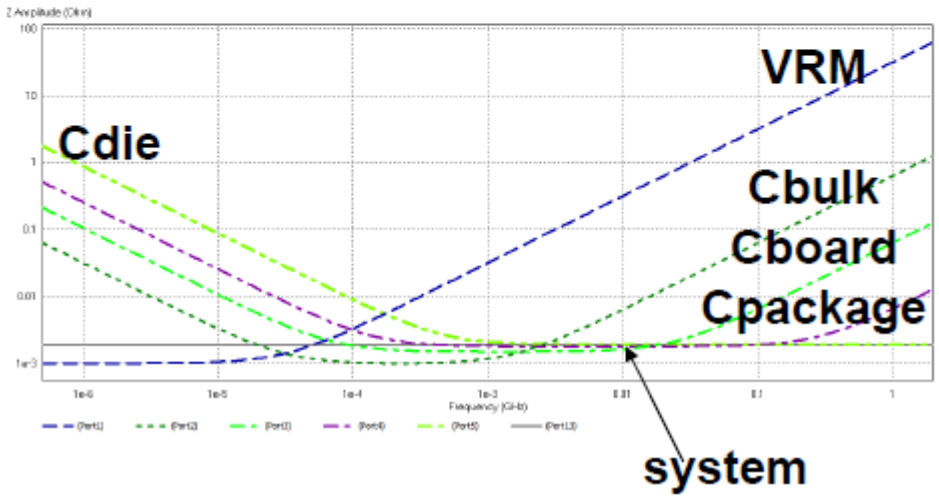




- AVP method was originally proposed to design a VRM with a bulk capacitor
- A flat PDS impedance can be achieved, if the component values are satisfied the conditions: Rvrm=Rbulk, Rbulk*Cbulk=Lvrm/Rvrm

Extended Adaptive Voltage Positioning (EAVP)





- To yield a flat PDS impedance
  - the ESR of decoupling stage N must me be equal to the ESR of decoupling stage N-1.
  - the RC time constant of decoupling stage N must be equal to the L/R time constant of stage N-1.

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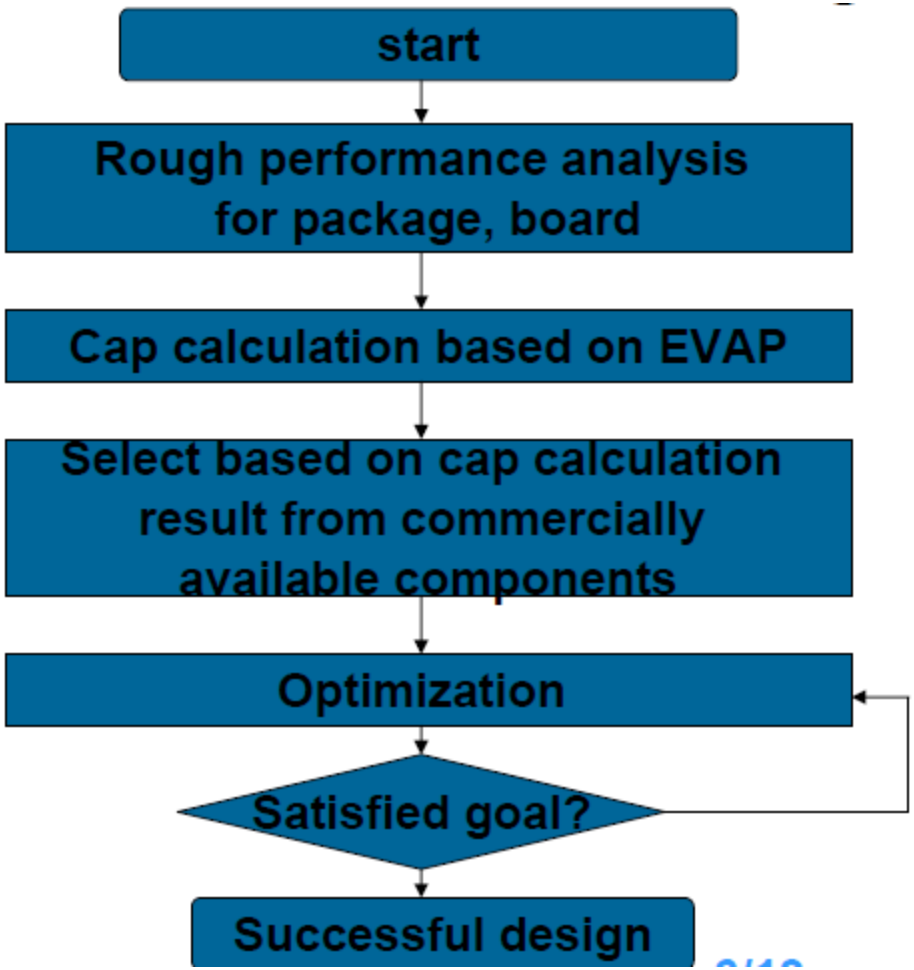
Optimized Extended Adaptive Voltage Positioning—Why

- 1D EVAP circuit topology does not correspond well to the complex 3D nature of a modern PDS.
  - vertically-stacked power planes
  - laterally-distributed decaps
  - Decapsare located on top and bottom of boards and packages.

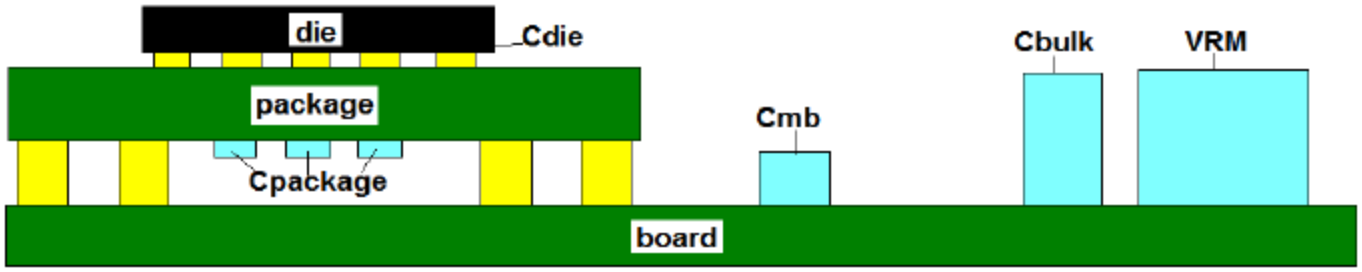
- The RLC element values required at each level of the PDS are often difficult to implement with commercially available components

Optimized Extended Adaptive Voltage Positioning—How



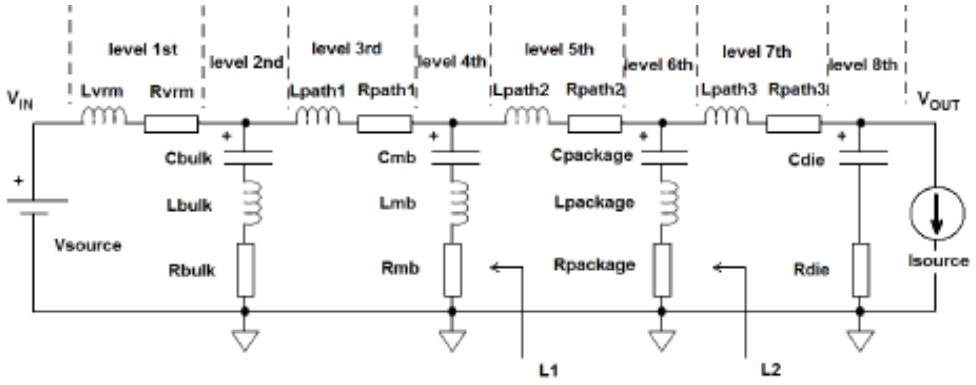
- EAVP was used to select capacitors for the initial PDS design.
- Then 3D EM analysis was applied to characterize the 3D PDS structure with capacitors placement diversity across multiple levels of the PDS (board-package-chip) and the ability to select capacitors from a library of commercially available components

Real system design



- An 6 layer FCBGA package
- An 8 layer board
- A 1 mΩ and 5.4 nH VRM
- Design goal :5 mΩPDS impedance
- Interested frequency range: DC to 2 GHz.

Calculation with EVAP



- Rvrm=Rbulk
- Rbulk*Cbulk=Lvrm/Rvrm
- Rmb= Rbulk+Rpath1=Rvrm+Rpath1
- Rmb*Cmb=(L1+Lpath1)/(Rvrm+Rpath1)
- (Lvrm//Lbulk+Lpath1)/(Rvrm+Rpath1)
- Rpackage=Rmb+Rpath2
- Rpackage*Cpackage=(L1+Lpath2)/(Rmb+Rpath2)
- Rdie=Rpackage+Rpath3
- Rdie*Cdie=(L2+Lpath3)/(Rpackage+Rpath3)

First level system calculation

		Inductance	Resistance	Capacitor
Condition	VRM	5n	1m	
	Path1	3.27n (estimated)	0.5m (estimated)	
	Path2	2n(estimated)	0.3m(estimated)	
	Path3	0.65n(estimated)	0.1m(estimated)	
Result	Bulk capacitor	0.1n	1m	5000u
	Capacitor on motherboard	0.01n	1.5m	1500u
	Capacitor on package	0.001n	1.8m	620u
	Capacitor on die		1.9m	180u

- The result for capacitor is not applicable directly

Real cap lib selection

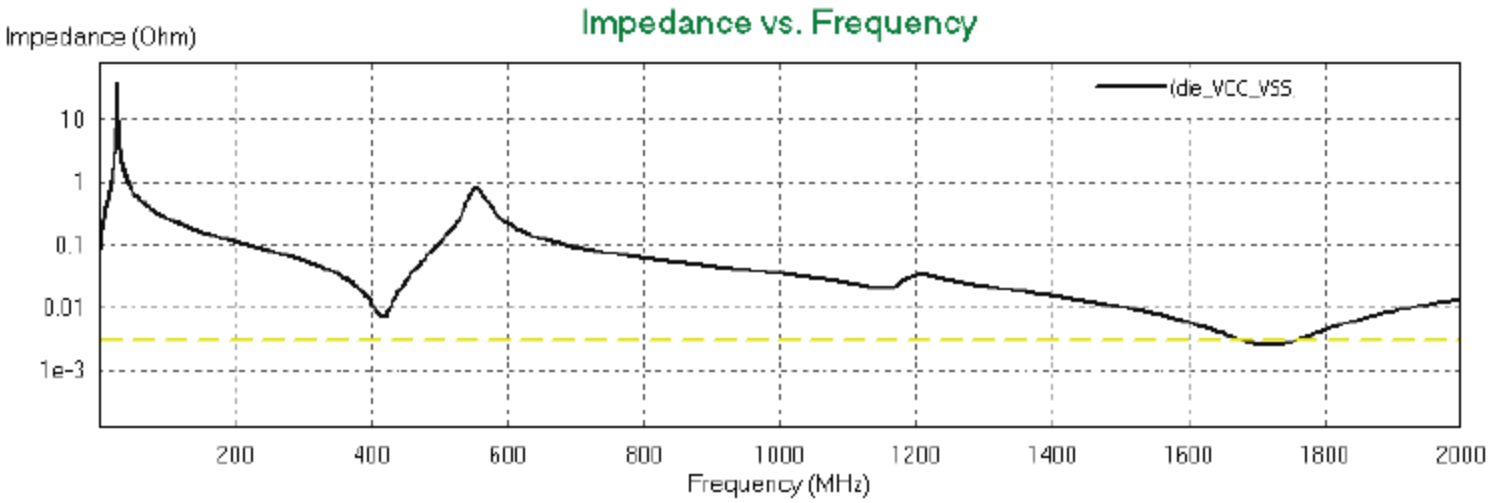
Capacitor Library Manager

Project Library External Library

ID	Part No.	Prefe...	Size	Model Type
1	Cdie1	5	0302	RLC
2	Cdie2	5	0302	RLC
3	Cpackag1	5	0402	SPICE Model
4	Cpacka...	5	0402	SPICE Model
5	Cpackage	5	0402	SPICE Model
6	Cpackge4	5	0402	SPICE Model
7	Cmf1	5	0806	SPICE Model
8	Cmf2	5	0806	SPICE Model
9	Cmf3	5	0806	SPICE Model
10	Cmf4	5	0806	SPICE Model
11	Cmf5	5	0806	SPICE Model
12	Cbulk	5	3030	RLC

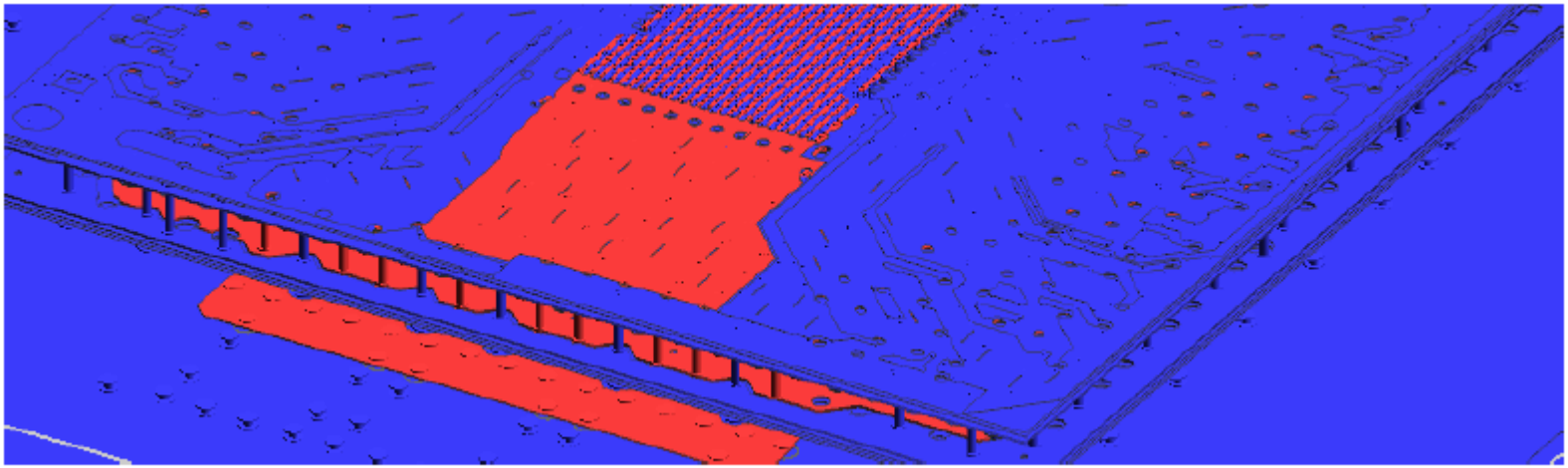
- Several caps were chosen based on EVAP calculation result among commercially available component.

Performance with no cap



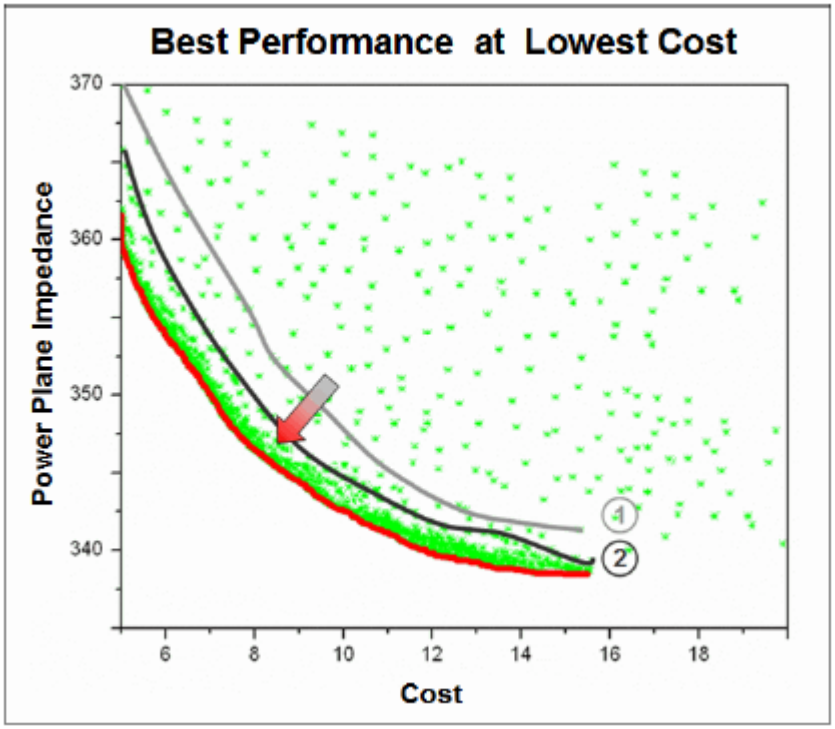
- When no cap was assembled on the system, the system works as above.
- The maximum impedance achieves to 38 ohm

Optimization structure



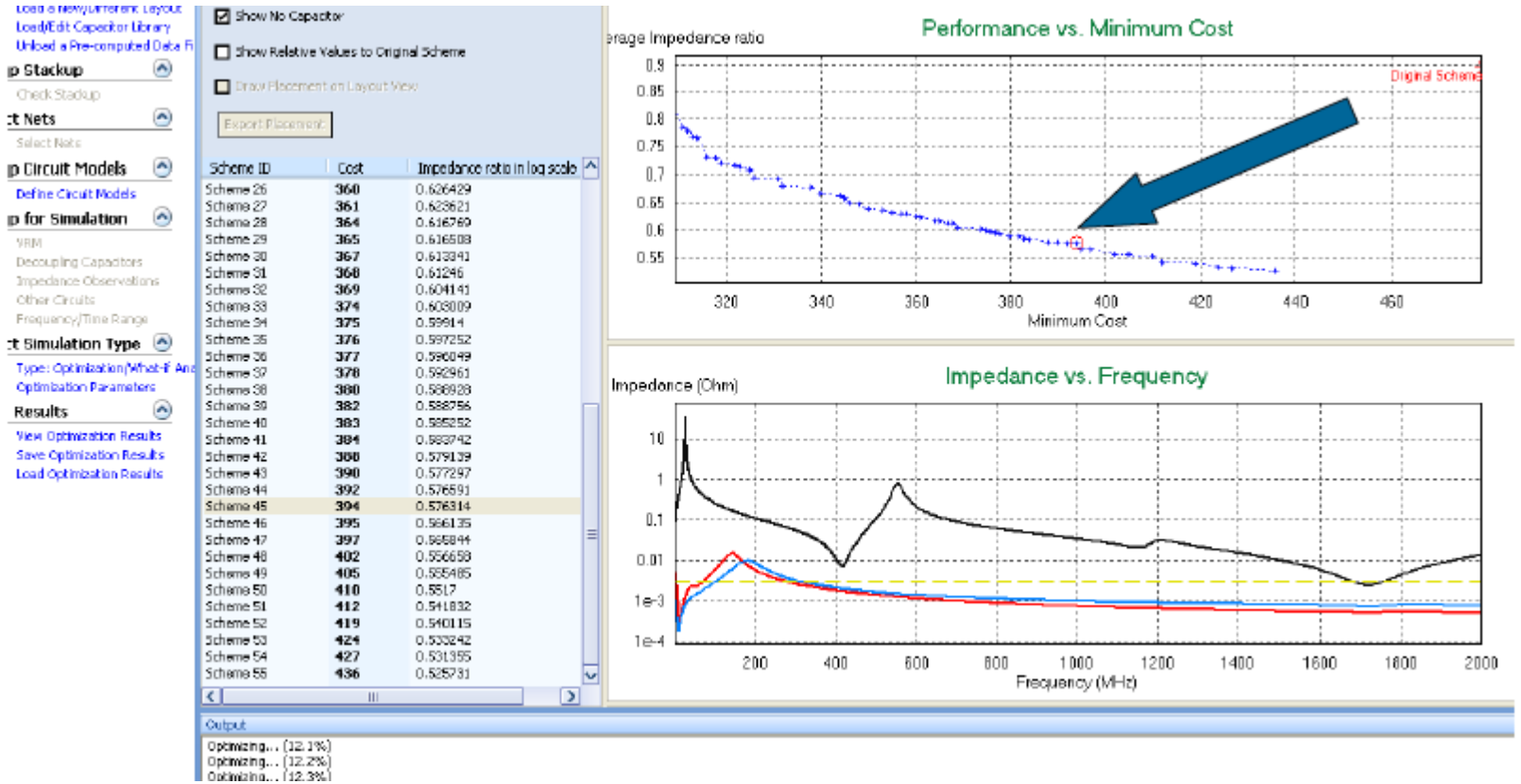
- Whole system including Cdie, package, caps on package, board and caps on board was consider as a whole.
- 3D EM solver was used to do optimization.

Performance vs. Cost



- The best performance vs. lest cost design will be find automatically by OptimizePI.

Optimization process



- Optimization is in processing.
- Several scheme will be provided with different performance and cost.

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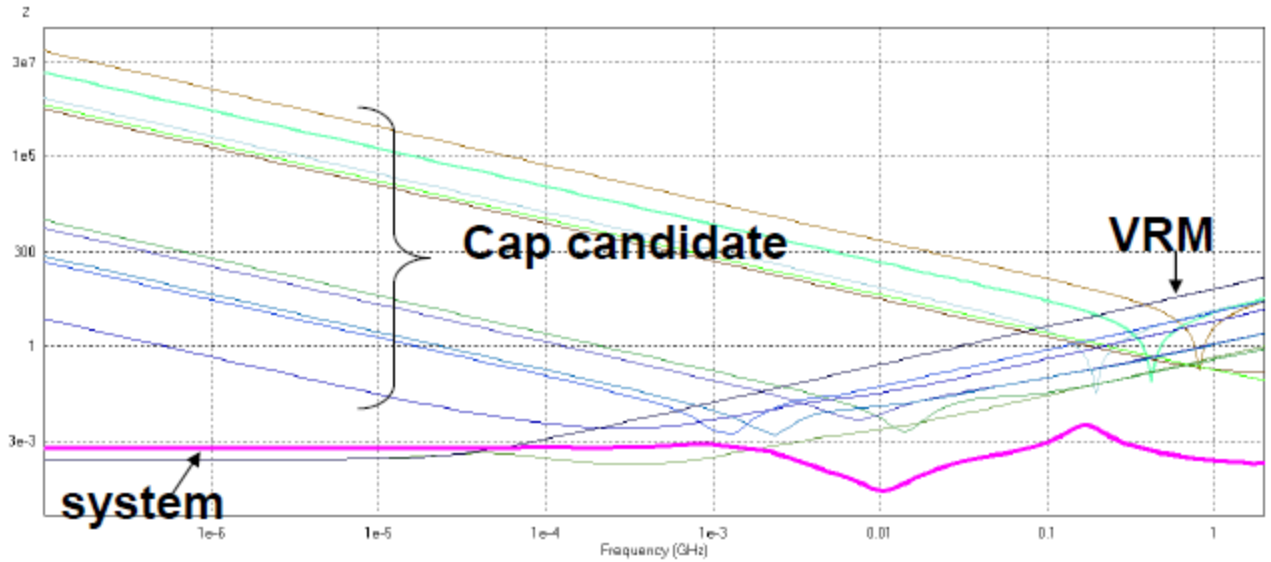
Placement

Scheme ID	Cost	Impedance	C1_1	C2_1	C3_1	C4_1	C5_1	C6_1	C7_1	C8_1	C9_1	C10_1	C11_1	C12_1	C13_1	C14_1	C15_1	C16_1	C17_1	C18_1	C19_1	C20_1	C21_1	C22_1	C23_1
Scheme 1	0.201	19.965131	X	4	X	X	X	X	2	X	2	X	X	X	X	X	4	4	X	X	X	X	X	3	X
Scheme 2	0.202	19.918919	X	X	X	X	4	X	X	4	X	X	X	X	X	X	X	X	X	X	4	3	X	5	3
Scheme 3	0.21	19.725069	4	X	X	X	X	X	X	3	X	X	2	4	X	X	X	X	2	X	X	X	4	5	4
Scheme 4	0.227	19.676452	X	X	X	5	X	X	X	4	X	2	X	X	2	X	X	X	X	X	X	X	X	5	4
Scheme 5	0.229	19.667312	X	X	X	4	X	X	X	X	2	2	4	X	3	X	X	X	X	X	2	X	X	3	4
Scheme 6	0.236	19.539375	X	X	X	5	3	X	X	X	2	X	X	4	X	5	4	X	4	4	X	X	X	X	X
Scheme 7	0.237	19.285003	3	X	X	X	X	X	X	4	X	X	X	2	X	X	2	X	X	X	X	3	4	5	3
Scheme 8	0.246	19.259111	X	X	X	4	X	X	2	X	X	X	X	X	X	X	X	X	X	X	2	X	X	4	4
Scheme 9	0.256	19.194559	X	4	X	X	X	X	2	X	4	X	X	X	X	X	4	X	X	X	X	X	X	3	X
Scheme 10	0.269	18.857856	X	X	X	X	X	2	4	X	X	X	X	3	X	X	X	X	X	X	X	X	X	1	X
Scheme 11	0.335	18.755864	X	X	X	5	2	X	X	4	X	X	3	X	5	2	X	X	X	2	X	X	X	X	X
Scheme 12	0.337	18.73206	X	X	X	X	4	2	4	X	X	X	X	3	3	X	X	X	X	X	3	3	X	1	X
Scheme 13	0.338	18.702451	X	2	X	X	X	X	3	4	X	X	X	X	X	X	4	X	X	X	X	5	2	1	3
Scheme 14	0.35	18.689192	X	X	X	5	X	X	5	X	X	X	X	X	X	X	X	X	X	X	X	3	X	1	3
Scheme 15	0.379	18.624997	4	X	4	X	X	X	X	X	X	X	4	X	X	X	X	X	1	4	X	X	X	5	X
Scheme 16	0.38	18.620311	2	X	X	X	X	4	3	X	X	X	X	5	4	X	X	X	1	X	X	X	4	1	3
Scheme 17	0.382	18.543074	4	2	X	X	X	X	3	X	X	X	X	3	X	X	3	X	X	4	X	X	2	5	X
Scheme 18	0.385	18.516154	X	1	X	X	5	X	X	X	2	X	X	X	X	X	4	X	X	X	2	X	4	X	4
Scheme 19	0.388	18.477548	X	X	X	X	4	4	5	4	4	X	X	X	X	X	X	X	X	X	X	3	X	1	3
Scheme 20	0.393	18.427117	X	X	X	5	X	X	X	4	5	X	X	X	5	2	2	X	X	4	X	X	4	4	X
Scheme 21	0.43	18.411733	3	X	X	X	X	X	X	3	X	2	X	X	X	X	X	X	X	X	5	X	1	3	X
Scheme 22	0.439	18.296769	X	X	X	X	2	2	5	4	2	X	X	X	X	X	X	X	X	X	X	3	X	1	3
Scheme 23	0.46	18.268527	X	X	X	5	X	X	5	X	X	X	X	X	X	X	X	4	X	X	2	3	X	1	1
Scheme 24	0.486	18.241662	X	X	4	X	X	X	4	4	X	X	X	X	X	X	X	X	X	4	X	2	4	1	5
Scheme 25	0.504	18.20095	3	X	5	X	X	2	X	3	X	X	X	X	X	X	X	X	5	3	X	X	1	1	2
Scheme 26	0.514	18.190489	X	5	X	5	X	5	4	X	2	X	X	X	4	X	X	3	3	2	3	X	3	1	X

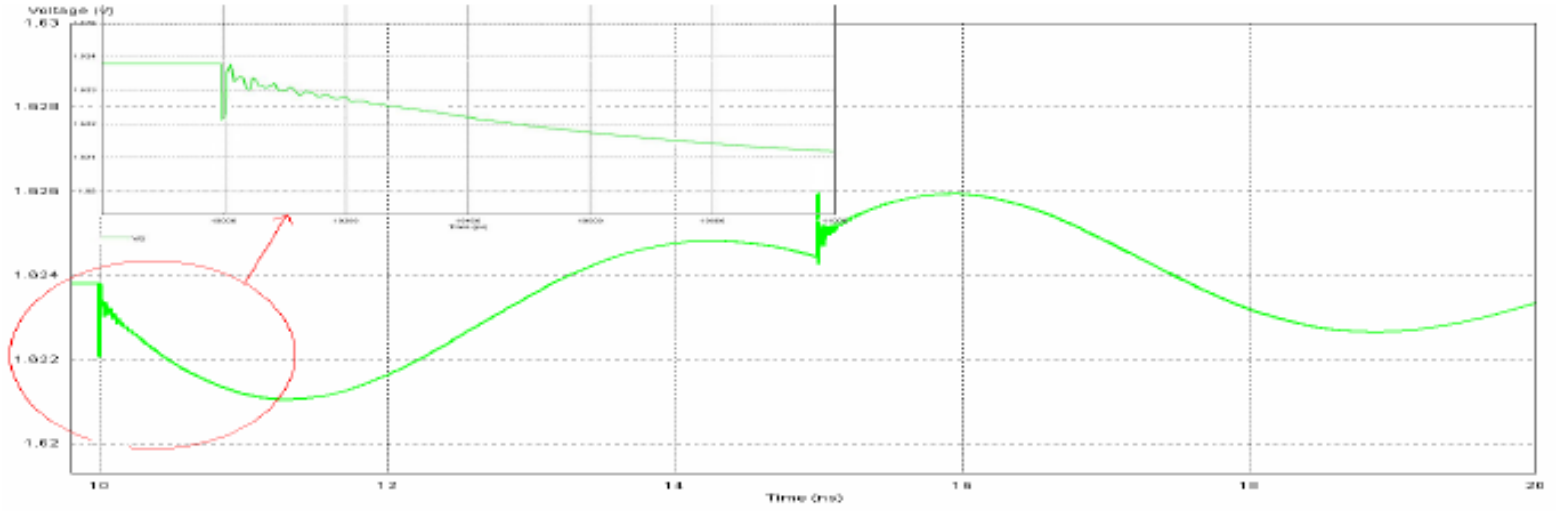
- The placement of every scheme can be output automatically in table format or in spd format.

Final result in frequency domain



- After optimization, a PDS impedance of less than 5 mΩ from DC to 2 GHz is achieved.

Time domain verification



- A step device current source of 1 amp was applied to verify performance in time domain.
- A 50 mV PDS noise voltage results is shown at the active device pins.

Conclusion

- A novel and easily-realized PDS design method was proposed for resonance-free PDS design.
- The 1D EAVP method was used to generate the initial 3D PDS design.
- The initial design was then characterized numerically with 3D EM analysis and subsequently optimized with circuit analysis for maximum performance and minimum cost.
- The time domain noise voltage of this frequency domain Optimized-EVAP method was verified to yield only 50 mV PDS noise.
- This design method is quick and yields 3D PDS designs that are easily implemented with commercially available components.

Reference

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