APPLICATION NOTE

cadence

Application Note: Best Practices for S-Parameter Extraction to Improve Time-Domain Convergence with Allegro Sigrity Tools

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Cadence Design Systems, Inc., 555 River Oaks Parkway, San Jose, CA 95134, USA

Contents

Overview

For Cadence® Sigrity™ SystemSI™ users, it is common practice to use Cadence Sigrity PowerSI™ as an extraction engine to produce S-parameter models that are used in SystemSI to build die-to-die topologies. One challenge in such a flow is non-convergence by the time-domain circuit simulator, especially when the S-parameter models involved have a large numbers of ports. There are a number of best practices that have emerged through experience that can make this process more robust. The purpose of this application note is to document those here. They fall into several categories:

- PowerSI recommendations applicable to both PCB and IC packages
- PowerSI IC package setup recommendations
  - Wirebonds
  - Flip-chip bumps
  - BGA balls
- Broadband SPICE conversion recommendations

This document does not cover basic usage of PowerSI and assumes intermediate experience with the tool. New users are encouraged to go through the PDN Impedance Extraction (PowerSI) Rapid Adoption Kit material as a prerequisite. A number of different Allegro® Sigrity workshops are also available that introduce PowerSI.

Section 1: PowerSI Recommendations for PCBs and IC Packages

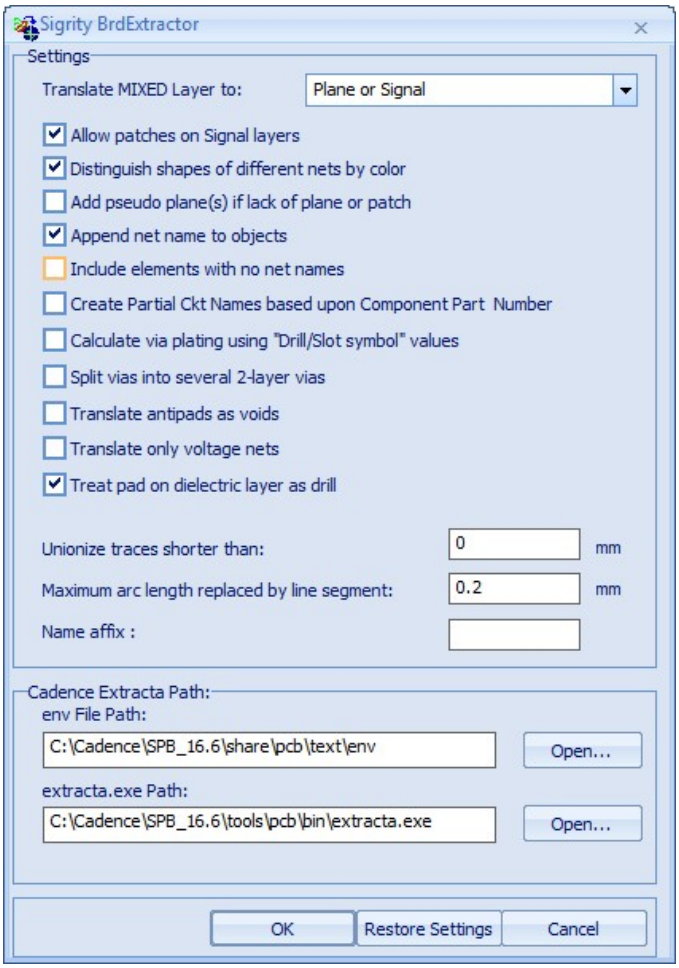
This section covers steps applicable to both PCB and IC packages:

- Translation options
- Stackup options
- Padstacks
- Net management
- Decoupling capacitor models
- Ports and their reference impedances
- Frequency sweep options
- S-parameter file formats
- Special voids

Translation of Cadence Layouts

The first step is to convert the Cadence database to the Sigrity “SPD” format. Before translation, check the design in Allegro for any short circuits and other design rule checks (DRCs).

Typically the checked boxes below should be selected.



Notes:

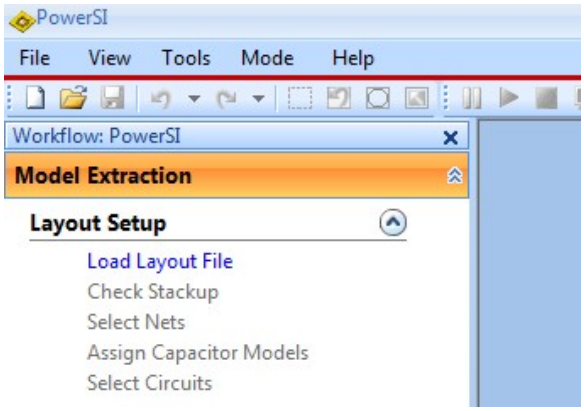
Via plating can also be translated if specified in the Allegro database “Drill / Slot symbol” information.

If non-functional pads will not be removed, select option “split vias into several 2-layer vias”. Note that this may significantly increase the size of the .spd file.

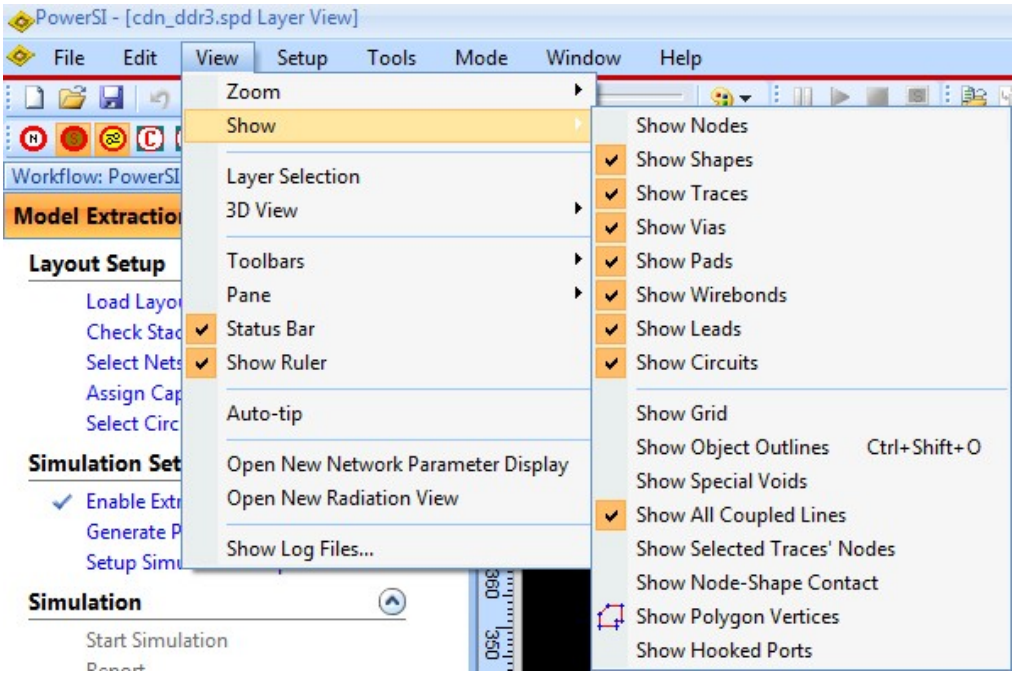
PowerSI GUI Setup

This section will walk through the major steps of the setup.

Under the Model Extraction workflow, click ***Load Layout File.***

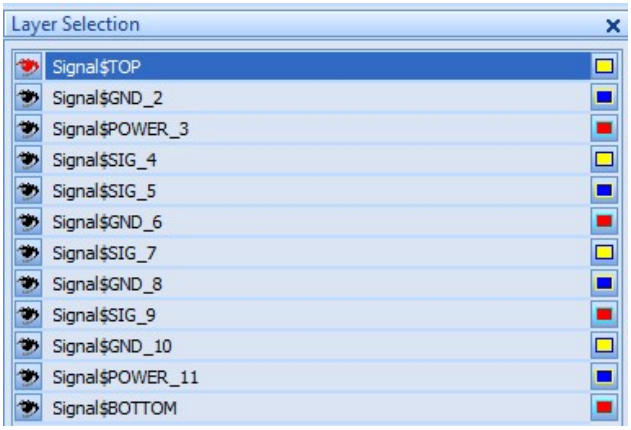


Under View > Show, turn items on or off to match the settings below. These are the typical view settings.



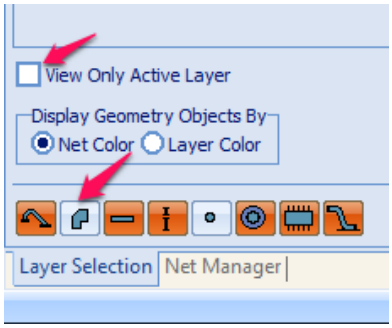
Note that “Show Nodes” is turned off. They are typically only turned on whenever circuits or ports are edited.

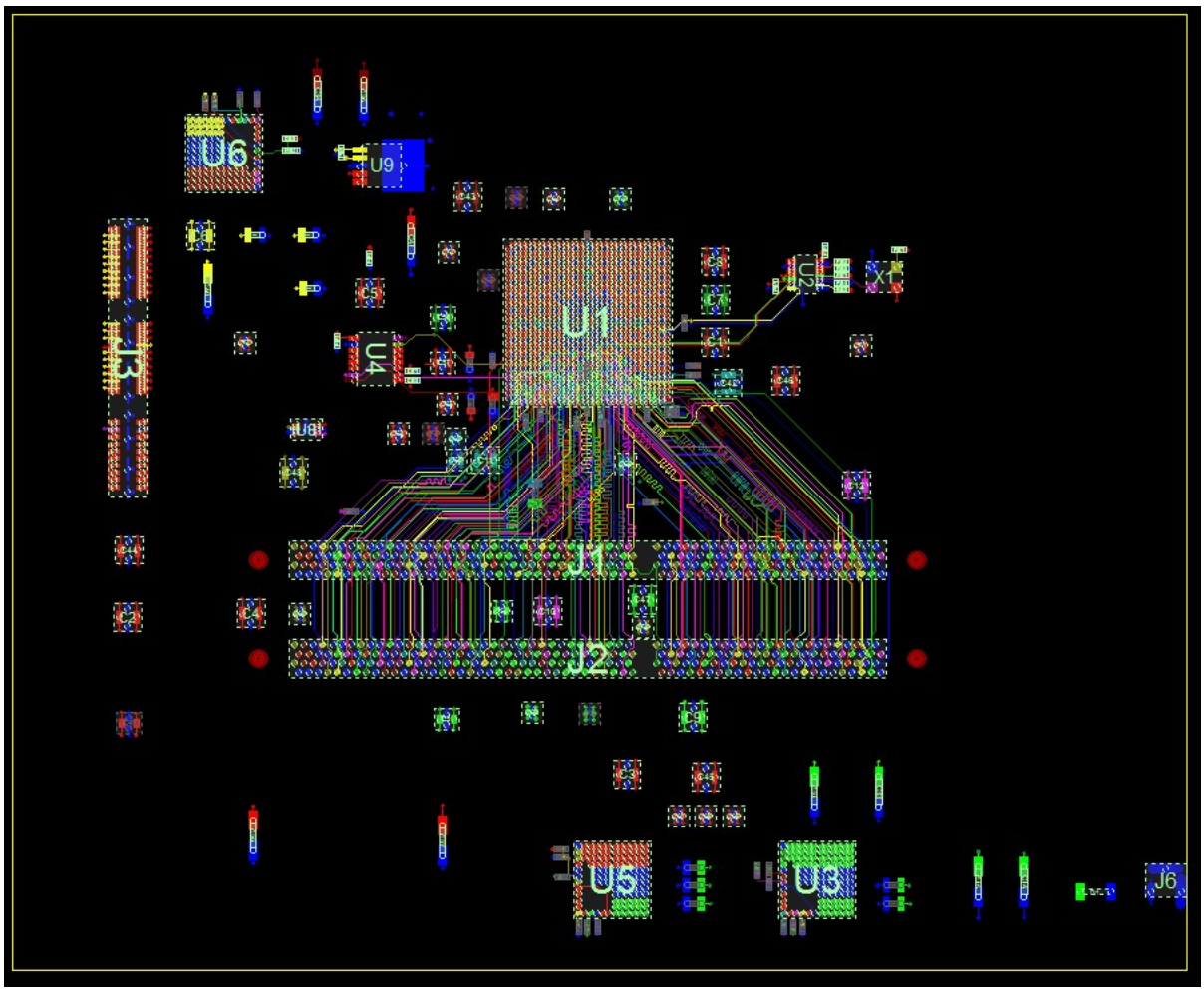
In the Layer Selection window pane, you can ***LMB*** on the layer name text (NOT the eye icon) to change the active layer.



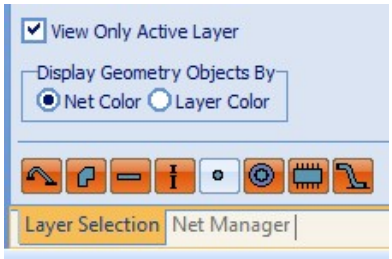
You can go through the layers as desired to get familiar with the stackup and routing.

At the bottom of the Layer Selection window pane, you can ***clear the check*** on ***View Only Active Layer*** and ***disable Show Shapes***. This will show all layers without shapes. This is useful to view only trace routing (see next page).



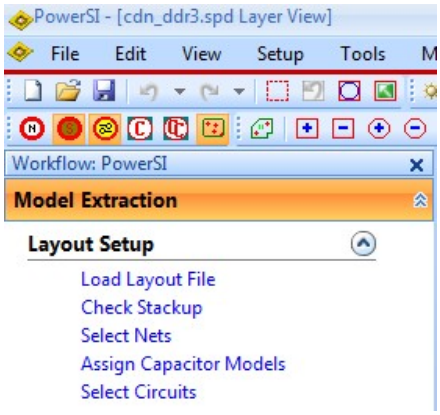


At the bottom of the Layer Selection window pane, ***check View Only Active Layer*** and ***enable Show Shapes***. This returns the GUI to the typical view settings.

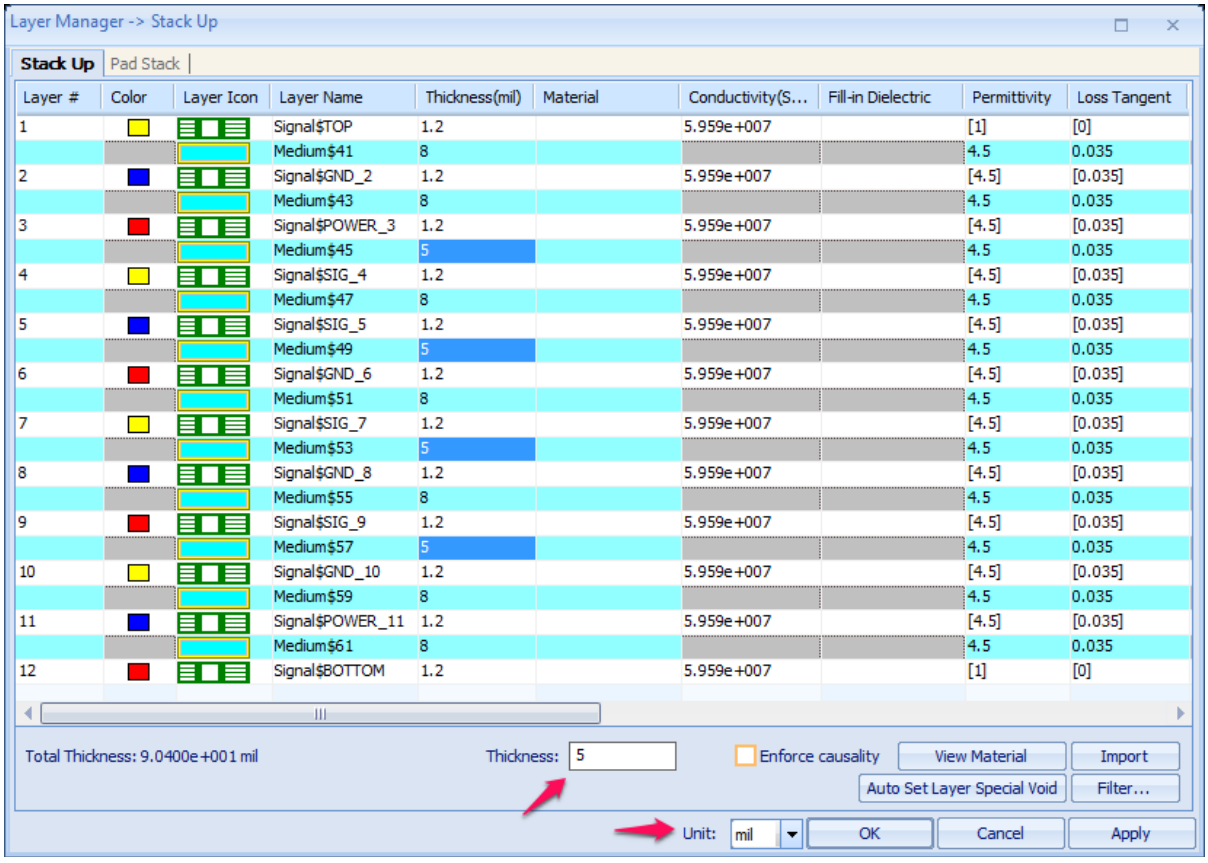


Stackup

On the Workflow, click ***Check Stackup***.

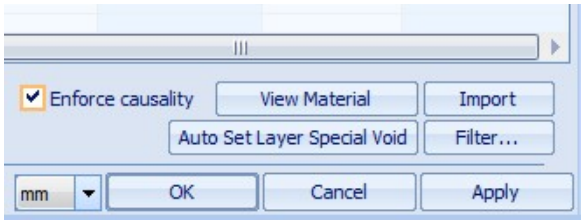


Inside the Stackup window, ***change units to mils*** with the drop-down selector. Using ***shift-LMB or ctrl-LMB*** select multiple cells and adjust their values at the same time.

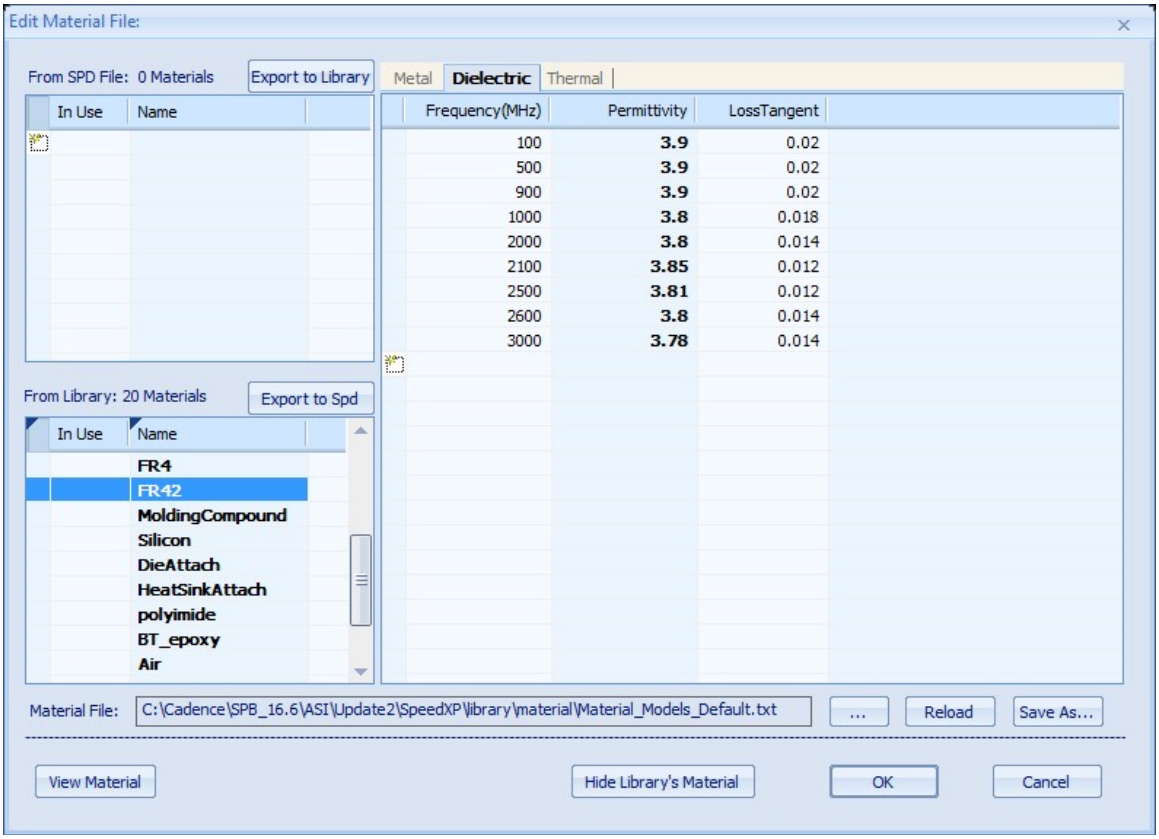


Enforce Causality

A frequency-independent material property with non-zero loss tangent is non-causal. In Cadence Sigrity SPEED2000™ (by default) and in PowerSI (by user option) we apply causal Debye material properties. In PowerSI this Debye model is applied only when the "Enforce Causality" checkbox is selected in the stackup editor.



Permittivity and loss tangent values can be constant or frequency dependent. Click View Material to and then Show Library's Material to see examples.

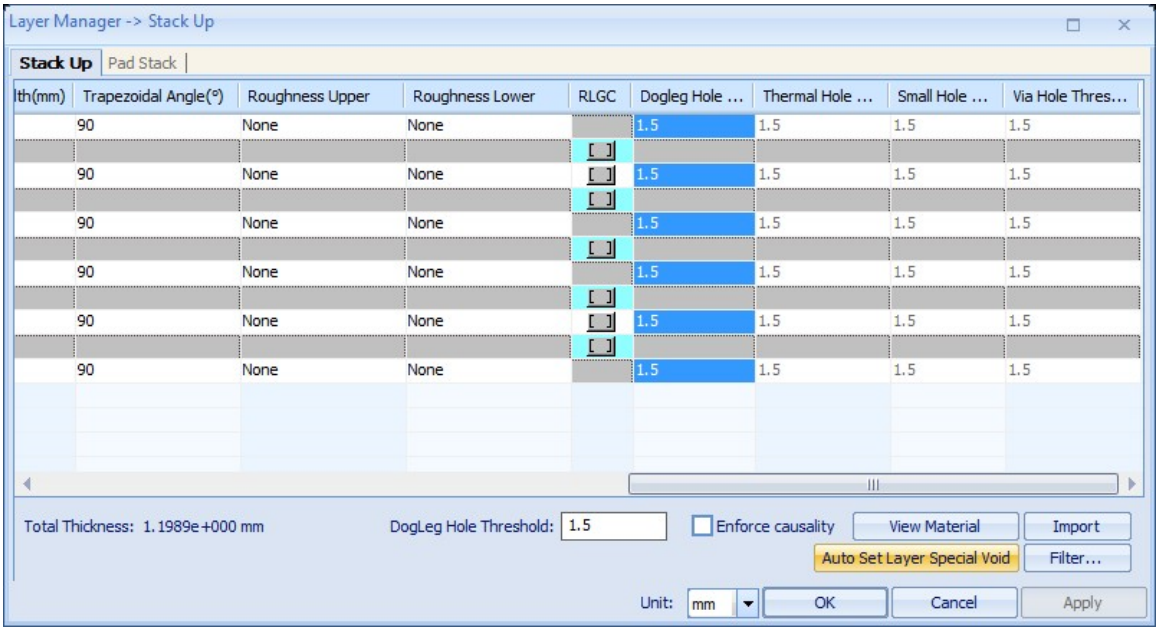


For the case of non-zero constant loss tangent, we apply a single-pole Debye frequency dependence with an extremely high resonance frequency that does not noticeably change the user-specified permittivity and loss tangent values at user simulation frequencies. The vast majority of customers fall into this category.

For the case of frequency-dependent material specification, we curve fit to a multi-pole Debye behavior to correspond as closely as possible to the user-specified data. There are no knobs for the user to turn other than adding more points to the table. But that's not usually an option unless you're measuring the dielectric materials; otherwise you could be using physically impossible values.

Per-Layer Special Voids

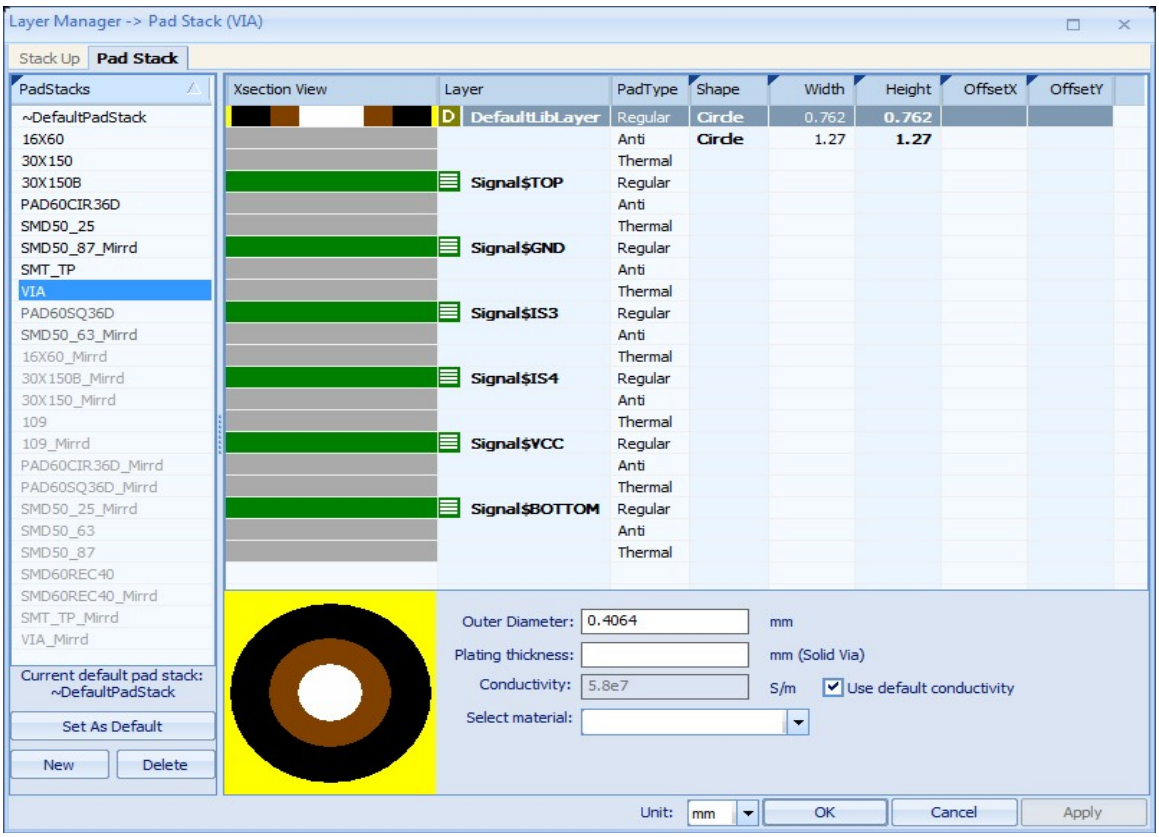
One of the most overlooked capabilities of the Stackup window is the ability to automatically set per-layer special voids. Special voids will be discussed in detail in a later section, but for now know that this option is highly recommended to help automate a more accurate setup. Just click ***Auto Set Layer Special Voids*.**



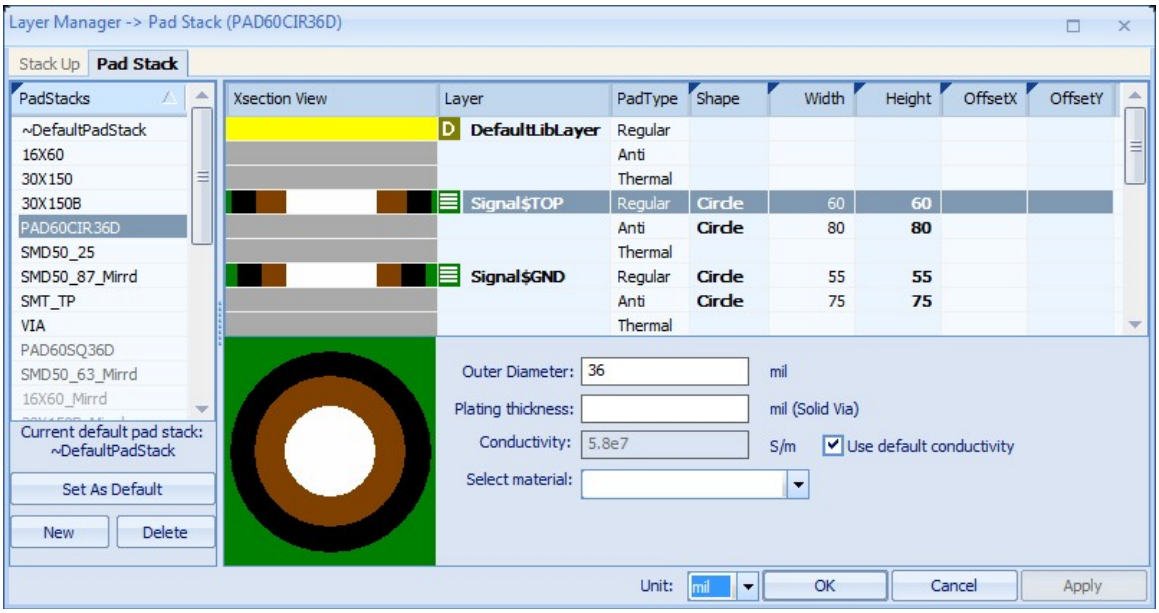
Padstacks

For simulation to create the most accurate via models, via plating, pad, and antipad sizes must be defined in the padstack library. Unfortunately pad stacks are not always set up in the layout database as there are multiple ways to define clearances in Allegro tools. It is highly recommended to update the layout database with complete pad stack information if at all possible.

There are two ways to enter data in the padstack library. The “DefaultLibLayer” is an easy way to make the same entries for all layers at once.

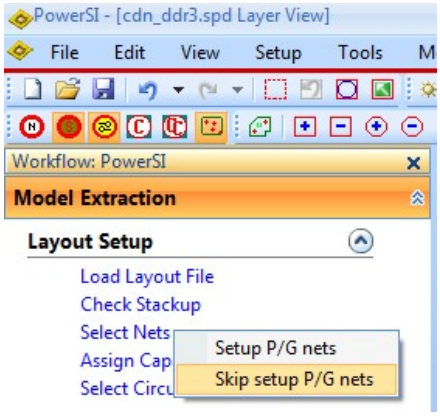


The other option is to specify per-layer values.

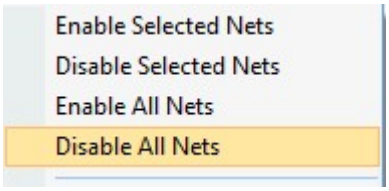


Net Management

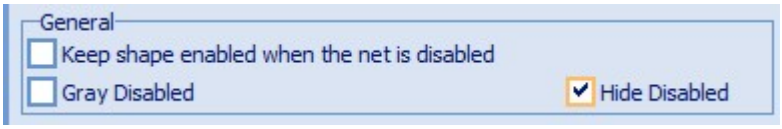
On the Workflow, click ***Select Nets***. A pop-up will appear. Select ***Skip setup P/G nets*** if you know the net names of interest. Choosing Setup P/G nets will open a wizard to identify nets for simulation.



If all nets were translated, it is usually best to first disable all nets and then selectively enable only the nets of interest. It is not common to enable all nets for simulation as that would yield unnecessarily long simulation time. RMB anywhere in the spreadsheet area of the Net Manager and select ***Disable All Nets***.



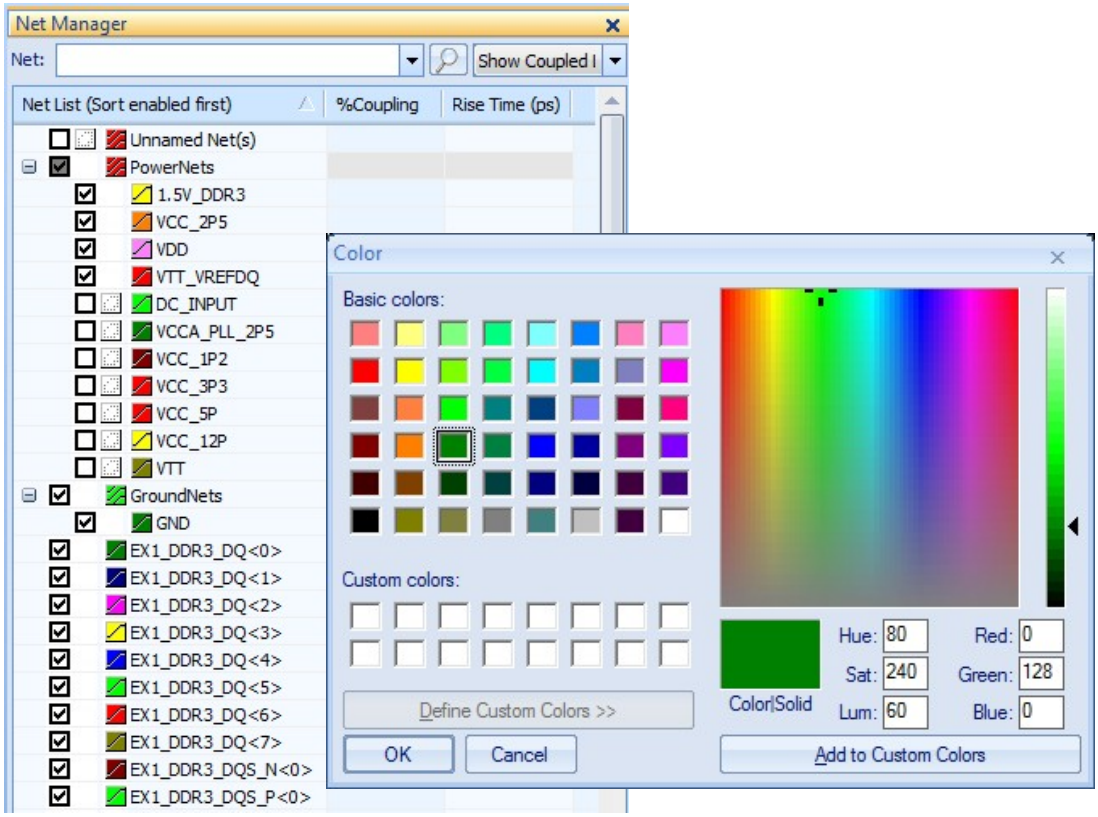
IMPORTANT: Note that you can still see the planes in the layout. At the bottom of the Net Manager, ***clear the check*** for ***Keep shape enabled when the net is disabled.***



When enabled, this option includes all planes in the simulation. This can lead to unacceptably long simulation times. This option is on by default to ensure good results for new users. It is better to take the time to selectively enable the necessary power nets to achieve the best balance between setup time and simulation time.

Check Hide Disabled if you don't want to see the disabled nets displayed in gray.

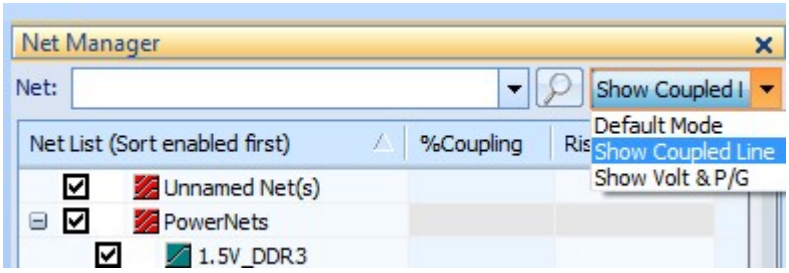
Change the power and ground nets display colors by ***LMC*** the ***colored square*** next to the net name. This is typically done to make it easier to identify a net's identity. The PowerSI port display uses red and green icons, so it's best to use ***dark green*** for the GND net as shown below and **anything other than red** for power nets.



Classify Net Groups – **classify at least one net to the Ground Net Group**. This is typically the largest digital ground net of the design. Power nets should be classified to the Power Net Group. These net groups are used by setup wizards such as assign capacitor models, port setup, and port reference impedance. While this step is not technically required, the wizards and automated setups will not work without it.

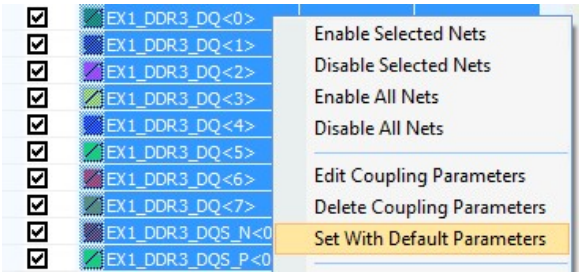
Trace Coupling

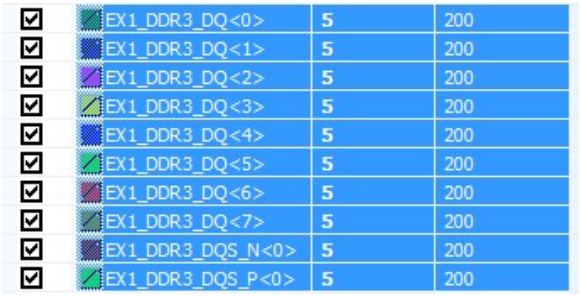
At the top right of Net Manager, click the pull-down and change the view mode to ***Show Coupled Line***.



In Hybrid Solvers, there are various switches available to make the computations for large/complex designs more efficient. Trace to trace coupling is one of these switches in Sigrity tools. By default, trace-to-trace couplings are unaccounted for unless the user specifies the Coupled Lines parameters. For many single-ended designs, this is acceptable since most trace couplings fall off quickly with separation distance. When trace coupling was first implemented, we did not want to force every computation to be prohibitively large... especially when large computer resources were costly.

To enable trace coupling, highlight the first signal net with ***LMC***. Then group-select all enabled signal nets with ***shift-LMC***. Then ***RMC*** anywhere in the blue highlighted area and select ***Set with Default Parameters***.





The % coupling value is a threshold. Anything larger will be included in simulation. Anything smaller will be discarded to improve simulation efficiency.

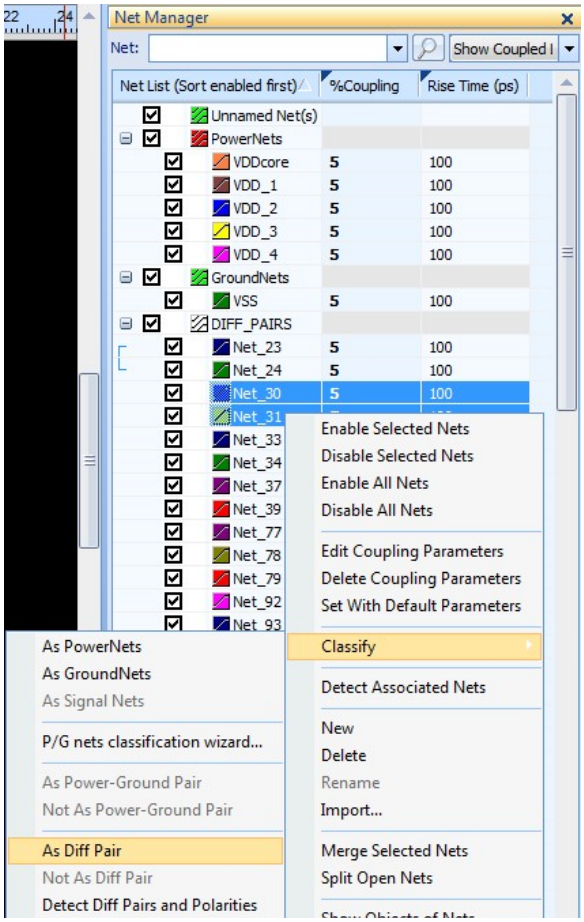
The default values of 200ps / 5% are a compromise between simulation time and accuracy. Smaller rise time and lower percentage can be applied for higher accuracy at a cost of longer simulations. Some users never change the values, while others often make the values much smaller (could potentially include much more coupling). There are no precise numerical values we can suggest to assure success; thus, our making available the two high-level specs to control coupling level and selecting a compromise default value for each.

The **coupled lines report** tells/shows you which couplings will be considered in the simulation. It's not an exact science, but if you look at the report and it intuitively seems that some couplings you suspect will be important are missing in a given region of your design, then simply use a lower coupling threshold and/or smaller rise time. After you specify such a low coupling level, it is always a good idea to look at the report before launching off a simulation, since you are at risk of including a LOT of couplings and getting a very slow simulation.

This is further described in the SPD layout user guide under section Show Coupled Lines Mode.

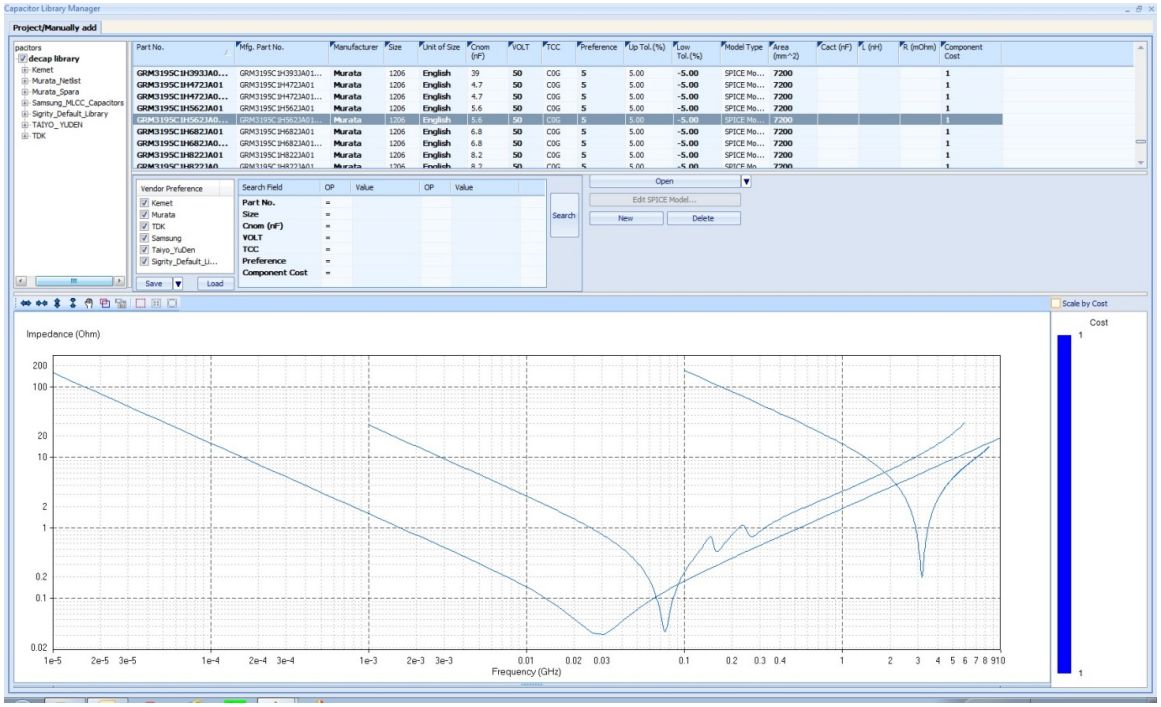
Differential Pairs

PowerSI can optionally calculate and display differential S-parameters. To enable these features, differential pairs must be identified in the Net Manager. Simply ***highlight the two nets of a pair, RMB in the blue area > Classify > As Diff Pair.*** The diff pair has been classified when a blue bracket appears to the left of the two net names.



Capacitor Models

The ASI installation includes thousands of decoupling capacitor models from multiple vendors. Many are measurement-based S-parameters, and these models vary widely in bandwidth. The responses of a few models are shown below as an example.

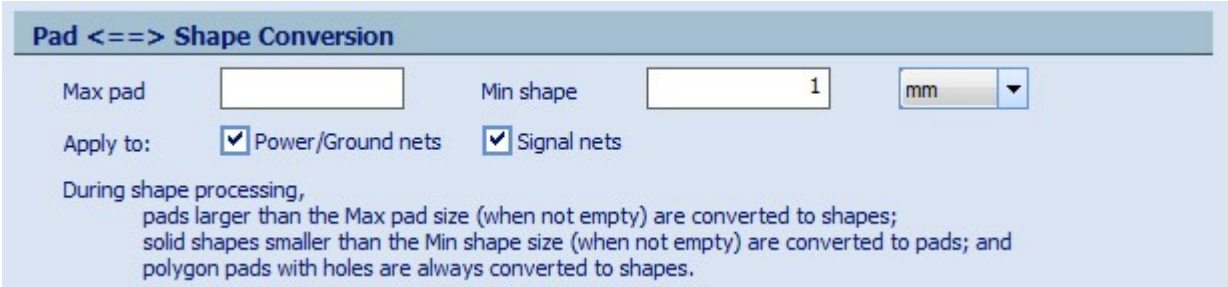


The simulation frequency range should not extend past the bandwidth of these models; otherwise PowerSI will have to extrapolate model response. Since this extrapolation may or may not be accurate, PowerSI will now warn the user if simulation bandwidth exceeds any S-parameter model's bandwidth. If it is necessary to use this model, it is recommended to lower the simulation bandwidth to match the capacitor model's bandwidth.

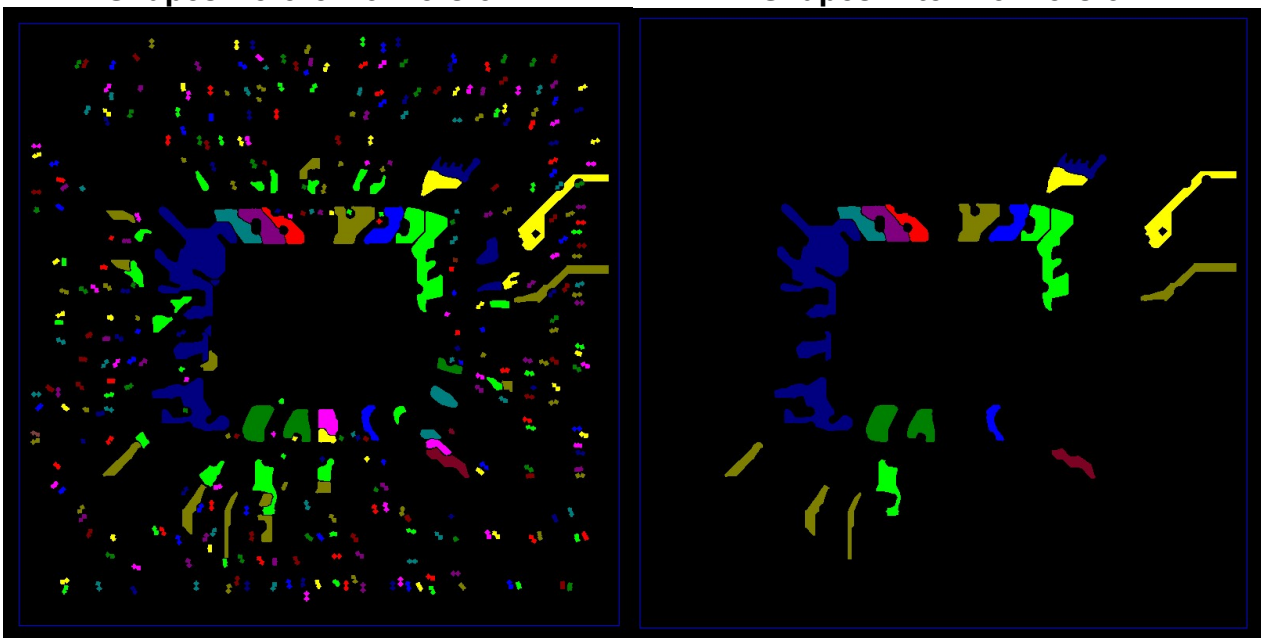
A more robust methodology is to use capacitor models built from SPICE elements, such as the Kemet, Murata (net list), and TDK libraries. These models should have valid response from DC to any frequency range appropriate for PowerSI.

Trace-to-Via Transitions (Fillets)

IC package and PCB layout tools have functions to add small transition shapes to the trace-via junctions. These very small shapes can cause difficulties for the shape meshing algorithms. It is highly recommended that these fillets not be added until simulation is complete. If they are present, though, convert them to pads with the Pad <==> Shape Conversion option.



Shapes Before Conversion **Shapes After Conversion**



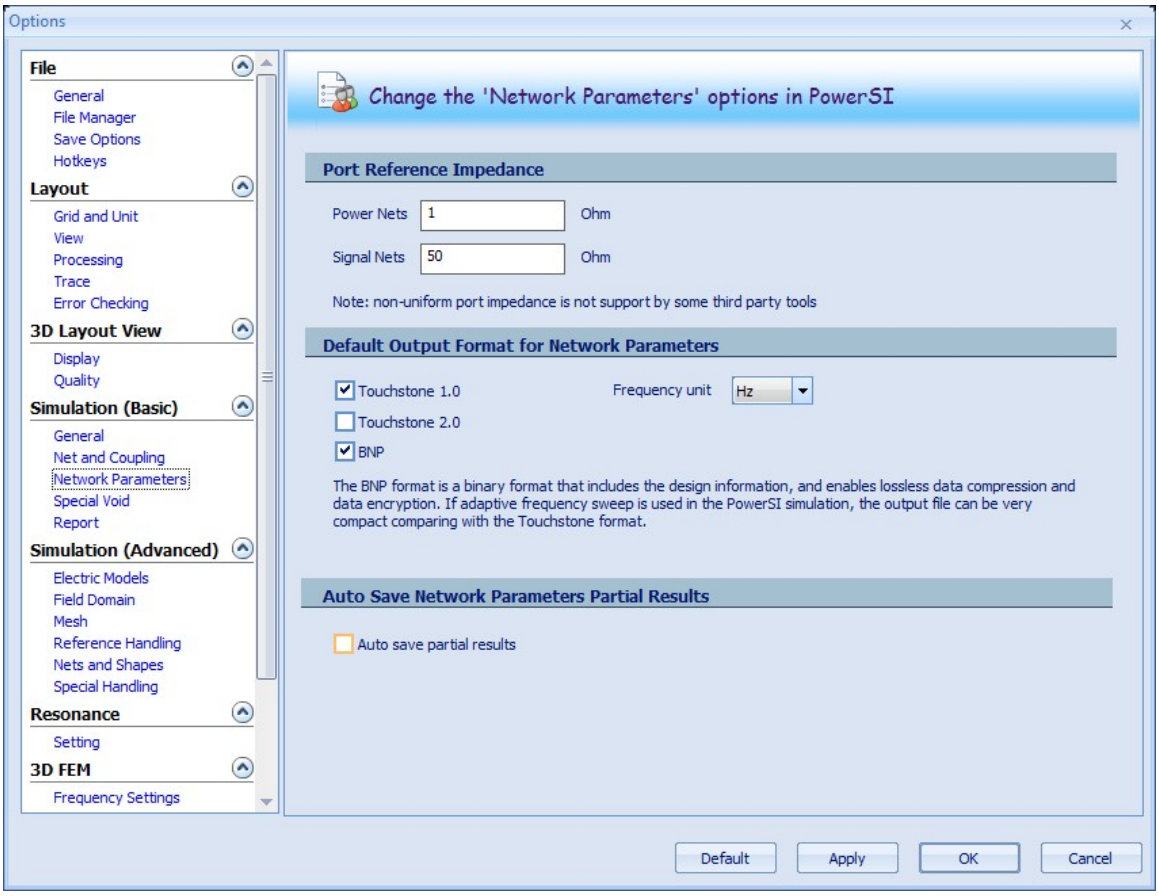
Ports

Net-based ports are automated with the Generate Port(s) wizard. It is most common to use a net-based approach until a more distributed, per-pin approach is mandated. Increasing the number of ports further complicates time-domain simulation, so the general recommendation is to use net-based ports if possible.

Port Reference Impedance

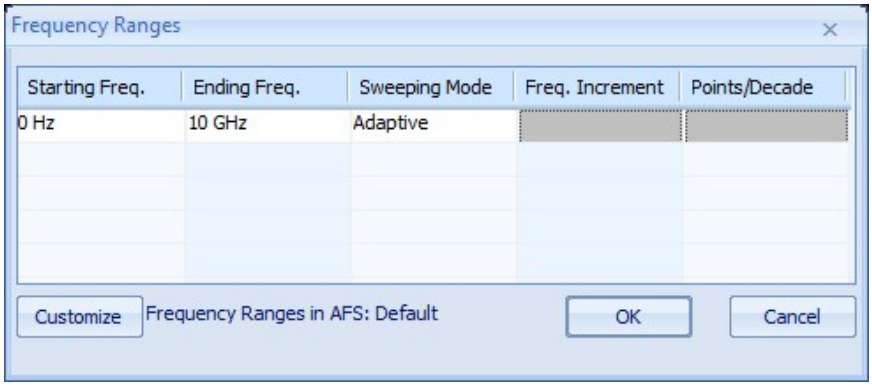
The original Touchstone format only allowed one reference impedance for all ports. Newer formats allow multiple reference impedances. The Network Parameters Options page allows independent settings for power and signal ports reference impedance.

In general, a small reference impedance for PDN ports can yield better results in Broadband SPICE's model conversion process. The idea is to choose a reference impedance near the impedance of the design under test (DUT). For PDN, this is typically a small value. There is no "one" correct/best choice for all situations, but **1 Ohm** and 0.1 Ohm are common choices.



Simulation Frequencies

PowerSI has an **adaptive** sampling algorithm that automatically solves the response between the specified starting and ending frequencies. It is highly recommended to use the Adaptive Frequency Sweep (AFS).



Note in the above picture a **Starting Frequency of 0 Hz**. This is a unique feature of the adaptive algorithm. Because field solvers become unstable as they are pushed toward DC, the first frequency that is actually calculated is 1kHz. The AFS algorithm extrapolates results below 1kHz to DC.

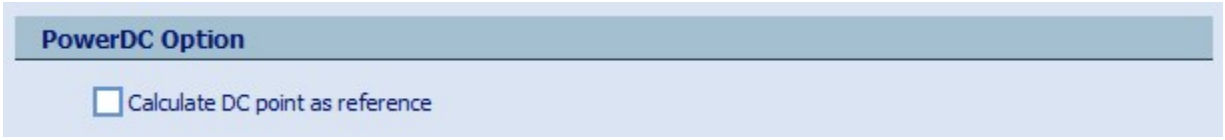
While 1kHz is very stable, in general it is not recommended to choose starting frequencies below 1kHz. **Do not choose 1Hz!** The starting frequency MUST be 0Hz to enable the AFS extrapolation.

To choose ending frequency, many users apply: **Fmax = 0.35 / rise time**

For more information on the derivation of this formula, please see: https://en.wikipedia.org/wiki/Rise_time

To further improve the low-frequency accuracy, in the Field Domain Options window, enable **Calculate DC point as reference**. This will run Cadence Sigrity PowerDC™ as a part of the PowerSI simulation to very accurately calculate the S-parameters' DC point.

Note: this option is not recommended for PCBs with large bulk decaps included in the PDN. Large bulk decaps cause low-frequency resonances that can be difficult to merge with PowerDC data. For those situations, if this option is desired it is recommended to disable the bulk decap and put a port at its location instead.

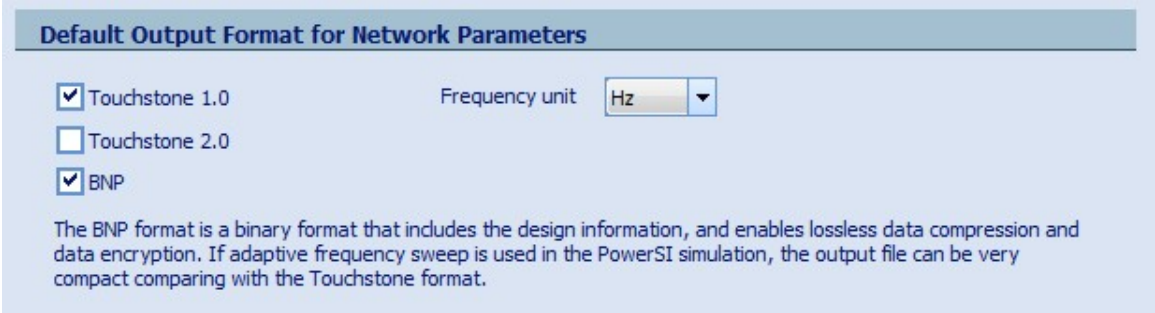


Simulation Options – BNP Format

Sigrity's Broadband Network Parameter (BNP) format was created to overcome the limitations of the original Touchstone format. One of the main reasons S-parameters can fail in time-domain simulation is due to extrapolation of data between Touchstone sampled points. These extrapolated points can fail passivity and / or causality, resulting in a non-convergent time-domain result.

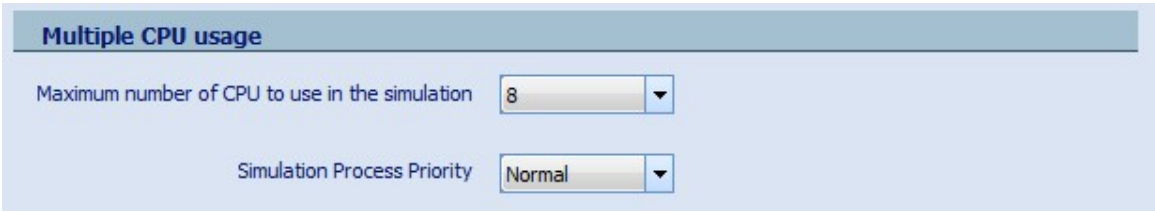
BNP has many benefits to improve time-domain convergence. If used with PowerSI Adaptive Frequency Sweep, BNP will store equation-based data that has response at any frequency between the minimum and maximum frequency sweep settings of PowerSI. This completely eliminates extrapolation problems. In addition to being more robust, the BNP file size is also much smaller; the file size savings increases as the number of ports increases. Some SPICE simulators have implemented native support for BNP, including HSPICE.

Note that Sigrity offers a free BNP viewer, and BNP data can be down-converted to sampled Touchstone data.



Simulation Options – CPUs

PowerSI can utilize multiple CPUs during some phases of the simulation. PowerSI can also utilize multiple computers for distributed simulation. This is mentioned simply to encourage users to allocate as many resources as possible to the simulation.

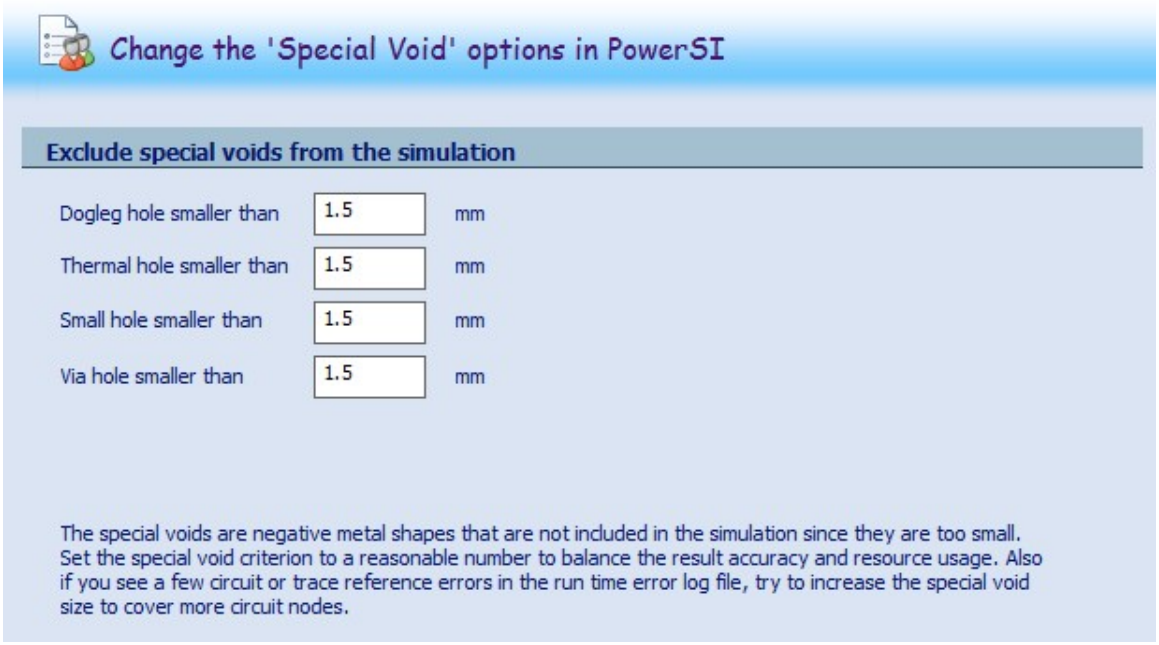


Simulation Options – Special Voids

Special voids are negative metal shapes that are not included in the simulation. These are very small geometries that can be ignored in an effort to improve simulation time. These adjustments can make simulations more accurate if used correctly or less accurate if used incorrectly. There is not one "correct" setting for special voids.

Without special voids, vias and their "breakout traces" do not have references. The vias are not in a field domain, so their coupling cannot be accurately calculated. At minimum, special void criteria should be set larger than single-ended and power/ground vias' antipad sizes.

The default size of 1.5mm is for IC package applications. Build-up packages with large core vias may need larger criteria. **The larger vias and antipads of PCBs require larger special voids settings. It is common for PCBs to set all special void criteria up to 5mm,** depending on the size of via antipads being used.



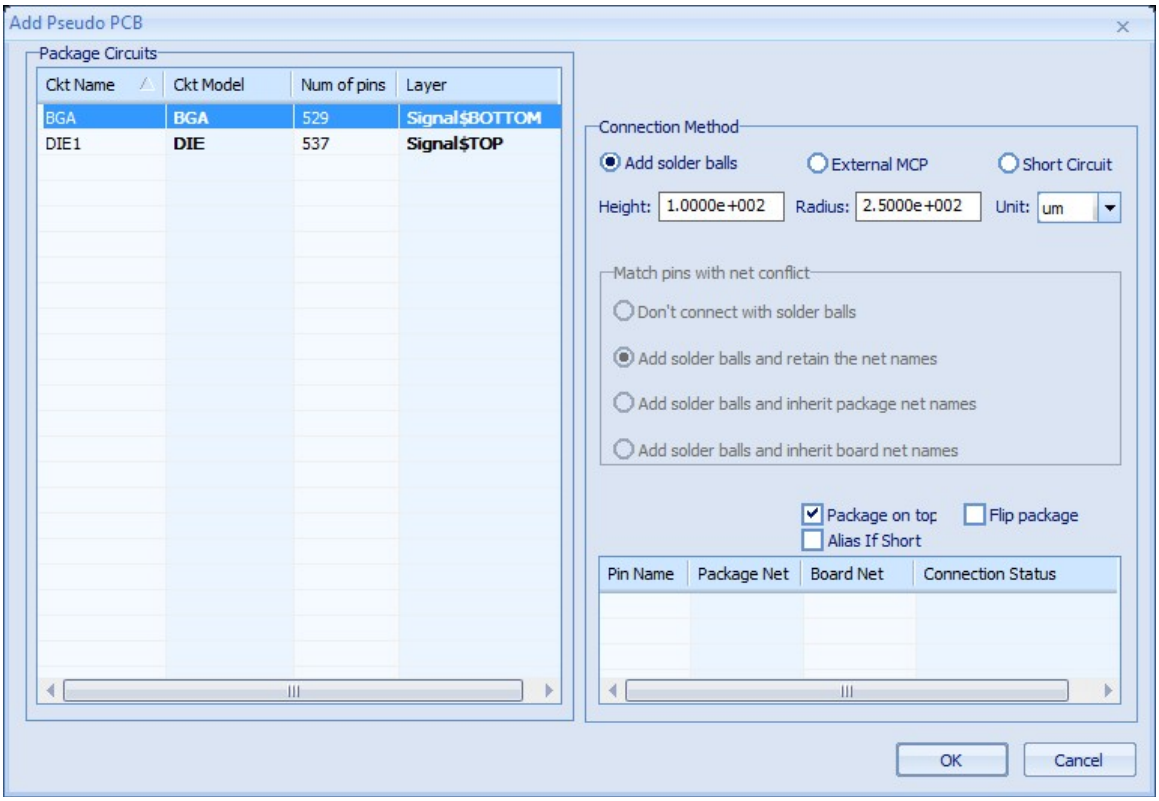
Section 2: PowerSI Recommendations for IC Packages

This section will provide recommendations that are specific to IC package designs. Note that Cadence Sigrity XtractIM™ is dedicated to IC packages and automates most of this section's recommendations. XtractIM also completely automates the S-parameter conversion to SPICE-based models. For most IC package applications, XtractIM is highly recommended instead of the PowerSI + Broadband SPICE flow.

BGA Setup

Most packages are drawn in Allegro APD/SiP without vias to represent the balls – this is the recommended flow. During package model extraction, however, it is usually desired to include the ball parasitics in the package model. Therefore, vias to represent the balls must be added in PowerSI.

There is an automated GUI for this step under **File > Merge > Pseudo PCB**. Select the BGA circuit, enter the ball physical properties, and click OK. Optional: assign the added plane to the GND net and set all GND vias' node contact = 1 in order to connect them to the plane.



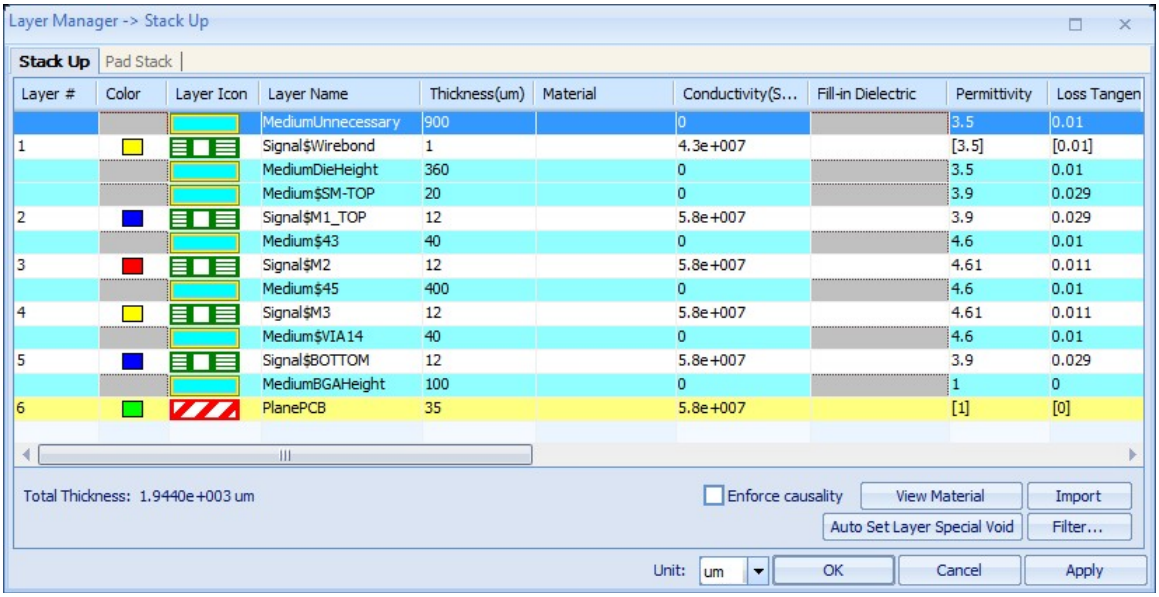
Flip-Chip Bumps

The Merge Pseudo PCB option shown above can be used a second time to add bumps on the top of a flip-chip package; simply **deselect the Package on Top option**. A plane will be added to the size of the entire package – reduce the size of that plane such that it slightly extends outside the bump area only.

It is recommended to assign the added plane to the GND net and set all GND vias' node contact = 1 in order to connect them to the plane. This will represent the impact of the chip above the package and yield a more accurate result.

Wirebond Die Height

It is not obvious in the Stackup window how to specify the die height. For the figure below, the die height is specified by the sum of all dielectric thicknesses between layers Signal$Wirebond and Signal$M1_TOP. In this example the die height is 380 um.



Wirebond Encapsulate / Molding

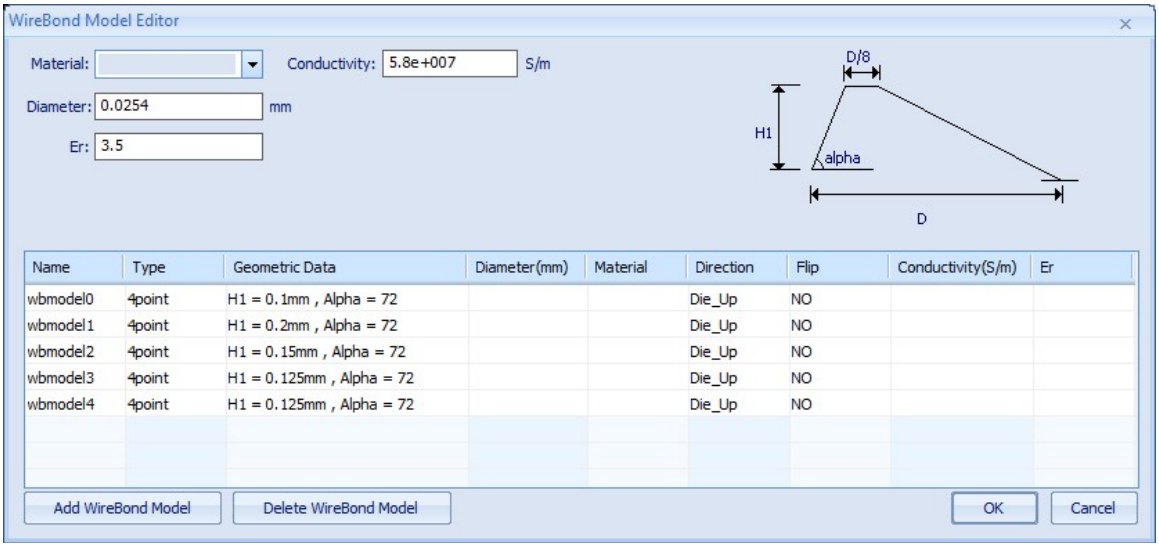
In the picture above, the highlighted layer “MediumUnncessary” typically should not be used. The wirebond material will be specified in the wirebond model library in the next step. If this layer is specified in the stackup, it will be applied over the entire package surface.

Wirebond Conductivity

Although there is a conductivity value in the stackup for the Signal$Wirebond layer, this value is NOT used during wirebond calculation. Wirebond conductivity is only specified in the wirebond model library.

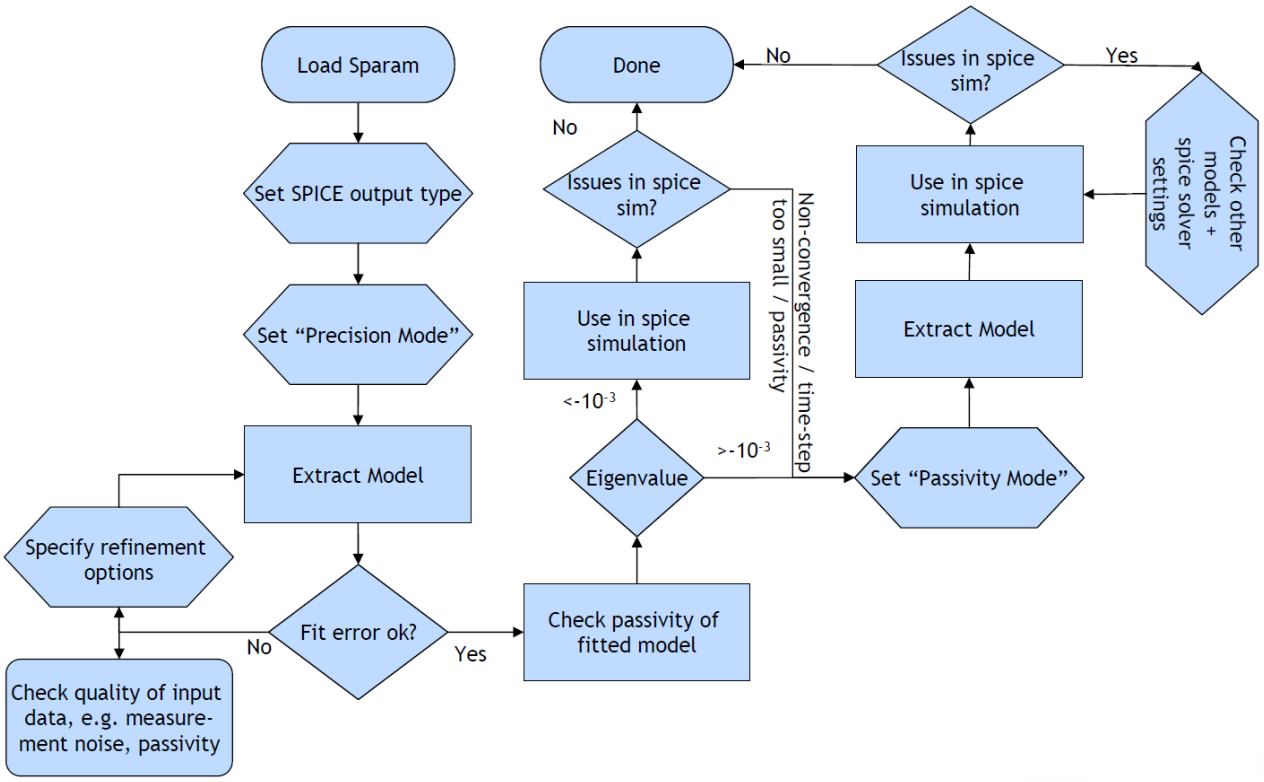
Wirebond Model Library

The wirebond model library is where the wirebond encapsulate / molding material's relative permittivity (Er) is specified. Ideally this value should match the Er of the die height dielectric material shown in the previous figure, but is not required in any way. Wirebond conductivity and all other parameters are also specified in this window.



Section 3: Model Conversion with Broadband SPICE

The final step of the PowerSI Model Extraction workflow is to “Generate a SPICE Model by Broadband SPICE”. It would take an entire application note to thoroughly cover all of Broadband SPICE’s options – the objective here is to highlight the availability of the two modes of conversion. The flowchart below provides an advanced use model of Broadband SPICE.



Precision Mode

The objective of precision mode is to extract an accurate equivalent circuit model that is loyal to the original S-parameters. This was the original mode of Broadband SPICE. It runs extremely fast, can handle any size of S-parameters, and rarely requires manual refinement shown in the bottom-left of the flowchart.

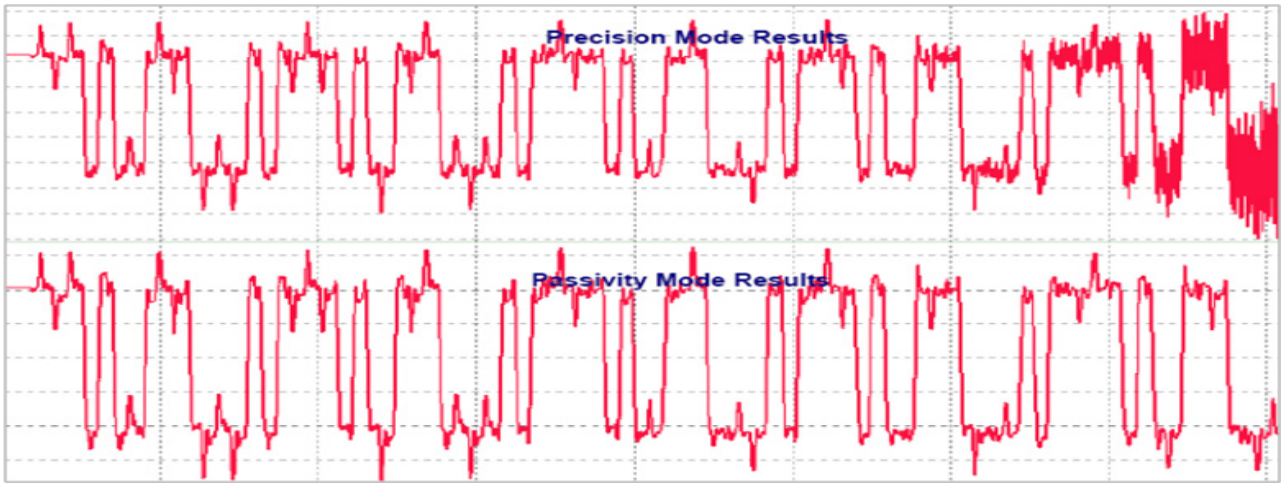
While the model fitting is extremely accurate, the drawback is that passivity is not enforced on the extracted model. These passivity violations may lead to problematic transient simulations. Broadband SPICE can perform passivity checking on the output model; this information can usually indicate the likelihood of time-convergence.

Passivity Mode

The objective of passivity mode is to rectify the main shortcoming of precision mode – guarantee passivity of the output model. Passivity mode is completely automatic, and the results are guaranteed to be passive. However, this comes at a cost of conversion time, memory requirement, and accuracy. By definition, this

model is not as accurate as precision mode because the S-parameters are being iteratively altered to enforce passivity. Capacity can also be an issue for a large number of ports and large bandwidths.

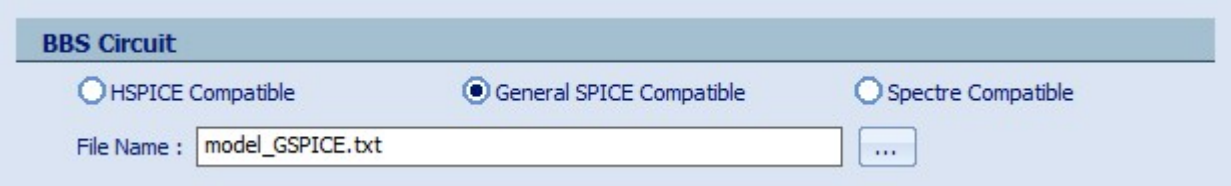
Even with these drawbacks, passivity mode can make the difference between a borderline passivity problem and a working simulation.



Broadband SPICE's Output File Formats

Broadband SPICE has multiple options for the output file's format. Theoretically, all formats should produce the same results in a subsequent SPICE simulation.

The "General SPICE" format is the most robust format, but newer techniques have file size and performance benefits. If "HSPICE compatible" is selected, Broadband SPICE will also output an "RFM" format. RFM has been found to simulate much faster in many test cases. In addition to HSPICE, RFM is also supported in SystemSI and SPEED2000.



Note: Do not use the "fitted" S-parameter output in time-domain simulation. These S-parameters are only for those wishing to perform detailed comparison of fitting accuracy.

Using S-Parameters Directly in Time-Domain Simulations

The S-parameters from PowerSI can be used directly in SystemSI, HSPICE, and many other SPICE simulators. If adaptive sweep and BNP format were used, these S-parameters may produce a perfectly valid time-domain result. However, this simulation will usually run much slower than one with a Broadband SPICE model instead. If using S-parameters directly, be sure to understand how the SPICE simulator handles S-parameters internally and any options available.

Summary / Checklist

A summary of the items covered in this document are listed below. This checklist can be used as quick reference during setup of a PowerSI and Broadband SPICE flow.

- **Translation** – review options
- **Stackup** – layer thicknesses, metal conductivity, dielectric properties, enforce causality, per-layer special voids
- **Padstacks** – pad and antipad sizes, plating thickness
- **Net management** – enable / disable nets, classify a ground net, trace coupling criteria, classify differential pairs
- **Capacitor models** – update ideal models with realistic SPICE-based or S-parameter models
- **Fillets** – check layout for small shapes at trace-to-via junctions and convert to pads
- **Ports** – net based, per-pin based, reference impedances
- **Simulation frequencies** – Adaptive sweep, start at 0Hz or 1kHz and above
- **Simulation options** – BNP format, set special voids criteria (especially for PCBs)
- **IC package setup** – BGA, flip-chip bumps, wirebond die height in stackup
- **Wirebond model library parameters** – encapsulate Er, profiles, conductivity, diameter
- **Model conversion with Broadband SPICE** – precision mode, passivity mode, file format

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